### Device Usage Page (usage\_statistics\_webtalk.html)

This HTML page displays the device usage statistics that will be sent to Xilinx.

To see the actual file transmitted to Xilinx, please click [here](http://docs.google.com/usage_statistics_webtalk.xml).

| **software\_version\_and\_target\_device** | | | |
| --- | --- | --- | --- |
| **beta** | FALSE | **build\_version** | 2405991 |
| **date\_generated** | Thu May 23 19:54:36 2019 | **os\_platform** | LIN64 |
| **product\_version** | Vivado v2018.3 (64-bit) | **project\_id** | 4067da432e3742488a6a1606dc3e6f5e |
| **project\_iteration** | 4 | **random\_id** | e15434ee65b35d6d93785cfbd4e35380 |
| **registration\_id** | e15434ee65b35d6d93785cfbd4e35380 | **route\_design** | TRUE |
| **target\_device** | xc7a100t | **target\_family** | artix7 |
| **target\_package** | csg324 | **target\_speed** | -1 |
| **tool\_flow** | Vivado |

| **user\_environment** | | | |
| --- | --- | --- | --- |
| **cpu\_name** | Intel(R) Core(TM) i7-7820HQ CPU @ 2.90GHz | **cpu\_speed** | 2903.475 MHz |
| **os\_name** | unknown | **os\_release** | unknown |
| **system\_ram** | 4.000 GB | **total\_processors** | 4 |

| **vivado\_usage** | | | |
| --- | --- | --- | --- |

| **gui\_handlers** | | | |
| --- | --- | --- | --- |
| abstractcombinedpanel\_remove\_selected\_elements=1 | basedialog\_cancel=2 | basedialog\_ok=92 | boardchooser\_board\_table=2 |
| cmdmsgdialog\_ok=14 | constraintschooserpanel\_create\_file=2 | createconstraintsfilepanel\_file\_name=1 | createsrcfiledialog\_file\_name=3 |
| createsrcfiledialog\_file\_type=1 | filesetpanel\_file\_set\_panel\_tree=23 | flownavigatortreepanel\_flow\_navigator\_tree=21 | iostandardcombobox\_choose\_io\_standard=1 |
| mainmenumgr\_edit=6 | mainmenumgr\_file=14 | mainmenumgr\_floorplanning=1 | mainmenumgr\_flow=2 |
| mainmenumgr\_io\_planning=1 | mainmenumgr\_open\_recent\_project=3 | mainmenumgr\_project=8 | mainmenumgr\_timing=1 |
| mainmenumgr\_tools=2 | maintoolbarmgr\_open=1 | pacommandnames\_add\_sources=1 | pacommandnames\_auto\_connect\_target=4 |
| pacommandnames\_auto\_update\_hier=1 | pacommandnames\_config\_bitstream=1 | pacommandnames\_goto\_netlist\_design=1 | pacommandnames\_new\_project=1 |
| pacommandnames\_open\_hardware\_manager=3 | pacommandnames\_open\_project=4 | pacommandnames\_run\_bitgen=4 | paviews\_code=1 |
| paviews\_project\_summary=4 | portmenu\_configure\_io\_ports=1 | programdebugtab\_open\_target=8 | programdebugtab\_program\_device=8 |
| programfpgadialog\_program=8 | projectnamechooser\_project\_name=1 | saveprojectutils\_reload=2 | saveprojectutils\_save=4 |
| searchcommandcomponent\_quick\_access=2 | signaltreepanel\_signal\_tree\_table=24 | srcchooserpanel\_add\_or\_create\_source\_file=1 | srcchooserpanel\_create\_file=5 |
| srcchoosertable\_src\_chooser\_table=3 | srcmenu\_ip\_hierarchy=1 |

| **java\_command\_handlers** | | | |
| --- | --- | --- | --- |
| addsources=1 | autoconnecttarget=4 | closeproject=1 | configurebitstream=1 |
| launchprogramfpga=4 | newproject=1 | openhardwaremanager=6 | openproject=4 |
| runbitgen=4 | runimplementation=7 | runsynthesis=8 | savedesign=2 |
| showview=5 | viewtaskprojectmanager=5 | viewtasksynthesis=3 |

| **other\_data** | | | |
| --- | --- | --- | --- |
| guimode=7 |

| **project\_data** | | | |
| --- | --- | --- | --- |
| constraintsetcount=1 | core\_container=false | currentimplrun=impl\_1 | currentsynthesisrun=synth\_1 |
| default\_library=xil\_defaultlib | designmode=RTL | export\_simulation\_activehdl=0 | export\_simulation\_ies=0 |
| export\_simulation\_modelsim=0 | export\_simulation\_questa=0 | export\_simulation\_riviera=0 | export\_simulation\_vcs=0 |
| export\_simulation\_xsim=0 | implstrategy=Vivado Implementation Defaults | launch\_simulation\_activehdl=0 | launch\_simulation\_ies=0 |
| launch\_simulation\_modelsim=0 | launch\_simulation\_questa=0 | launch\_simulation\_riviera=0 | launch\_simulation\_vcs=0 |
| launch\_simulation\_xsim=0 | simulator\_language=Mixed | srcsetcount=1 | synthesisstrategy=Vivado Synthesis Defaults |
| target\_language=Verilog | target\_simulator=XSim | totalimplruns=1 | totalsynthesisruns=1 |

| **unisim\_transformation** |
| --- |
| | **post\_unisim\_transformation** | | | | | --- | --- | --- | --- | | bufg=1 | fdre=5 | gnd=1 | ibuf=2 | | lut4=1 | obuf=5 | vcc=1 | |
| | **pre\_unisim\_transformation** | | | | | --- | --- | --- | --- | | bufg=1 | fdre=5 | gnd=1 | ibuf=2 | | lut4=1 | obuf=5 | vcc=1 | |

| **report\_drc** |
| --- |
| | **command\_line\_options** | | | | | --- | --- | --- | --- | | -append=default::[not\_specified] | -checks=default::[not\_specified] | -fail\_on=default::[not\_specified] | -force=default::[not\_specified] | | -format=default::[not\_specified] | -internal=default::[not\_specified] | -internal\_only=default::[not\_specified] | -messages=default::[not\_specified] | | -name=default::[not\_specified] | -no\_waivers=default::[not\_specified] | -return\_string=default::[not\_specified] | -ruledecks=default::[not\_specified] | | -upgrade\_cw=default::[not\_specified] | -waived=default::[not\_specified] | |
| | **results** | | | | | --- | --- | --- | --- | | cfgbvs-1=1 | plck-12=1 | |

| **report\_utilization** |
| --- |
| | **clocking** | | | | | --- | --- | --- | --- | | bufgctrl\_available=32 | bufgctrl\_fixed=0 | bufgctrl\_used=1 | bufgctrl\_util\_percentage=3.13 | | bufhce\_available=96 | bufhce\_fixed=0 | bufhce\_used=0 | bufhce\_util\_percentage=0.00 | | bufio\_available=24 | bufio\_fixed=0 | bufio\_used=0 | bufio\_util\_percentage=0.00 | | bufmrce\_available=12 | bufmrce\_fixed=0 | bufmrce\_used=0 | bufmrce\_util\_percentage=0.00 | | bufr\_available=24 | bufr\_fixed=0 | bufr\_used=0 | bufr\_util\_percentage=0.00 | | mmcme2\_adv\_available=6 | mmcme2\_adv\_fixed=0 | mmcme2\_adv\_used=0 | mmcme2\_adv\_util\_percentage=0.00 | | plle2\_adv\_available=6 | plle2\_adv\_fixed=0 | plle2\_adv\_used=0 | plle2\_adv\_util\_percentage=0.00 | |
| | **dsp** | | | | | --- | --- | --- | --- | | dsps\_available=240 | dsps\_fixed=0 | dsps\_used=0 | dsps\_util\_percentage=0.00 | |
| | **io\_standard** | | | | | --- | --- | --- | --- | | blvds\_25=0 | diff\_hstl\_i=0 | diff\_hstl\_i\_18=0 | diff\_hstl\_ii=0 | | diff\_hstl\_ii\_18=0 | diff\_hsul\_12=0 | diff\_mobile\_ddr=0 | diff\_sstl135=0 | | diff\_sstl135\_r=0 | diff\_sstl15=0 | diff\_sstl15\_r=0 | diff\_sstl18\_i=0 | | diff\_sstl18\_ii=0 | hstl\_i=0 | hstl\_i\_18=0 | hstl\_ii=0 | | hstl\_ii\_18=0 | hsul\_12=0 | lvcmos12=0 | lvcmos15=0 | | lvcmos18=0 | lvcmos25=0 | lvcmos33=1 | lvds\_25=0 | | lvttl=0 | mini\_lvds\_25=0 | mobile\_ddr=0 | pci33\_3=0 | | ppds\_25=0 | rsds\_25=0 | sstl135=0 | sstl135\_r=0 | | sstl15=0 | sstl15\_r=0 | sstl18\_i=0 | sstl18\_ii=0 | | tmds\_33=0 | |
| | **memory** | | | | | --- | --- | --- | --- | | block\_ram\_tile\_available=135 | block\_ram\_tile\_fixed=0 | block\_ram\_tile\_used=0 | block\_ram\_tile\_util\_percentage=0.00 | | ramb18\_available=270 | ramb18\_fixed=0 | ramb18\_used=0 | ramb18\_util\_percentage=0.00 | | ramb36\_fifo\_available=135 | ramb36\_fifo\_fixed=0 | ramb36\_fifo\_used=0 | ramb36\_fifo\_util\_percentage=0.00 | |
| | **primitives** | | | | | --- | --- | --- | --- | | bufg\_functional\_category=Clock | bufg\_used=1 | fdre\_functional\_category=Flop & Latch | fdre\_used=7 | | ibuf\_functional\_category=IO | ibuf\_used=2 | lut4\_functional\_category=LUT | lut4\_used=1 | | obuf\_functional\_category=IO | obuf\_used=5 | |
| | **slice\_logic** | | | | | --- | --- | --- | --- | | f7\_muxes\_available=31700 | f7\_muxes\_fixed=0 | f7\_muxes\_used=0 | f7\_muxes\_util\_percentage=0.00 | | f8\_muxes\_available=15850 | f8\_muxes\_fixed=0 | f8\_muxes\_used=0 | f8\_muxes\_util\_percentage=0.00 | | lut\_as\_logic\_available=63400 | lut\_as\_logic\_fixed=0 | lut\_as\_logic\_used=1 | lut\_as\_logic\_util\_percentage=<0.01 | | lut\_as\_memory\_available=19000 | lut\_as\_memory\_fixed=0 | lut\_as\_memory\_used=0 | lut\_as\_memory\_util\_percentage=0.00 | | register\_as\_flip\_flop\_available=126800 | register\_as\_flip\_flop\_fixed=0 | register\_as\_flip\_flop\_used=7 | register\_as\_flip\_flop\_util\_percentage=<0.01 | | register\_as\_latch\_available=126800 | register\_as\_latch\_fixed=0 | register\_as\_latch\_used=0 | register\_as\_latch\_util\_percentage=0.00 | | slice\_luts\_available=63400 | slice\_luts\_fixed=0 | slice\_luts\_used=1 | slice\_luts\_util\_percentage=<0.01 | | slice\_registers\_available=126800 | slice\_registers\_fixed=0 | slice\_registers\_used=7 | slice\_registers\_util\_percentage=<0.01 | | lut\_as\_distributed\_ram\_fixed=0 | lut\_as\_distributed\_ram\_used=0 | lut\_as\_logic\_available=63400 | lut\_as\_logic\_fixed=0 | | lut\_as\_logic\_used=1 | lut\_as\_logic\_util\_percentage=<0.01 | lut\_as\_memory\_available=19000 | lut\_as\_memory\_fixed=0 | | lut\_as\_memory\_used=0 | lut\_as\_memory\_util\_percentage=0.00 | lut\_as\_shift\_register\_fixed=0 | lut\_as\_shift\_register\_used=0 | | lut\_in\_front\_of\_the\_register\_is\_unused\_fixed=0 | lut\_in\_front\_of\_the\_register\_is\_unused\_used=5 | lut\_in\_front\_of\_the\_register\_is\_used\_fixed=5 | lut\_in\_front\_of\_the\_register\_is\_used\_used=1 | | register\_driven\_from\_outside\_the\_slice\_fixed=1 | register\_driven\_from\_outside\_the\_slice\_used=6 | register\_driven\_from\_within\_the\_slice\_fixed=6 | register\_driven\_from\_within\_the\_slice\_used=1 | | slice\_available=15850 | slice\_fixed=0 | slice\_registers\_available=126800 | slice\_registers\_fixed=0 | | slice\_registers\_used=7 | slice\_registers\_util\_percentage=<0.01 | slice\_used=2 | slice\_util\_percentage=0.01 | | slicel\_fixed=0 | slicel\_used=2 | slicem\_fixed=0 | slicem\_used=0 | | unique\_control\_sets\_available=15850 | unique\_control\_sets\_fixed=15850 | unique\_control\_sets\_used=1 | unique\_control\_sets\_util\_percentage=<0.01 | | using\_o5\_and\_o6\_fixed=<0.01 | using\_o5\_and\_o6\_used=0 | using\_o5\_output\_only\_fixed=0 | using\_o5\_output\_only\_used=0 | | using\_o6\_output\_only\_fixed=0 | using\_o6\_output\_only\_used=1 | |
| | **specific\_feature** | | | | | --- | --- | --- | --- | | bscane2\_available=4 | bscane2\_fixed=0 | bscane2\_used=0 | bscane2\_util\_percentage=0.00 | | capturee2\_available=1 | capturee2\_fixed=0 | capturee2\_used=0 | capturee2\_util\_percentage=0.00 | | dna\_port\_available=1 | dna\_port\_fixed=0 | dna\_port\_used=0 | dna\_port\_util\_percentage=0.00 | | efuse\_usr\_available=1 | efuse\_usr\_fixed=0 | efuse\_usr\_used=0 | efuse\_usr\_util\_percentage=0.00 | | frame\_ecce2\_available=1 | frame\_ecce2\_fixed=0 | frame\_ecce2\_used=0 | frame\_ecce2\_util\_percentage=0.00 | | icape2\_available=2 | icape2\_fixed=0 | icape2\_used=0 | icape2\_util\_percentage=0.00 | | pcie\_2\_1\_available=1 | pcie\_2\_1\_fixed=0 | pcie\_2\_1\_used=0 | pcie\_2\_1\_util\_percentage=0.00 | | startupe2\_available=1 | startupe2\_fixed=0 | startupe2\_used=0 | startupe2\_util\_percentage=0.00 | | xadc\_available=1 | xadc\_fixed=0 | xadc\_used=0 | xadc\_util\_percentage=0.00 | |

| **synthesis** |
| --- |
| | **command\_line\_options** | | | | | --- | --- | --- | --- | | -assert=default::[not\_specified] | -bufg=default::12 | -cascade\_dsp=default::auto | -constrset=default::[not\_specified] | | -control\_set\_opt\_threshold=default::auto | -directive=default::default | -fanout\_limit=default::10000 | -flatten\_hierarchy=default::rebuilt | | -fsm\_extraction=default::auto | -gated\_clock\_conversion=default::off | -generic=default::[not\_specified] | -include\_dirs=default::[not\_specified] | | -keep\_equivalent\_registers=default::[not\_specified] | -max\_bram=default::-1 | -max\_bram\_cascade\_height=default::-1 | -max\_dsp=default::-1 | | -max\_uram=default::-1 | -max\_uram\_cascade\_height=default::-1 | -mode=default::default | -name=default::[not\_specified] | | -no\_lc=default::[not\_specified] | -no\_srlextract=default::[not\_specified] | -no\_timing\_driven=default::[not\_specified] | -part=xc7a100tcsg324-1 | | -resource\_sharing=default::auto | -retiming=default::[not\_specified] | -rtl=default::[not\_specified] | -rtl\_skip\_constraints=default::[not\_specified] | | -rtl\_skip\_ip=default::[not\_specified] | -seu\_protect=default::none | -sfcu=default::[not\_specified] | -shreg\_min\_size=default::3 | | -top=Lab10\_SEQ | -verilog\_define=default::[not\_specified] | |
| | **usage** | | | | | --- | --- | --- | --- | | elapsed=00:00:11s | hls\_ip=0 | memory\_gain=315.906MB | memory\_peak=1700.180MB | |