\*\*\* Running vivado

with args -log Lab10\_Wave.vdi -applog -m64 -product Vivado -messageDb vivado.pb -mode batch -source Lab10\_Wave.tcl -notrace

\*\*\*\*\*\* Vivado v2018.3 (64-bit)

\*\*\*\* SW Build 2405991 on Thu Dec 6 23:36:41 MST 2018

\*\*\*\* IP Build 2404404 on Fri Dec 7 01:43:56 MST 2018

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CRITICAL WARNING: [Common 17-741] No write access right to the local Tcl store at '/home/jinson/.Xilinx/Vivado/2018.3/XilinxTclStore'. XilinxTclStore is reverted to the installation area. If you want to use local Tcl Store, please change the access right and relaunch Vivado.

source Lab10\_Wave.tcl -notrace

Command: open\_checkpoint /home/jinson/vivado/Lab10\_Wave/Lab10\_Wave.runs/impl\_1/Lab10\_Wave.dcp

Starting open\_checkpoint Task

Time (s): cpu = 00:00:00.03 ; elapsed = 00:00:00.07 . Memory (MB): peak = 1387.270 ; gain = 0.000 ; free physical = 838 ; free virtual = 2994

INFO: [Netlist 29-17] Analyzing 7 Unisim elements for replacement

INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds

INFO: [Project 1-479] Netlist was created with Vivado 2018.3

INFO: [Device 21-403] Loading part xc7a100tcsg324-1

INFO: [Project 1-570] Preparing netlist for logic optimization

INFO: [Timing 38-478] Restoring timing data from binary archive.

INFO: [Timing 38-479] Binary timing data restore complete.

INFO: [Project 1-856] Restoring constraints from binary archive.

INFO: [Project 1-853] Binary constraint restore complete.

Reading XDEF placement.

Reading placer database...

Reading XDEF routing.

Read XDEF File: Time (s): cpu = 00:00:00.09 ; elapsed = 00:00:00.13 . Memory (MB): peak = 1912.219 ; gain = 0.000 ; free physical = 207 ; free virtual = 2364

Restored from archive | CPU: 0.130000 secs | Memory: 0.994278 MB |

Finished XDEF File Restore: Time (s): cpu = 00:00:00.09 ; elapsed = 00:00:00.13 . Memory (MB): peak = 1912.219 ; gain = 0.000 ; free physical = 207 ; free virtual = 2364

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1912.219 ; gain = 0.000 ; free physical = 208 ; free virtual = 2364

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

INFO: [Project 1-604] Checkpoint was created with Vivado v2018.3 (64-bit) build 2405991

open\_checkpoint: Time (s): cpu = 00:00:09 ; elapsed = 00:00:10 . Memory (MB): peak = 1912.219 ; gain = 524.949 ; free physical = 207 ; free virtual = 2364

Command: opt\_design

Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'

INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t'

Running DRC as a precondition to command opt\_design

Starting DRC Task

INFO: [DRC 23-27] Running DRC with 4 threads

INFO: [Project 1-461] DRC finished with 0 Errors

INFO: [Project 1-462] Please refer to the DRC report (report\_drc) for more information.

Time (s): cpu = 00:00:00.98 ; elapsed = 00:00:01 . Memory (MB): peak = 1949.234 ; gain = 37.016 ; free physical = 202 ; free virtual = 2358

Starting Cache Timing Information Task

INFO: [Timing 38-35] Done setting XDC timing constraints.

Ending Cache Timing Information Task | Checksum: 1c9419230

Time (s): cpu = 00:00:00.02 ; elapsed = 00:00:00.02 . Memory (MB): peak = 2017.234 ; gain = 68.000 ; free physical = 202 ; free virtual = 2358

Starting Logic Optimization Task

Phase 1 Retarget

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

INFO: [Opt 31-49] Retargeted 0 cell(s).

Phase 1 Retarget | Checksum: 1c9419230

Time (s): cpu = 00:00:00.10 ; elapsed = 00:00:00.19 . Memory (MB): peak = 2077.234 ; gain = 0.000 ; free physical = 136 ; free virtual = 2293

INFO: [Opt 31-389] Phase Retarget created 0 cells and removed 0 cells

Phase 2 Constant propagation

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

Phase 2 Constant propagation | Checksum: 1c9419230

Time (s): cpu = 00:00:00.10 ; elapsed = 00:00:00.19 . Memory (MB): peak = 2077.234 ; gain = 0.000 ; free physical = 136 ; free virtual = 2293

INFO: [Opt 31-389] Phase Constant propagation created 0 cells and removed 0 cells

Phase 3 Sweep

Phase 3 Sweep | Checksum: 1eacbeff4

Time (s): cpu = 00:00:00.10 ; elapsed = 00:00:00.20 . Memory (MB): peak = 2077.234 ; gain = 0.000 ; free physical = 136 ; free virtual = 2293

INFO: [Opt 31-389] Phase Sweep created 0 cells and removed 0 cells

Phase 4 BUFG optimization

Phase 4 BUFG optimization | Checksum: 1eacbeff4

Time (s): cpu = 00:00:00.10 ; elapsed = 00:00:00.20 . Memory (MB): peak = 2077.234 ; gain = 0.000 ; free physical = 136 ; free virtual = 2293

INFO: [Opt 31-662] Phase BUFG optimization created 0 cells of which 0 are BUFGs and removed 0 cells.

Phase 5 Shift Register Optimization

Phase 5 Shift Register Optimization | Checksum: 139e370ad

Time (s): cpu = 00:00:00.12 ; elapsed = 00:00:00.22 . Memory (MB): peak = 2077.234 ; gain = 0.000 ; free physical = 136 ; free virtual = 2293

INFO: [Opt 31-389] Phase Shift Register Optimization created 0 cells and removed 0 cells

Phase 6 Post Processing Netlist

Phase 6 Post Processing Netlist | Checksum: 139e370ad

Time (s): cpu = 00:00:00.12 ; elapsed = 00:00:00.22 . Memory (MB): peak = 2077.234 ; gain = 0.000 ; free physical = 136 ; free virtual = 2293

INFO: [Opt 31-389] Phase Post Processing Netlist created 0 cells and removed 0 cells

Opt\_design Change Summary

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-------------------------------------------------------------------------------------------------------------------------

| Phase | #Cells created | #Cells Removed | #Constrained objects preventing optimizations |

-------------------------------------------------------------------------------------------------------------------------

| Retarget | 0 | 0 | 0 |

| Constant propagation | 0 | 0 | 0 |

| Sweep | 0 | 0 | 0 |

| BUFG optimization | 0 | 0 | 0 |

| Shift Register Optimization | 0 | 0 | 0 |

| Post Processing Netlist | 0 | 0 | 0 |

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Starting Connectivity Check Task

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00 . Memory (MB): peak = 2077.234 ; gain = 0.000 ; free physical = 136 ; free virtual = 2293

Ending Logic Optimization Task | Checksum: 139e370ad

Time (s): cpu = 00:00:00.13 ; elapsed = 00:00:00.22 . Memory (MB): peak = 2077.234 ; gain = 0.000 ; free physical = 136 ; free virtual = 2293

Starting Power Optimization Task

INFO: [Pwropt 34-132] Skipping clock gating for clocks with a period < 2.00 ns.

Ending Power Optimization Task | Checksum: 139e370ad

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.02 . Memory (MB): peak = 2077.234 ; gain = 0.000 ; free physical = 136 ; free virtual = 2293

Starting Final Cleanup Task

Ending Final Cleanup Task | Checksum: 139e370ad

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2077.234 ; gain = 0.000 ; free physical = 136 ; free virtual = 2293

Starting Netlist Obfuscation Task

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2077.234 ; gain = 0.000 ; free physical = 136 ; free virtual = 2293

Ending Netlist Obfuscation Task | Checksum: 139e370ad

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2077.234 ; gain = 0.000 ; free physical = 136 ; free virtual = 2293

INFO: [Common 17-83] Releasing license: Implementation

27 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.

opt\_design completed successfully

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2077.234 ; gain = 0.000 ; free physical = 136 ; free virtual = 2293

INFO: [Timing 38-480] Writing timing data to binary archive.

Writing placer database...

Writing XDEF routing.

Writing XDEF routing logical nets.

Writing XDEF routing special nets.

Write XDEF Complete: Time (s): cpu = 00:00:00.02 ; elapsed = 00:00:00.01 . Memory (MB): peak = 2109.250 ; gain = 0.000 ; free physical = 134 ; free virtual = 2291

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2109.250 ; gain = 0.000 ; free physical = 134 ; free virtual = 2291

INFO: [Common 17-1381] The checkpoint '/home/jinson/vivado/Lab10\_Wave/Lab10\_Wave.runs/impl\_1/Lab10\_Wave\_opt.dcp' has been generated.

INFO: [runtcl-4] Executing : report\_drc -file Lab10\_Wave\_drc\_opted.rpt -pb Lab10\_Wave\_drc\_opted.pb -rpx Lab10\_Wave\_drc\_opted.rpx

Command: report\_drc -file Lab10\_Wave\_drc\_opted.rpt -pb Lab10\_Wave\_drc\_opted.pb -rpx Lab10\_Wave\_drc\_opted.rpx

INFO: [IP\_Flow 19-234] Refreshing IP repositories

INFO: [IP\_Flow 19-1704] No user IP repositories specified

INFO: [IP\_Flow 19-2313] Loaded Vivado IP repository '/tools/Xilinx/Vivado/2018.3/data/ip'.

INFO: [DRC 23-27] Running DRC with 4 threads

INFO: [Coretcl 2-168] The results of DRC are in file /home/jinson/vivado/Lab10\_Wave/Lab10\_Wave.runs/impl\_1/Lab10\_Wave\_drc\_opted.rpt.

report\_drc completed successfully

Command: place\_design

Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'

INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t'

INFO: [DRC 23-27] Running DRC with 4 threads

INFO: [Vivado\_Tcl 4-198] DRC finished with 0 Errors

INFO: [Vivado\_Tcl 4-199] Please refer to the DRC report (report\_drc) for more information.

Running DRC as a precondition to command place\_design

INFO: [DRC 23-27] Running DRC with 4 threads

INFO: [Vivado\_Tcl 4-198] DRC finished with 0 Errors

INFO: [Vivado\_Tcl 4-199] Please refer to the DRC report (report\_drc) for more information.

Starting Placer Task

INFO: [Place 30-611] Multithreading enabled for place\_design using a maximum of 4 CPUs

Phase 1 Placer Initialization

Phase 1.1 Placer Initialization Netlist Sorting

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2141.266 ; gain = 0.000 ; free physical = 122 ; free virtual = 2261

Phase 1.1 Placer Initialization Netlist Sorting | Checksum: 115f70ec8

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2141.266 ; gain = 0.000 ; free physical = 122 ; free virtual = 2261

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2141.266 ; gain = 0.000 ; free physical = 122 ; free virtual = 2261

Phase 1.2 IO Placement/ Clock Placement/ Build Placer Device

INFO: [Timing 38-35] Done setting XDC timing constraints.

Phase 1.2 IO Placement/ Clock Placement/ Build Placer Device | Checksum: e6af0fcc

Time (s): cpu = 00:00:00.59 ; elapsed = 00:00:00.41 . Memory (MB): peak = 2141.266 ; gain = 0.000 ; free physical = 107 ; free virtual = 2246

Phase 1.3 Build Placer Netlist Model

Phase 1.3 Build Placer Netlist Model | Checksum: 1332d71a2

Time (s): cpu = 00:00:00.61 ; elapsed = 00:00:00.43 . Memory (MB): peak = 2141.266 ; gain = 0.000 ; free physical = 107 ; free virtual = 2245

Phase 1.4 Constrain Clocks/Macros

Phase 1.4 Constrain Clocks/Macros | Checksum: 1332d71a2

Time (s): cpu = 00:00:00.62 ; elapsed = 00:00:00.43 . Memory (MB): peak = 2141.266 ; gain = 0.000 ; free physical = 107 ; free virtual = 2245

Phase 1 Placer Initialization | Checksum: 1332d71a2

Time (s): cpu = 00:00:00.62 ; elapsed = 00:00:00.43 . Memory (MB): peak = 2141.266 ; gain = 0.000 ; free physical = 107 ; free virtual = 2245

Phase 2 Global Placement

Phase 2.1 Floorplanning

Phase 2.1 Floorplanning | Checksum: 1332d71a2

Time (s): cpu = 00:00:00.62 ; elapsed = 00:00:00.44 . Memory (MB): peak = 2141.266 ; gain = 0.000 ; free physical = 105 ; free virtual = 2244

WARNING: [Place 46-29] place\_design is not in timing mode. Skip physical synthesis in placer

Phase 2 Global Placement | Checksum: 1c27ca26f

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.63 . Memory (MB): peak = 2161.266 ; gain = 20.000 ; free physical = 104 ; free virtual = 2233

Phase 3 Detail Placement

Phase 3.1 Commit Multi Column Macros

Phase 3.1 Commit Multi Column Macros | Checksum: 1c27ca26f

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.64 . Memory (MB): peak = 2161.266 ; gain = 20.000 ; free physical = 110 ; free virtual = 2236

Phase 3.2 Commit Most Macros & LUTRAMs

Phase 3.2 Commit Most Macros & LUTRAMs | Checksum: 132535d99

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.65 . Memory (MB): peak = 2161.266 ; gain = 20.000 ; free physical = 115 ; free virtual = 2238

Phase 3.3 Area Swap Optimization

Phase 3.3 Area Swap Optimization | Checksum: 162ea9312

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.67 . Memory (MB): peak = 2161.266 ; gain = 20.000 ; free physical = 124 ; free virtual = 2236

Phase 3.4 Pipeline Register Optimization

Phase 3.4 Pipeline Register Optimization | Checksum: 162ea9312

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.67 . Memory (MB): peak = 2161.266 ; gain = 20.000 ; free physical = 124 ; free virtual = 2236

Phase 3.5 Small Shape Detail Placement

Phase 3.5 Small Shape Detail Placement | Checksum: 1390cfaa7

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.81 . Memory (MB): peak = 2161.266 ; gain = 20.000 ; free physical = 121 ; free virtual = 2233

Phase 3.6 Re-assign LUT pins

Phase 3.6 Re-assign LUT pins | Checksum: 1390cfaa7

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.81 . Memory (MB): peak = 2161.266 ; gain = 20.000 ; free physical = 121 ; free virtual = 2233

Phase 3.7 Pipeline Register Optimization

Phase 3.7 Pipeline Register Optimization | Checksum: 1390cfaa7

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.81 . Memory (MB): peak = 2161.266 ; gain = 20.000 ; free physical = 121 ; free virtual = 2233

Phase 3 Detail Placement | Checksum: 1390cfaa7

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.81 . Memory (MB): peak = 2161.266 ; gain = 20.000 ; free physical = 121 ; free virtual = 2233

Phase 4 Post Placement Optimization and Clean-Up

Phase 4.1 Post Commit Optimization

Phase 4.1 Post Commit Optimization | Checksum: 1390cfaa7

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.81 . Memory (MB): peak = 2161.266 ; gain = 20.000 ; free physical = 121 ; free virtual = 2233

Phase 4.2 Post Placement Cleanup

Phase 4.2 Post Placement Cleanup | Checksum: 1390cfaa7

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.82 . Memory (MB): peak = 2161.266 ; gain = 20.000 ; free physical = 123 ; free virtual = 2235

Phase 4.3 Placer Reporting

Phase 4.3 Placer Reporting | Checksum: 1390cfaa7

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.82 . Memory (MB): peak = 2161.266 ; gain = 20.000 ; free physical = 123 ; free virtual = 2235

Phase 4.4 Final Placement Cleanup

Netlist sorting complete. Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.01 . Memory (MB): peak = 2161.266 ; gain = 0.000 ; free physical = 123 ; free virtual = 2235

Phase 4.4 Final Placement Cleanup | Checksum: ddb4d379

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.83 . Memory (MB): peak = 2161.266 ; gain = 20.000 ; free physical = 123 ; free virtual = 2235

Phase 4 Post Placement Optimization and Clean-Up | Checksum: ddb4d379

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.83 . Memory (MB): peak = 2161.266 ; gain = 20.000 ; free physical = 123 ; free virtual = 2235

Ending Placer Task | Checksum: c9b766d0

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.83 . Memory (MB): peak = 2161.266 ; gain = 20.000 ; free physical = 132 ; free virtual = 2244

INFO: [Common 17-83] Releasing license: Implementation

45 Infos, 1 Warnings, 0 Critical Warnings and 0 Errors encountered.

place\_design completed successfully

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2161.266 ; gain = 0.000 ; free physical = 134 ; free virtual = 2246

INFO: [Timing 38-480] Writing timing data to binary archive.

Writing placer database...

Writing XDEF routing.

Writing XDEF routing logical nets.

Writing XDEF routing special nets.

Write XDEF Complete: Time (s): cpu = 00:00:00.04 ; elapsed = 00:00:00.02 . Memory (MB): peak = 2161.266 ; gain = 0.000 ; free physical = 133 ; free virtual = 2246

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2161.266 ; gain = 0.000 ; free physical = 133 ; free virtual = 2246

INFO: [Common 17-1381] The checkpoint '/home/jinson/vivado/Lab10\_Wave/Lab10\_Wave.runs/impl\_1/Lab10\_Wave\_placed.dcp' has been generated.

INFO: [runtcl-4] Executing : report\_io -file Lab10\_Wave\_io\_placed.rpt

report\_io: Time (s): cpu = 00:00:00.09 ; elapsed = 00:00:00.12 . Memory (MB): peak = 2161.266 ; gain = 0.000 ; free physical = 127 ; free virtual = 2239

INFO: [runtcl-4] Executing : report\_utilization -file Lab10\_Wave\_utilization\_placed.rpt -pb Lab10\_Wave\_utilization\_placed.pb

INFO: [runtcl-4] Executing : report\_control\_sets -verbose -file Lab10\_Wave\_control\_sets\_placed.rpt

report\_control\_sets: Time (s): cpu = 00:00:00.06 ; elapsed = 00:00:00.08 . Memory (MB): peak = 2161.266 ; gain = 0.000 ; free physical = 133 ; free virtual = 2245

Command: route\_design

Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'

INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t'

Running DRC as a precondition to command route\_design

INFO: [DRC 23-27] Running DRC with 4 threads

INFO: [Vivado\_Tcl 4-198] DRC finished with 0 Errors

INFO: [Vivado\_Tcl 4-199] Please refer to the DRC report (report\_drc) for more information.

Starting Routing Task

INFO: [Route 35-254] Multithreading enabled for route\_design using a maximum of 4 CPUs

Checksum: PlaceDB: 7f842d92 ConstDB: 0 ShapeSum: 4a33393e RouteDB: 0

Phase 1 Build RT Design

Phase 1 Build RT Design | Checksum: 9c8643eb

Time (s): cpu = 00:00:22 ; elapsed = 00:00:17 . Memory (MB): peak = 2299.316 ; gain = 138.051 ; free physical = 106 ; free virtual = 2100

Post Restoration Checksum: NetGraph: 5ab4fb41 NumContArr: 41d148aa Constraints: 0 Timing: 0

Phase 2 Router Initialization

INFO: [Route 35-64] No timing constraints were detected. The router will operate in resource-optimization mode.

Phase 2.1 Fix Topology Constraints

Phase 2.1 Fix Topology Constraints | Checksum: 9c8643eb

Time (s): cpu = 00:00:22 ; elapsed = 00:00:17 . Memory (MB): peak = 2306.312 ; gain = 145.047 ; free physical = 107 ; free virtual = 2085

Phase 2.2 Pre Route Cleanup

Phase 2.2 Pre Route Cleanup | Checksum: 9c8643eb

Time (s): cpu = 00:00:22 ; elapsed = 00:00:17 . Memory (MB): peak = 2306.312 ; gain = 145.047 ; free physical = 107 ; free virtual = 2085

Number of Nodes with overlaps = 0

Phase 2 Router Initialization | Checksum: a133899e

Time (s): cpu = 00:00:22 ; elapsed = 00:00:18 . Memory (MB): peak = 2314.578 ; gain = 153.312 ; free physical = 105 ; free virtual = 2076

Phase 3 Initial Routing

Phase 3 Initial Routing | Checksum: e2ce5854

Time (s): cpu = 00:00:22 ; elapsed = 00:00:18 . Memory (MB): peak = 2321.434 ; gain = 160.168 ; free physical = 121 ; free virtual = 2077

Phase 4 Rip-up And Reroute

Phase 4.1 Global Iteration 0

Number of Nodes with overlaps = 2

Number of Nodes with overlaps = 0

Phase 4.1 Global Iteration 0 | Checksum: a7ab51a3

Time (s): cpu = 00:00:22 ; elapsed = 00:00:18 . Memory (MB): peak = 2321.434 ; gain = 160.168 ; free physical = 121 ; free virtual = 2077

Phase 4 Rip-up And Reroute | Checksum: a7ab51a3

Time (s): cpu = 00:00:22 ; elapsed = 00:00:18 . Memory (MB): peak = 2321.434 ; gain = 160.168 ; free physical = 121 ; free virtual = 2077

Phase 5 Delay and Skew Optimization

Phase 5 Delay and Skew Optimization | Checksum: a7ab51a3

Time (s): cpu = 00:00:22 ; elapsed = 00:00:18 . Memory (MB): peak = 2321.434 ; gain = 160.168 ; free physical = 121 ; free virtual = 2077

Phase 6 Post Hold Fix

Phase 6.1 Hold Fix Iter

Phase 6.1 Hold Fix Iter | Checksum: a7ab51a3

Time (s): cpu = 00:00:22 ; elapsed = 00:00:18 . Memory (MB): peak = 2321.434 ; gain = 160.168 ; free physical = 121 ; free virtual = 2077

Phase 6 Post Hold Fix | Checksum: a7ab51a3

Time (s): cpu = 00:00:22 ; elapsed = 00:00:18 . Memory (MB): peak = 2321.434 ; gain = 160.168 ; free physical = 121 ; free virtual = 2077

Phase 7 Route finalize

Router Utilization Summary

Global Vertical Routing Utilization = 0.00596248 %

Global Horizontal Routing Utilization = 0.00227337 %

Routable Net Status\*

\*Does not include unroutable nets such as driverless and loadless.

Run report\_route\_status for detailed report.

Number of Failed Nets = 0

Number of Unrouted Nets = 0

Number of Partially Routed Nets = 0

Number of Node Overlaps = 0

Congestion Report

North Dir 1x1 Area, Max Cong = 17.1171%, No Congested Regions.

South Dir 1x1 Area, Max Cong = 14.4144%, No Congested Regions.

East Dir 1x1 Area, Max Cong = 4.41176%, No Congested Regions.

West Dir 1x1 Area, Max Cong = 5.88235%, No Congested Regions.

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Reporting congestion hotspots

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Direction: North

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Congested clusters found at Level 0

Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0

Direction: South

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Congested clusters found at Level 0

Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0

Direction: East

----------------

Congested clusters found at Level 0

Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0

Direction: West

----------------

Congested clusters found at Level 0

Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0

Phase 7 Route finalize | Checksum: a7ab51a3

Time (s): cpu = 00:00:22 ; elapsed = 00:00:18 . Memory (MB): peak = 2321.434 ; gain = 160.168 ; free physical = 121 ; free virtual = 2077

Phase 8 Verifying routed nets

Verification completed successfully

Phase 8 Verifying routed nets | Checksum: a7ab51a3

Time (s): cpu = 00:00:22 ; elapsed = 00:00:18 . Memory (MB): peak = 2321.434 ; gain = 160.168 ; free physical = 120 ; free virtual = 2076

Phase 9 Depositing Routes

Phase 9 Depositing Routes | Checksum: 12722b941

Time (s): cpu = 00:00:22 ; elapsed = 00:00:18 . Memory (MB): peak = 2321.434 ; gain = 160.168 ; free physical = 121 ; free virtual = 2077

INFO: [Route 35-16] Router Completed Successfully

Time (s): cpu = 00:00:22 ; elapsed = 00:00:18 . Memory (MB): peak = 2321.434 ; gain = 160.168 ; free physical = 138 ; free virtual = 2095

Routing Is Done.

INFO: [Common 17-83] Releasing license: Implementation

58 Infos, 1 Warnings, 0 Critical Warnings and 0 Errors encountered.

route\_design completed successfully

route\_design: Time (s): cpu = 00:00:24 ; elapsed = 00:00:19 . Memory (MB): peak = 2321.434 ; gain = 160.168 ; free physical = 138 ; free virtual = 2095

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2321.434 ; gain = 0.000 ; free physical = 138 ; free virtual = 2095

INFO: [Timing 38-480] Writing timing data to binary archive.

Writing placer database...

Writing XDEF routing.

Writing XDEF routing logical nets.

Writing XDEF routing special nets.

Write XDEF Complete: Time (s): cpu = 00:00:00.04 ; elapsed = 00:00:00.02 . Memory (MB): peak = 2321.434 ; gain = 0.000 ; free physical = 138 ; free virtual = 2095

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2321.434 ; gain = 0.000 ; free physical = 138 ; free virtual = 2095

INFO: [Common 17-1381] The checkpoint '/home/jinson/vivado/Lab10\_Wave/Lab10\_Wave.runs/impl\_1/Lab10\_Wave\_routed.dcp' has been generated.

INFO: [runtcl-4] Executing : report\_drc -file Lab10\_Wave\_drc\_routed.rpt -pb Lab10\_Wave\_drc\_routed.pb -rpx Lab10\_Wave\_drc\_routed.rpx

Command: report\_drc -file Lab10\_Wave\_drc\_routed.rpt -pb Lab10\_Wave\_drc\_routed.pb -rpx Lab10\_Wave\_drc\_routed.rpx

INFO: [IP\_Flow 19-1839] IP Catalog is up to date.

INFO: [DRC 23-27] Running DRC with 4 threads

INFO: [Coretcl 2-168] The results of DRC are in file /home/jinson/vivado/Lab10\_Wave/Lab10\_Wave.runs/impl\_1/Lab10\_Wave\_drc\_routed.rpt.

report\_drc completed successfully

INFO: [runtcl-4] Executing : report\_methodology -file Lab10\_Wave\_methodology\_drc\_routed.rpt -pb Lab10\_Wave\_methodology\_drc\_routed.pb -rpx Lab10\_Wave\_methodology\_drc\_routed.rpx

Command: report\_methodology -file Lab10\_Wave\_methodology\_drc\_routed.rpt -pb Lab10\_Wave\_methodology\_drc\_routed.pb -rpx Lab10\_Wave\_methodology\_drc\_routed.rpx

INFO: [Timing 38-35] Done setting XDC timing constraints.

INFO: [DRC 23-133] Running Methodology with 4 threads

INFO: [Coretcl 2-1520] The results of Report Methodology are in file /home/jinson/vivado/Lab10\_Wave/Lab10\_Wave.runs/impl\_1/Lab10\_Wave\_methodology\_drc\_routed.rpt.

report\_methodology completed successfully

INFO: [runtcl-4] Executing : report\_power -file Lab10\_Wave\_power\_routed.rpt -pb Lab10\_Wave\_power\_summary\_routed.pb -rpx Lab10\_Wave\_power\_routed.rpx

Command: report\_power -file Lab10\_Wave\_power\_routed.rpt -pb Lab10\_Wave\_power\_summary\_routed.pb -rpx Lab10\_Wave\_power\_routed.rpx

WARNING: [Power 33-232] No user defined clocks were found in the design!

Resolution: Please specify clocks using create\_clock/create\_generated\_clock for sequential elements. For pure combinatorial circuits, please specify a virtual clock, otherwise the vectorless estimation might be inaccurate

INFO: [Timing 38-35] Done setting XDC timing constraints.

Running Vector-less Activity Propagation...

Finished Running Vector-less Activity Propagation

70 Infos, 2 Warnings, 0 Critical Warnings and 0 Errors encountered.

report\_power completed successfully

INFO: [runtcl-4] Executing : report\_route\_status -file Lab10\_Wave\_route\_status.rpt -pb Lab10\_Wave\_route\_status.pb

INFO: [runtcl-4] Executing : report\_timing\_summary -max\_paths 10 -file Lab10\_Wave\_timing\_summary\_routed.rpt -pb Lab10\_Wave\_timing\_summary\_routed.pb -rpx Lab10\_Wave\_timing\_summary\_routed.rpx -warn\_on\_violation

INFO: [Timing 38-91] UpdateTimingParams: Speed grade: -1, Delay Type: min\_max.

INFO: [Timing 38-191] Multithreading enabled for timing update using a maximum of 4 CPUs

WARNING: [Timing 38-313] There are no user specified timing constraints. Timing constraints are needed for proper timing analysis.

INFO: [runtcl-4] Executing : report\_incremental\_reuse -file Lab10\_Wave\_incremental\_reuse\_routed.rpt

INFO: [Vivado\_Tcl 4-1062] Incremental flow is disabled. No incremental reuse Info to report.

INFO: [runtcl-4] Executing : report\_clock\_utilization -file Lab10\_Wave\_clock\_utilization\_routed.rpt

INFO: [runtcl-4] Executing : report\_bus\_skew -warn\_on\_violation -file Lab10\_Wave\_bus\_skew\_routed.rpt -pb Lab10\_Wave\_bus\_skew\_routed.pb -rpx Lab10\_Wave\_bus\_skew\_routed.rpx

INFO: [Timing 38-91] UpdateTimingParams: Speed grade: -1, Delay Type: min\_max.

INFO: [Timing 38-191] Multithreading enabled for timing update using a maximum of 4 CPUs

INFO: [Common 17-206] Exiting Vivado at Thu May 23 20:12:47 2019...

\*\*\* Running vivado

with args -log Lab10\_Wave.vdi -applog -m64 -product Vivado -messageDb vivado.pb -mode batch -source Lab10\_Wave.tcl -notrace

\*\*\*\*\*\* Vivado v2018.3 (64-bit)

\*\*\*\* SW Build 2405991 on Thu Dec 6 23:36:41 MST 2018

\*\*\*\* IP Build 2404404 on Fri Dec 7 01:43:56 MST 2018

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CRITICAL WARNING: [Common 17-741] No write access right to the local Tcl store at '/home/jinson/.Xilinx/Vivado/2018.3/XilinxTclStore'. XilinxTclStore is reverted to the installation area. If you want to use local Tcl Store, please change the access right and relaunch Vivado.

source Lab10\_Wave.tcl -notrace

Command: open\_checkpoint Lab10\_Wave\_routed.dcp

Starting open\_checkpoint Task

Time (s): cpu = 00:00:00.05 ; elapsed = 00:00:00.07 . Memory (MB): peak = 1378.266 ; gain = 0.000 ; free physical = 1052 ; free virtual = 3023

INFO: [Netlist 29-17] Analyzing 7 Unisim elements for replacement

INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds

INFO: [Project 1-479] Netlist was created with Vivado 2018.3

INFO: [Device 21-403] Loading part xc7a100tcsg324-1

INFO: [Project 1-570] Preparing netlist for logic optimization

INFO: [Timing 38-478] Restoring timing data from binary archive.

INFO: [Timing 38-479] Binary timing data restore complete.

INFO: [Project 1-856] Restoring constraints from binary archive.

INFO: [Project 1-853] Binary constraint restore complete.

Reading XDEF placement.

Reading placer database...

Reading XDEF routing.

Read XDEF File: Time (s): cpu = 00:00:00.06 ; elapsed = 00:00:00.13 . Memory (MB): peak = 2004.262 ; gain = 0.000 ; free physical = 331 ; free virtual = 2308

Restored from archive | CPU: 0.130000 secs | Memory: 1.066521 MB |

Finished XDEF File Restore: Time (s): cpu = 00:00:00.06 ; elapsed = 00:00:00.14 . Memory (MB): peak = 2004.262 ; gain = 0.000 ; free physical = 331 ; free virtual = 2308

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2004.262 ; gain = 0.000 ; free physical = 332 ; free virtual = 2309

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

INFO: [Project 1-604] Checkpoint was created with Vivado v2018.3 (64-bit) build 2405991

open\_checkpoint: Time (s): cpu = 00:00:09 ; elapsed = 00:00:10 . Memory (MB): peak = 2004.262 ; gain = 625.996 ; free physical = 331 ; free virtual = 2308

Command: write\_bitstream -force Lab10\_Wave.bit

Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'

INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t'

Running DRC as a precondition to command write\_bitstream

INFO: [IP\_Flow 19-234] Refreshing IP repositories

INFO: [IP\_Flow 19-1704] No user IP repositories specified

INFO: [IP\_Flow 19-2313] Loaded Vivado IP repository '/tools/Xilinx/Vivado/2018.3/data/ip'.

INFO: [DRC 23-27] Running DRC with 4 threads

WARNING: [DRC CFGBVS-1] Missing CFGBVS and CONFIG\_VOLTAGE Design Properties: Neither the CFGBVS nor CONFIG\_VOLTAGE voltage property is set in the current\_design. Configuration bank voltage select (CFGBVS) must be set to VCCO or GND, and CONFIG\_VOLTAGE must be set to the correct configuration voltage, in order to determine the I/O voltage support for the pins in bank 0. It is suggested to specify these either using the 'Edit Device Properties' function in the GUI or directly in the XDC file using the following syntax:

set\_property CFGBVS value1 [current\_design]

#where value1 is either VCCO or GND

set\_property CONFIG\_VOLTAGE value2 [current\_design]

#where value2 is the voltage provided to configuration bank 0

Refer to the device configuration user guide for more information.

INFO: [Vivado 12-3199] DRC finished with 0 Errors, 1 Warnings

INFO: [Vivado 12-3200] Please refer to the DRC report (report\_drc) for more information.

INFO: [Designutils 20-2272] Running write\_bitstream with 4 threads.

Loading data files...

Loading site data...

Loading route data...

Processing options...

Creating bitmap...

Creating bitstream...

Bitstream compression saved 27611712 bits.

Writing bitstream ./Lab10\_Wave.bit...

INFO: [Vivado 12-1842] Bitgen Completed Successfully.

INFO: [Project 1-120] WebTalk data collection is mandatory when using a WebPACK part without a full Vivado license. To see the specific WebTalk data collected for your design, open the usage\_statistics\_webtalk.html or usage\_statistics\_webtalk.xml file in the implementation directory.

CRITICAL WARNING: [Common 17-570] Unable to write the webtalk settings file. Please check that the appropriate environment variable (APPDATA or HOME) is properly set.

CRITICAL WARNING: [Common 17-570] Unable to write the webtalk settings file. Please check that the appropriate environment variable (APPDATA or HOME) is properly set.

INFO: [Common 17-83] Releasing license: Implementation

22 Infos, 1 Warnings, 2 Critical Warnings and 0 Errors encountered.

write\_bitstream completed successfully

write\_bitstream: Time (s): cpu = 00:00:08 ; elapsed = 00:00:09 . Memory (MB): peak = 2446.098 ; gain = 441.836 ; free physical = 424 ; free virtual = 2225

INFO: [Common 17-206] Exiting Vivado at Thu May 23 20:13:27 2019...