\*\*\* Running vivado

with args -log Lab06\_clk\_odd.vdi -applog -m64 -product Vivado -messageDb vivado.pb -mode batch -source Lab06\_clk\_odd.tcl -notrace

\*\*\*\*\*\* Vivado v2018.3 (64-bit)

\*\*\*\* SW Build 2405991 on Thu Dec 6 23:36:41 MST 2018

\*\*\*\* IP Build 2404404 on Fri Dec 7 01:43:56 MST 2018

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CRITICAL WARNING: [Common 17-741] No write access right to the local Tcl store at '/home/jinson/.Xilinx/Vivado/2018.3/XilinxTclStore'. XilinxTclStore is reverted to the installation area. If you want to use local Tcl Store, please change the access right and relaunch Vivado.

source Lab06\_clk\_odd.tcl -notrace

Command: link\_design -top Lab06\_clk\_odd -part xc7a100tcsg324-1

Design is defaulting to srcset: sources\_1

Design is defaulting to constrset: constrs\_1

INFO: [Project 1-479] Netlist was created with Vivado 2018.3

INFO: [Device 21-403] Loading part xc7a100tcsg324-1

INFO: [Project 1-570] Preparing netlist for logic optimization

Parsing XDC File [/home/jinson/vivado/Lab06\_clk\_odd/Lab06\_clk\_odd.srcs/constrs\_1/new/Lab06\_clk\_odd.xdc]

Finished Parsing XDC File [/home/jinson/vivado/Lab06\_clk\_odd/Lab06\_clk\_odd.srcs/constrs\_1/new/Lab06\_clk\_odd.xdc]

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1513.602 ; gain = 0.000 ; free physical = 1461 ; free virtual = 3538

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

5 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.

link\_design completed successfully

Command: opt\_design

Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'

INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t'

Running DRC as a precondition to command opt\_design

Starting DRC Task

INFO: [DRC 23-27] Running DRC with 4 threads

INFO: [Project 1-461] DRC finished with 0 Errors

INFO: [Project 1-462] Please refer to the DRC report (report\_drc) for more information.

Time (s): cpu = 00:00:00.84 ; elapsed = 00:00:00.93 . Memory (MB): peak = 1564.617 ; gain = 47.016 ; free physical = 1454 ; free virtual = 3531

Starting Cache Timing Information Task

INFO: [Timing 38-35] Done setting XDC timing constraints.

Ending Cache Timing Information Task | Checksum: 19267095c

Time (s): cpu = 00:00:05 ; elapsed = 00:00:06 . Memory (MB): peak = 1993.117 ; gain = 428.500 ; free physical = 1075 ; free virtual = 3152

Starting Logic Optimization Task

Phase 1 Retarget

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

INFO: [Opt 31-49] Retargeted 0 cell(s).

Phase 1 Retarget | Checksum: f5388059

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.02 . Memory (MB): peak = 2070.117 ; gain = 0.000 ; free physical = 1006 ; free virtual = 3083

INFO: [Opt 31-389] Phase Retarget created 6 cells and removed 6 cells

Phase 2 Constant propagation

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

Phase 2 Constant propagation | Checksum: f5388059

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.02 . Memory (MB): peak = 2070.117 ; gain = 0.000 ; free physical = 1006 ; free virtual = 3083

INFO: [Opt 31-389] Phase Constant propagation created 0 cells and removed 0 cells

Phase 3 Sweep

Phase 3 Sweep | Checksum: f5388059

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.02 . Memory (MB): peak = 2070.117 ; gain = 0.000 ; free physical = 1006 ; free virtual = 3083

INFO: [Opt 31-389] Phase Sweep created 0 cells and removed 0 cells

Phase 4 BUFG optimization

Phase 4 BUFG optimization | Checksum: f5388059

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.02 . Memory (MB): peak = 2070.117 ; gain = 0.000 ; free physical = 1006 ; free virtual = 3083

INFO: [Opt 31-662] Phase BUFG optimization created 0 cells of which 0 are BUFGs and removed 0 cells.

Phase 5 Shift Register Optimization

Phase 5 Shift Register Optimization | Checksum: f5388059

Time (s): cpu = 00:00:00.03 ; elapsed = 00:00:00.04 . Memory (MB): peak = 2070.117 ; gain = 0.000 ; free physical = 1006 ; free virtual = 3083

INFO: [Opt 31-389] Phase Shift Register Optimization created 0 cells and removed 0 cells

Phase 6 Post Processing Netlist

Phase 6 Post Processing Netlist | Checksum: f5388059

Time (s): cpu = 00:00:00.03 ; elapsed = 00:00:00.04 . Memory (MB): peak = 2070.117 ; gain = 0.000 ; free physical = 1006 ; free virtual = 3083

INFO: [Opt 31-389] Phase Post Processing Netlist created 0 cells and removed 0 cells

Opt\_design Change Summary

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-------------------------------------------------------------------------------------------------------------------------

| Phase | #Cells created | #Cells Removed | #Constrained objects preventing optimizations |

-------------------------------------------------------------------------------------------------------------------------

| Retarget | 6 | 6 | 0 |

| Constant propagation | 0 | 0 | 0 |

| Sweep | 0 | 0 | 0 |

| BUFG optimization | 0 | 0 | 0 |

| Shift Register Optimization | 0 | 0 | 0 |

| Post Processing Netlist | 0 | 0 | 0 |

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Starting Connectivity Check Task

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2070.117 ; gain = 0.000 ; free physical = 1006 ; free virtual = 3083

Ending Logic Optimization Task | Checksum: f5388059

Time (s): cpu = 00:00:00.03 ; elapsed = 00:00:00.04 . Memory (MB): peak = 2070.117 ; gain = 0.000 ; free physical = 1006 ; free virtual = 3083

Starting Power Optimization Task

INFO: [Pwropt 34-132] Skipping clock gating for clocks with a period < 2.00 ns.

Ending Power Optimization Task | Checksum: f5388059

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.02 . Memory (MB): peak = 2070.117 ; gain = 0.000 ; free physical = 1006 ; free virtual = 3083

Starting Final Cleanup Task

Ending Final Cleanup Task | Checksum: f5388059

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2070.117 ; gain = 0.000 ; free physical = 1006 ; free virtual = 3083

Starting Netlist Obfuscation Task

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2070.117 ; gain = 0.000 ; free physical = 1006 ; free virtual = 3083

Ending Netlist Obfuscation Task | Checksum: f5388059

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2070.117 ; gain = 0.000 ; free physical = 1006 ; free virtual = 3083

INFO: [Common 17-83] Releasing license: Implementation

21 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.

opt\_design completed successfully

opt\_design: Time (s): cpu = 00:00:07 ; elapsed = 00:00:07 . Memory (MB): peak = 2070.117 ; gain = 552.516 ; free physical = 1006 ; free virtual = 3083

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2070.117 ; gain = 0.000 ; free physical = 1006 ; free virtual = 3083

INFO: [Timing 38-480] Writing timing data to binary archive.

Writing placer database...

Writing XDEF routing.

Writing XDEF routing logical nets.

Writing XDEF routing special nets.

Write XDEF Complete: Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.01 . Memory (MB): peak = 2102.133 ; gain = 0.000 ; free physical = 1004 ; free virtual = 3082

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2102.133 ; gain = 0.000 ; free physical = 1003 ; free virtual = 3081

INFO: [Common 17-1381] The checkpoint '/home/jinson/vivado/Lab06\_clk\_odd/Lab06\_clk\_odd.runs/impl\_1/Lab06\_clk\_odd\_opt.dcp' has been generated.

INFO: [runtcl-4] Executing : report\_drc -file Lab06\_clk\_odd\_drc\_opted.rpt -pb Lab06\_clk\_odd\_drc\_opted.pb -rpx Lab06\_clk\_odd\_drc\_opted.rpx

Command: report\_drc -file Lab06\_clk\_odd\_drc\_opted.rpt -pb Lab06\_clk\_odd\_drc\_opted.pb -rpx Lab06\_clk\_odd\_drc\_opted.rpx

INFO: [IP\_Flow 19-234] Refreshing IP repositories

INFO: [IP\_Flow 19-1704] No user IP repositories specified

INFO: [IP\_Flow 19-2313] Loaded Vivado IP repository '/tools/Xilinx/Vivado/2018.3/data/ip'.

INFO: [DRC 23-27] Running DRC with 4 threads

INFO: [Coretcl 2-168] The results of DRC are in file /home/jinson/vivado/Lab06\_clk\_odd/Lab06\_clk\_odd.runs/impl\_1/Lab06\_clk\_odd\_drc\_opted.rpt.

report\_drc completed successfully

Command: place\_design

Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'

INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t'

INFO: [DRC 23-27] Running DRC with 4 threads

INFO: [Vivado\_Tcl 4-198] DRC finished with 0 Errors

INFO: [Vivado\_Tcl 4-199] Please refer to the DRC report (report\_drc) for more information.

Running DRC as a precondition to command place\_design

INFO: [DRC 23-27] Running DRC with 4 threads

INFO: [Vivado\_Tcl 4-198] DRC finished with 0 Errors

INFO: [Vivado\_Tcl 4-199] Please refer to the DRC report (report\_drc) for more information.

Starting Placer Task

INFO: [Place 30-611] Multithreading enabled for place\_design using a maximum of 4 CPUs

Phase 1 Placer Initialization

Phase 1.1 Placer Initialization Netlist Sorting

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2110.137 ; gain = 0.000 ; free physical = 964 ; free virtual = 3041

Phase 1.1 Placer Initialization Netlist Sorting | Checksum: acdec706

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.01 . Memory (MB): peak = 2110.137 ; gain = 0.000 ; free physical = 964 ; free virtual = 3041

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2110.137 ; gain = 0.000 ; free physical = 964 ; free virtual = 3041

Phase 1.2 IO Placement/ Clock Placement/ Build Placer Device

INFO: [Timing 38-35] Done setting XDC timing constraints.

Phase 1.2 IO Placement/ Clock Placement/ Build Placer Device | Checksum: acdec706

Time (s): cpu = 00:00:00.39 ; elapsed = 00:00:00.36 . Memory (MB): peak = 2119.133 ; gain = 8.996 ; free physical = 952 ; free virtual = 3030

Phase 1.3 Build Placer Netlist Model

Phase 1.3 Build Placer Netlist Model | Checksum: fa66cd67

Time (s): cpu = 00:00:00.40 ; elapsed = 00:00:00.38 . Memory (MB): peak = 2119.133 ; gain = 8.996 ; free physical = 952 ; free virtual = 3030

Phase 1.4 Constrain Clocks/Macros

Phase 1.4 Constrain Clocks/Macros | Checksum: fa66cd67

Time (s): cpu = 00:00:00.40 ; elapsed = 00:00:00.38 . Memory (MB): peak = 2119.133 ; gain = 8.996 ; free physical = 952 ; free virtual = 3030

Phase 1 Placer Initialization | Checksum: fa66cd67

Time (s): cpu = 00:00:00.40 ; elapsed = 00:00:00.38 . Memory (MB): peak = 2119.133 ; gain = 8.996 ; free physical = 952 ; free virtual = 3030

Phase 2 Global Placement

Phase 2.1 Floorplanning

Phase 2.1 Floorplanning | Checksum: fa66cd67

Time (s): cpu = 00:00:00.40 ; elapsed = 00:00:00.38 . Memory (MB): peak = 2119.133 ; gain = 8.996 ; free physical = 951 ; free virtual = 3028

WARNING: [Place 46-29] place\_design is not in timing mode. Skip physical synthesis in placer

Phase 2 Global Placement | Checksum: 133d900d8

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.74 . Memory (MB): peak = 2153.145 ; gain = 43.008 ; free physical = 940 ; free virtual = 3018

Phase 3 Detail Placement

Phase 3.1 Commit Multi Column Macros

Phase 3.1 Commit Multi Column Macros | Checksum: 133d900d8

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.75 . Memory (MB): peak = 2153.145 ; gain = 43.008 ; free physical = 940 ; free virtual = 3018

Phase 3.2 Commit Most Macros & LUTRAMs

Phase 3.2 Commit Most Macros & LUTRAMs | Checksum: 18b1f26b4

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.76 . Memory (MB): peak = 2153.145 ; gain = 43.008 ; free physical = 940 ; free virtual = 3018

Phase 3.3 Area Swap Optimization

Phase 3.3 Area Swap Optimization | Checksum: 16eccca93

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.76 . Memory (MB): peak = 2153.145 ; gain = 43.008 ; free physical = 939 ; free virtual = 3017

Phase 3.4 Pipeline Register Optimization

Phase 3.4 Pipeline Register Optimization | Checksum: 16eccca93

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.76 . Memory (MB): peak = 2153.145 ; gain = 43.008 ; free physical = 939 ; free virtual = 3017

Phase 3.5 Small Shape Detail Placement

Phase 3.5 Small Shape Detail Placement | Checksum: 10b3e42d8

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.88 . Memory (MB): peak = 2159.523 ; gain = 49.387 ; free physical = 937 ; free virtual = 3015

Phase 3.6 Re-assign LUT pins

Phase 3.6 Re-assign LUT pins | Checksum: 10b3e42d8

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.88 . Memory (MB): peak = 2159.523 ; gain = 49.387 ; free physical = 937 ; free virtual = 3015

Phase 3.7 Pipeline Register Optimization

Phase 3.7 Pipeline Register Optimization | Checksum: 10b3e42d8

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.88 . Memory (MB): peak = 2159.523 ; gain = 49.387 ; free physical = 937 ; free virtual = 3015

Phase 3 Detail Placement | Checksum: 10b3e42d8

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.88 . Memory (MB): peak = 2159.523 ; gain = 49.387 ; free physical = 937 ; free virtual = 3015

Phase 4 Post Placement Optimization and Clean-Up

Phase 4.1 Post Commit Optimization

Phase 4.1 Post Commit Optimization | Checksum: 10b3e42d8

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.89 . Memory (MB): peak = 2159.523 ; gain = 49.387 ; free physical = 937 ; free virtual = 3015

Phase 4.2 Post Placement Cleanup

Phase 4.2 Post Placement Cleanup | Checksum: 10b3e42d8

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.89 . Memory (MB): peak = 2159.523 ; gain = 49.387 ; free physical = 939 ; free virtual = 3017

Phase 4.3 Placer Reporting

Phase 4.3 Placer Reporting | Checksum: 10b3e42d8

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.89 . Memory (MB): peak = 2159.523 ; gain = 49.387 ; free physical = 939 ; free virtual = 3017

Phase 4.4 Final Placement Cleanup

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2159.523 ; gain = 0.000 ; free physical = 939 ; free virtual = 3017

Phase 4.4 Final Placement Cleanup | Checksum: 10b3e42d8

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.89 . Memory (MB): peak = 2159.523 ; gain = 49.387 ; free physical = 939 ; free virtual = 3017

Phase 4 Post Placement Optimization and Clean-Up | Checksum: 10b3e42d8

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.89 . Memory (MB): peak = 2159.523 ; gain = 49.387 ; free physical = 939 ; free virtual = 3017

Ending Placer Task | Checksum: 3debcbe4

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.90 . Memory (MB): peak = 2159.523 ; gain = 49.387 ; free physical = 948 ; free virtual = 3026

INFO: [Common 17-83] Releasing license: Implementation

39 Infos, 1 Warnings, 0 Critical Warnings and 0 Errors encountered.

place\_design completed successfully

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2159.523 ; gain = 0.000 ; free physical = 950 ; free virtual = 3028

INFO: [Timing 38-480] Writing timing data to binary archive.

Writing placer database...

Writing XDEF routing.

Writing XDEF routing logical nets.

Writing XDEF routing special nets.

Write XDEF Complete: Time (s): cpu = 00:00:00.02 ; elapsed = 00:00:00.01 . Memory (MB): peak = 2159.523 ; gain = 0.000 ; free physical = 949 ; free virtual = 3028

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2159.523 ; gain = 0.000 ; free physical = 948 ; free virtual = 3028

INFO: [Common 17-1381] The checkpoint '/home/jinson/vivado/Lab06\_clk\_odd/Lab06\_clk\_odd.runs/impl\_1/Lab06\_clk\_odd\_placed.dcp' has been generated.

INFO: [runtcl-4] Executing : report\_io -file Lab06\_clk\_odd\_io\_placed.rpt

report\_io: Time (s): cpu = 00:00:00.10 ; elapsed = 00:00:00.13 . Memory (MB): peak = 2159.523 ; gain = 0.000 ; free physical = 936 ; free virtual = 3015

INFO: [runtcl-4] Executing : report\_utilization -file Lab06\_clk\_odd\_utilization\_placed.rpt -pb Lab06\_clk\_odd\_utilization\_placed.pb

INFO: [runtcl-4] Executing : report\_control\_sets -verbose -file Lab06\_clk\_odd\_control\_sets\_placed.rpt

report\_control\_sets: Time (s): cpu = 00:00:00.04 ; elapsed = 00:00:00.08 . Memory (MB): peak = 2159.523 ; gain = 0.000 ; free physical = 944 ; free virtual = 3022

Command: route\_design

Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'

INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t'

Running DRC as a precondition to command route\_design

INFO: [DRC 23-27] Running DRC with 4 threads

INFO: [Vivado\_Tcl 4-198] DRC finished with 0 Errors

INFO: [Vivado\_Tcl 4-199] Please refer to the DRC report (report\_drc) for more information.

Starting Routing Task

INFO: [Route 35-254] Multithreading enabled for route\_design using a maximum of 4 CPUs

Checksum: PlaceDB: 31271f55 ConstDB: 0 ShapeSum: cc4ac8f RouteDB: 0

Phase 1 Build RT Design

Phase 1 Build RT Design | Checksum: b71a21d0

Time (s): cpu = 00:00:21 ; elapsed = 00:00:17 . Memory (MB): peak = 2299.199 ; gain = 139.676 ; free physical = 797 ; free virtual = 2877

Post Restoration Checksum: NetGraph: 1b197b4 NumContArr: b5688a1c Constraints: 0 Timing: 0

Phase 2 Router Initialization

INFO: [Route 35-64] No timing constraints were detected. The router will operate in resource-optimization mode.

Phase 2.1 Fix Topology Constraints

Phase 2.1 Fix Topology Constraints | Checksum: b71a21d0

Time (s): cpu = 00:00:21 ; elapsed = 00:00:17 . Memory (MB): peak = 2306.195 ; gain = 146.672 ; free physical = 781 ; free virtual = 2861

Phase 2.2 Pre Route Cleanup

Phase 2.2 Pre Route Cleanup | Checksum: b71a21d0

Time (s): cpu = 00:00:21 ; elapsed = 00:00:17 . Memory (MB): peak = 2306.195 ; gain = 146.672 ; free physical = 781 ; free virtual = 2861

Phase 2 Router Initialization | Checksum: b71a21d0

Time (s): cpu = 00:00:21 ; elapsed = 00:00:17 . Memory (MB): peak = 2312.461 ; gain = 152.938 ; free physical = 778 ; free virtual = 2859

Phase 3 Initial Routing

Phase 3 Initial Routing | Checksum: 14cb178e5

Time (s): cpu = 00:00:21 ; elapsed = 00:00:17 . Memory (MB): peak = 2316.895 ; gain = 157.371 ; free physical = 774 ; free virtual = 2855

Phase 4 Rip-up And Reroute

Phase 4.1 Global Iteration 0

Number of Nodes with overlaps = 0

Phase 4.1 Global Iteration 0 | Checksum: 170c42c4d

Time (s): cpu = 00:00:21 ; elapsed = 00:00:17 . Memory (MB): peak = 2316.895 ; gain = 157.371 ; free physical = 775 ; free virtual = 2855

Phase 4 Rip-up And Reroute | Checksum: 170c42c4d

Time (s): cpu = 00:00:21 ; elapsed = 00:00:17 . Memory (MB): peak = 2316.895 ; gain = 157.371 ; free physical = 775 ; free virtual = 2855

Phase 5 Delay and Skew Optimization

Phase 5 Delay and Skew Optimization | Checksum: 170c42c4d

Time (s): cpu = 00:00:21 ; elapsed = 00:00:17 . Memory (MB): peak = 2316.895 ; gain = 157.371 ; free physical = 775 ; free virtual = 2855

Phase 6 Post Hold Fix

Phase 6.1 Hold Fix Iter

Phase 6.1 Hold Fix Iter | Checksum: 170c42c4d

Time (s): cpu = 00:00:21 ; elapsed = 00:00:17 . Memory (MB): peak = 2316.895 ; gain = 157.371 ; free physical = 775 ; free virtual = 2855

Phase 6 Post Hold Fix | Checksum: 170c42c4d

Time (s): cpu = 00:00:21 ; elapsed = 00:00:17 . Memory (MB): peak = 2316.895 ; gain = 157.371 ; free physical = 775 ; free virtual = 2855

Phase 7 Route finalize

Router Utilization Summary

Global Vertical Routing Utilization = 0.000522261 %

Global Horizontal Routing Utilization = 0.000426257 %

Routable Net Status\*

\*Does not include unroutable nets such as driverless and loadless.

Run report\_route\_status for detailed report.

Number of Failed Nets = 0

Number of Unrouted Nets = 0

Number of Partially Routed Nets = 0

Number of Node Overlaps = 0

Congestion Report

North Dir 1x1 Area, Max Cong = 4.5045%, No Congested Regions.

South Dir 1x1 Area, Max Cong = 6.30631%, No Congested Regions.

East Dir 1x1 Area, Max Cong = 1.47059%, No Congested Regions.

West Dir 1x1 Area, Max Cong = 2.94118%, No Congested Regions.

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Reporting congestion hotspots

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Direction: North

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Congested clusters found at Level 0

Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0

Direction: South

----------------

Congested clusters found at Level 0

Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0

Direction: East

----------------

Congested clusters found at Level 0

Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0

Direction: West

----------------

Congested clusters found at Level 0

Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0

Phase 7 Route finalize | Checksum: 170c42c4d

Time (s): cpu = 00:00:22 ; elapsed = 00:00:18 . Memory (MB): peak = 2316.895 ; gain = 157.371 ; free physical = 775 ; free virtual = 2855

Phase 8 Verifying routed nets

Verification completed successfully

Phase 8 Verifying routed nets | Checksum: 170c42c4d

Time (s): cpu = 00:00:22 ; elapsed = 00:00:18 . Memory (MB): peak = 2317.895 ; gain = 158.371 ; free physical = 774 ; free virtual = 2854

Phase 9 Depositing Routes

Phase 9 Depositing Routes | Checksum: 1414c5d4a

Time (s): cpu = 00:00:22 ; elapsed = 00:00:18 . Memory (MB): peak = 2317.895 ; gain = 158.371 ; free physical = 774 ; free virtual = 2854

INFO: [Route 35-16] Router Completed Successfully

Time (s): cpu = 00:00:22 ; elapsed = 00:00:18 . Memory (MB): peak = 2317.895 ; gain = 158.371 ; free physical = 790 ; free virtual = 2871

Routing Is Done.

INFO: [Common 17-83] Releasing license: Implementation

52 Infos, 1 Warnings, 0 Critical Warnings and 0 Errors encountered.

route\_design completed successfully

route\_design: Time (s): cpu = 00:00:23 ; elapsed = 00:00:18 . Memory (MB): peak = 2317.895 ; gain = 158.371 ; free physical = 792 ; free virtual = 2872

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2317.895 ; gain = 0.000 ; free physical = 792 ; free virtual = 2872

INFO: [Timing 38-480] Writing timing data to binary archive.

Writing placer database...

Writing XDEF routing.

Writing XDEF routing logical nets.

Writing XDEF routing special nets.

Write XDEF Complete: Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.01 . Memory (MB): peak = 2317.895 ; gain = 0.000 ; free physical = 790 ; free virtual = 2872

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2317.895 ; gain = 0.000 ; free physical = 789 ; free virtual = 2871

INFO: [Common 17-1381] The checkpoint '/home/jinson/vivado/Lab06\_clk\_odd/Lab06\_clk\_odd.runs/impl\_1/Lab06\_clk\_odd\_routed.dcp' has been generated.

INFO: [runtcl-4] Executing : report\_drc -file Lab06\_clk\_odd\_drc\_routed.rpt -pb Lab06\_clk\_odd\_drc\_routed.pb -rpx Lab06\_clk\_odd\_drc\_routed.rpx

Command: report\_drc -file Lab06\_clk\_odd\_drc\_routed.rpt -pb Lab06\_clk\_odd\_drc\_routed.pb -rpx Lab06\_clk\_odd\_drc\_routed.rpx

INFO: [IP\_Flow 19-1839] IP Catalog is up to date.

INFO: [DRC 23-27] Running DRC with 4 threads

INFO: [Coretcl 2-168] The results of DRC are in file /home/jinson/vivado/Lab06\_clk\_odd/Lab06\_clk\_odd.runs/impl\_1/Lab06\_clk\_odd\_drc\_routed.rpt.

report\_drc completed successfully

INFO: [runtcl-4] Executing : report\_methodology -file Lab06\_clk\_odd\_methodology\_drc\_routed.rpt -pb Lab06\_clk\_odd\_methodology\_drc\_routed.pb -rpx Lab06\_clk\_odd\_methodology\_drc\_routed.rpx

Command: report\_methodology -file Lab06\_clk\_odd\_methodology\_drc\_routed.rpt -pb Lab06\_clk\_odd\_methodology\_drc\_routed.pb -rpx Lab06\_clk\_odd\_methodology\_drc\_routed.rpx

INFO: [Timing 38-35] Done setting XDC timing constraints.

INFO: [DRC 23-133] Running Methodology with 4 threads

INFO: [Coretcl 2-1520] The results of Report Methodology are in file /home/jinson/vivado/Lab06\_clk\_odd/Lab06\_clk\_odd.runs/impl\_1/Lab06\_clk\_odd\_methodology\_drc\_routed.rpt.

report\_methodology completed successfully

INFO: [runtcl-4] Executing : report\_power -file Lab06\_clk\_odd\_power\_routed.rpt -pb Lab06\_clk\_odd\_power\_summary\_routed.pb -rpx Lab06\_clk\_odd\_power\_routed.rpx

Command: report\_power -file Lab06\_clk\_odd\_power\_routed.rpt -pb Lab06\_clk\_odd\_power\_summary\_routed.pb -rpx Lab06\_clk\_odd\_power\_routed.rpx

WARNING: [Power 33-232] No user defined clocks were found in the design!

Resolution: Please specify clocks using create\_clock/create\_generated\_clock for sequential elements. For pure combinatorial circuits, please specify a virtual clock, otherwise the vectorless estimation might be inaccurate

INFO: [Timing 38-35] Done setting XDC timing constraints.

Running Vector-less Activity Propagation...

Finished Running Vector-less Activity Propagation

64 Infos, 2 Warnings, 0 Critical Warnings and 0 Errors encountered.

report\_power completed successfully

INFO: [runtcl-4] Executing : report\_route\_status -file Lab06\_clk\_odd\_route\_status.rpt -pb Lab06\_clk\_odd\_route\_status.pb

INFO: [runtcl-4] Executing : report\_timing\_summary -max\_paths 10 -file Lab06\_clk\_odd\_timing\_summary\_routed.rpt -pb Lab06\_clk\_odd\_timing\_summary\_routed.pb -rpx Lab06\_clk\_odd\_timing\_summary\_routed.rpx -warn\_on\_violation

INFO: [Timing 38-91] UpdateTimingParams: Speed grade: -1, Delay Type: min\_max.

INFO: [Timing 38-191] Multithreading enabled for timing update using a maximum of 4 CPUs

WARNING: [Timing 38-313] There are no user specified timing constraints. Timing constraints are needed for proper timing analysis.

INFO: [runtcl-4] Executing : report\_incremental\_reuse -file Lab06\_clk\_odd\_incremental\_reuse\_routed.rpt

INFO: [Vivado\_Tcl 4-1062] Incremental flow is disabled. No incremental reuse Info to report.

INFO: [runtcl-4] Executing : report\_clock\_utilization -file Lab06\_clk\_odd\_clock\_utilization\_routed.rpt

INFO: [runtcl-4] Executing : report\_bus\_skew -warn\_on\_violation -file Lab06\_clk\_odd\_bus\_skew\_routed.rpt -pb Lab06\_clk\_odd\_bus\_skew\_routed.pb -rpx Lab06\_clk\_odd\_bus\_skew\_routed.rpx

INFO: [Timing 38-91] UpdateTimingParams: Speed grade: -1, Delay Type: min\_max.

INFO: [Timing 38-191] Multithreading enabled for timing update using a maximum of 4 CPUs

Command: write\_bitstream -force Lab06\_clk\_odd.bit

Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'

INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t'

Running DRC as a precondition to command write\_bitstream

INFO: [IP\_Flow 19-1839] IP Catalog is up to date.

INFO: [DRC 23-27] Running DRC with 4 threads

ERROR: [DRC LUTLP-1] Combinatorial Loop Alert: 1 LUT cells form a combinatorial loop. This can create a race condition. Timing analysis may not be accurate. The preferred resolution is to modify the design to remove combinatorial logic loops. If the loop is known and understood, this DRC can be bypassed by acknowledging the condition and setting the following XDC constraint on any one of the nets in the loop: 'set\_property ALLOW\_COMBINATORIAL\_LOOPS TRUE [get\_nets <myHier/myNet>]'. One net in the loop is out0[2]. Please evaluate your design. The cells in the loop are: valid\_reg\_i\_10.

ERROR: [DRC LUTLP-1] Combinatorial Loop Alert: 1 LUT cells form a combinatorial loop. This can create a race condition. Timing analysis may not be accurate. The preferred resolution is to modify the design to remove combinatorial logic loops. If the loop is known and understood, this DRC can be bypassed by acknowledging the condition and setting the following XDC constraint on any one of the nets in the loop: 'set\_property ALLOW\_COMBINATORIAL\_LOOPS TRUE [get\_nets <myHier/myNet>]'. One net in the loop is out0[3]. Please evaluate your design. The cells in the loop are: valid\_reg\_i\_6.

ERROR: [DRC LUTLP-1] Combinatorial Loop Alert: 1 LUT cells form a combinatorial loop. This can create a race condition. Timing analysis may not be accurate. The preferred resolution is to modify the design to remove combinatorial logic loops. If the loop is known and understood, this DRC can be bypassed by acknowledging the condition and setting the following XDC constraint on any one of the nets in the loop: 'set\_property ALLOW\_COMBINATORIAL\_LOOPS TRUE [get\_nets <myHier/myNet>]'. One net in the loop is out0\_\_0[1]. Please evaluate your design. The cells in the loop are: valid\_reg\_i\_11.

ERROR: [DRC LUTLP-1] Combinatorial Loop Alert: 1 LUT cells form a combinatorial loop. This can create a race condition. Timing analysis may not be accurate. The preferred resolution is to modify the design to remove combinatorial logic loops. If the loop is known and understood, this DRC can be bypassed by acknowledging the condition and setting the following XDC constraint on any one of the nets in the loop: 'set\_property ALLOW\_COMBINATORIAL\_LOOPS TRUE [get\_nets <myHier/myNet>]'. One net in the loop is out[0]. Please evaluate your design. The cells in the loop are: valid\_reg\_i\_8.

ERROR: [DRC LUTLP-1] Combinatorial Loop Alert: 1 LUT cells form a combinatorial loop. This can create a race condition. Timing analysis may not be accurate. The preferred resolution is to modify the design to remove combinatorial logic loops. If the loop is known and understood, this DRC can be bypassed by acknowledging the condition and setting the following XDC constraint on any one of the nets in the loop: 'set\_property ALLOW\_COMBINATORIAL\_LOOPS TRUE [get\_nets <myHier/myNet>]'. One net in the loop is out[3]. Please evaluate your design. The cells in the loop are: valid\_reg\_i\_3.

ERROR: [DRC LUTLP-1] Combinatorial Loop Alert: 1 LUT cells form a combinatorial loop. This can create a race condition. Timing analysis may not be accurate. The preferred resolution is to modify the design to remove combinatorial logic loops. If the loop is known and understood, this DRC can be bypassed by acknowledging the condition and setting the following XDC constraint on any one of the nets in the loop: 'set\_property ALLOW\_COMBINATORIAL\_LOOPS TRUE [get\_nets <myHier/myNet>]'. One net in the loop is out[4]. Please evaluate your design. The cells in the loop are: valid\_reg\_i\_5.

ERROR: [DRC LUTLP-1] Combinatorial Loop Alert: 1 LUT cells form a combinatorial loop. This can create a race condition. Timing analysis may not be accurate. The preferred resolution is to modify the design to remove combinatorial logic loops. If the loop is known and understood, this DRC can be bypassed by acknowledging the condition and setting the following XDC constraint on any one of the nets in the loop: 'set\_property ALLOW\_COMBINATORIAL\_LOOPS TRUE [get\_nets <myHier/myNet>]'. One net in the loop is valid\_reg\_i\_2\_n\_0. Please evaluate your design. The cells in the loop are: valid\_reg\_i\_2.

ERROR: [DRC LUTLP-1] Combinatorial Loop Alert: 11 LUT cells form a combinatorial loop. This can create a race condition. Timing analysis may not be accurate. The preferred resolution is to modify the design to remove combinatorial logic loops. If the loop is known and understood, this DRC can be bypassed by acknowledging the condition and setting the following XDC constraint on any one of the nets in the loop: 'set\_property ALLOW\_COMBINATORIAL\_LOOPS TRUE [get\_nets <myHier/myNet>]'. One net in the loop is out0[2]. Please evaluate your design. The cells in the loop are: valid\_reg\_i\_2, valid\_reg\_i\_3, valid\_reg\_i\_4, valid\_reg\_i\_5, valid\_reg\_i\_6, valid\_reg\_i\_7, valid\_reg\_i\_8, valid\_reg\_i\_9, valid\_reg\_i\_10, valid\_reg\_i\_11, and valid\_reg\_i\_12.

WARNING: [DRC CFGBVS-1] Missing CFGBVS and CONFIG\_VOLTAGE Design Properties: Neither the CFGBVS nor CONFIG\_VOLTAGE voltage property is set in the current\_design. Configuration bank voltage select (CFGBVS) must be set to VCCO or GND, and CONFIG\_VOLTAGE must be set to the correct configuration voltage, in order to determine the I/O voltage support for the pins in bank 0. It is suggested to specify these either using the 'Edit Device Properties' function in the GUI or directly in the XDC file using the following syntax:

set\_property CFGBVS value1 [current\_design]

#where value1 is either VCCO or GND

set\_property CONFIG\_VOLTAGE value2 [current\_design]

#where value2 is the voltage provided to configuration bank 0

Refer to the device configuration user guide for more information.

WARNING: [DRC PDRC-153] Gated clock check: Net valid\_reg\_i\_2\_n\_0 is a gated clock net sourced by a combinational pin valid\_reg\_i\_2/O, cell valid\_reg\_i\_2. This is not good design practice and will likely impact performance. For SLICE registers, for example, use the CE pin to control the loading of data.

INFO: [Vivado 12-3199] DRC finished with 8 Errors, 2 Warnings

INFO: [Vivado 12-3200] Please refer to the DRC report (report\_drc) for more information.

ERROR: [Vivado 12-1345] Error(s) found during DRC. Bitgen not run.

INFO: [Common 17-83] Releasing license: Implementation

80 Infos, 5 Warnings, 0 Critical Warnings and 9 Errors encountered.

write\_bitstream failed

ERROR: [Common 17-39] 'write\_bitstream' failed due to earlier errors.

INFO: [Common 17-206] Exiting Vivado at Thu Apr 25 19:08:12 2019...