\*\*\* Running vivado

with args -log Lab06\_clk\_odd.vds -m64 -product Vivado -mode batch -messageDb vivado.pb -notrace -source Lab06\_clk\_odd.tcl

\*\*\*\*\*\* Vivado v2018.3 (64-bit)

\*\*\*\* SW Build 2405991 on Thu Dec 6 23:36:41 MST 2018

\*\*\*\* IP Build 2404404 on Fri Dec 7 01:43:56 MST 2018

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CRITICAL WARNING: [Common 17-741] No write access right to the local Tcl store at '/home/jinson/.Xilinx/Vivado/2018.3/XilinxTclStore'. XilinxTclStore is reverted to the installation area. If you want to use local Tcl Store, please change the access right and relaunch Vivado.

source Lab06\_clk\_odd.tcl -notrace

Command: synth\_design -top Lab06\_clk\_odd -part xc7a100tcsg324-1

Starting synth\_design

Attempting to get a license for feature 'Synthesis' and/or device 'xc7a100t'

INFO: [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a100t'

INFO: Launching helper process for spawning children vivado processes

INFO: Helper process launched with PID 11880

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Starting RTL Elaboration : Time (s): cpu = 00:00:01 ; elapsed = 00:00:02 . Memory (MB): peak = 1389.355 ; gain = 0.000 ; free physical = 1619 ; free virtual = 3689

---------------------------------------------------------------------------------

INFO: [Synth 8-6157] synthesizing module 'Lab06\_clk\_odd' [/home/jinson/vivado/Lab06\_clk\_odd/Lab06\_clk\_odd.srcs/sources\_1/new/Lab06\_clk\_odd.v:23]

WARNING: [Synth 8-567] referenced signal 'out' should be on the sensitivity list [/home/jinson/vivado/Lab06\_clk\_odd/Lab06\_clk\_odd.srcs/sources\_1/new/Lab06\_clk\_odd.v:36]

WARNING: [Synth 8-567] referenced signal 'valid' should be on the sensitivity list [/home/jinson/vivado/Lab06\_clk\_odd/Lab06\_clk\_odd.srcs/sources\_1/new/Lab06\_clk\_odd.v:36]

INFO: [Synth 8-6155] done synthesizing module 'Lab06\_clk\_odd' (1#1) [/home/jinson/vivado/Lab06\_clk\_odd/Lab06\_clk\_odd.srcs/sources\_1/new/Lab06\_clk\_odd.v:23]

WARNING: [Synth 8-3331] design Lab06\_clk\_odd has unconnected port clk

---------------------------------------------------------------------------------

Finished RTL Elaboration : Time (s): cpu = 00:00:02 ; elapsed = 00:00:03 . Memory (MB): peak = 1389.355 ; gain = 0.000 ; free physical = 1629 ; free virtual = 3701

---------------------------------------------------------------------------------

Report Check Netlist:

+------+------------------+-------+---------+-------+------------------+

| |Item |Errors |Warnings |Status |Description |

+------+------------------+-------+---------+-------+------------------+

|1 |multi\_driven\_nets | 0| 0|Passed |Multi driven nets |

+------+------------------+-------+---------+-------+------------------+

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Start Handling Custom Attributes

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Finished Handling Custom Attributes : Time (s): cpu = 00:00:02 ; elapsed = 00:00:03 . Memory (MB): peak = 1389.355 ; gain = 0.000 ; free physical = 1629 ; free virtual = 3702

---------------------------------------------------------------------------------

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Finished RTL Optimization Phase 1 : Time (s): cpu = 00:00:02 ; elapsed = 00:00:03 . Memory (MB): peak = 1389.355 ; gain = 0.000 ; free physical = 1629 ; free virtual = 3702

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INFO: [Device 21-403] Loading part xc7a100tcsg324-1

INFO: [Project 1-570] Preparing netlist for logic optimization

Processing XDC Constraints

Initializing timing engine

Parsing XDC File [/home/jinson/vivado/Lab06\_clk\_odd/Lab06\_clk\_odd.srcs/constrs\_1/new/Lab06\_clk\_odd.xdc]

Finished Parsing XDC File [/home/jinson/vivado/Lab06\_clk\_odd/Lab06\_clk\_odd.srcs/constrs\_1/new/Lab06\_clk\_odd.xdc]

INFO: [Project 1-236] Implementation specific constraints were found while reading constraint file [/home/jinson/vivado/Lab06\_clk\_odd/Lab06\_clk\_odd.srcs/constrs\_1/new/Lab06\_clk\_odd.xdc]. These constraints will be ignored for synthesis but will be used in implementation. Impacted constraints are listed in the file [.Xil/Lab06\_clk\_odd\_propImpl.xdc].

Resolution: To avoid this warning, move constraints listed in [.Xil/Lab06\_clk\_odd\_propImpl.xdc] to another XDC file and exclude this new file from synthesis with the used\_in\_synthesis property (File Properties dialog in GUI) and re-run elaboration/synthesis.

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1653.141 ; gain = 0.000 ; free physical = 1378 ; free virtual = 3451

Completed Processing XDC Constraints

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1653.141 ; gain = 0.000 ; free physical = 1378 ; free virtual = 3451

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1653.141 ; gain = 0.000 ; free physical = 1378 ; free virtual = 3451

Constraint Validation Runtime : Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1653.141 ; gain = 0.000 ; free physical = 1378 ; free virtual = 3451

---------------------------------------------------------------------------------

Finished Constraint Validation : Time (s): cpu = 00:00:06 ; elapsed = 00:00:08 . Memory (MB): peak = 1653.141 ; gain = 263.785 ; free physical = 1447 ; free virtual = 3520

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Start Loading Part and Timing Information

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Loading part: xc7a100tcsg324-1

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Finished Loading Part and Timing Information : Time (s): cpu = 00:00:06 ; elapsed = 00:00:08 . Memory (MB): peak = 1653.141 ; gain = 263.785 ; free physical = 1447 ; free virtual = 3520

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---------------------------------------------------------------------------------

Start Applying 'set\_property' XDC Constraints

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---------------------------------------------------------------------------------

Finished applying 'set\_property' XDC Constraints : Time (s): cpu = 00:00:07 ; elapsed = 00:00:08 . Memory (MB): peak = 1653.141 ; gain = 263.785 ; free physical = 1448 ; free virtual = 3522

---------------------------------------------------------------------------------

WARNING: [Synth 8-327] inferring latch for variable 'valid\_reg' [/home/jinson/vivado/Lab06\_clk\_odd/Lab06\_clk\_odd.srcs/sources\_1/new/Lab06\_clk\_odd.v:38]

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Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:07 ; elapsed = 00:00:08 . Memory (MB): peak = 1653.141 ; gain = 263.785 ; free physical = 1439 ; free virtual = 3513

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Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

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Start RTL Component Statistics

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Detailed RTL Component Info :

+---Adders :

2 Input 5 Bit Adders := 1

+---Muxes :

2 Input 5 Bit Muxes := 1

---------------------------------------------------------------------------------

Finished RTL Component Statistics

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Start RTL Hierarchical Component Statistics

---------------------------------------------------------------------------------

Hierarchical RTL Component report

Module Lab06\_clk\_odd

Detailed RTL Component Info :

+---Adders :

2 Input 5 Bit Adders := 1

+---Muxes :

2 Input 5 Bit Muxes := 1

---------------------------------------------------------------------------------

Finished RTL Hierarchical Component Statistics

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Start Part Resource Summary

---------------------------------------------------------------------------------

Part Resources:

DSPs: 240 (col length:80)

BRAMs: 270 (col length: RAMB18 80 RAMB36 40)

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Finished Part Resource Summary

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---------------------------------------------------------------------------------

Start Cross Boundary and Area Optimization

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Warning: Parallel synthesis criteria is not met

WARNING: [Synth 8-3331] design Lab06\_clk\_odd has unconnected port clk

---------------------------------------------------------------------------------

Finished Cross Boundary and Area Optimization : Time (s): cpu = 00:00:07 ; elapsed = 00:00:09 . Memory (MB): peak = 1653.141 ; gain = 263.785 ; free physical = 1425 ; free virtual = 3503

---------------------------------------------------------------------------------

Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

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Start Applying XDC Timing Constraints

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---------------------------------------------------------------------------------

Finished Applying XDC Timing Constraints : Time (s): cpu = 00:00:11 ; elapsed = 00:00:13 . Memory (MB): peak = 1692.141 ; gain = 302.785 ; free physical = 1300 ; free virtual = 3378

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Start Timing Optimization

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Finished Timing Optimization : Time (s): cpu = 00:00:11 ; elapsed = 00:00:13 . Memory (MB): peak = 1692.141 ; gain = 302.785 ; free physical = 1300 ; free virtual = 3378

---------------------------------------------------------------------------------

Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

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Start Technology Mapping

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Finished Technology Mapping : Time (s): cpu = 00:00:11 ; elapsed = 00:00:13 . Memory (MB): peak = 1701.156 ; gain = 311.801 ; free physical = 1300 ; free virtual = 3377

---------------------------------------------------------------------------------

Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

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Start IO Insertion

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Start Flattening Before IO Insertion

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---------------------------------------------------------------------------------

Finished Flattening Before IO Insertion

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Start Final Netlist Cleanup

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Finished Final Netlist Cleanup

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Finished IO Insertion : Time (s): cpu = 00:00:12 ; elapsed = 00:00:13 . Memory (MB): peak = 1701.156 ; gain = 311.801 ; free physical = 1300 ; free virtual = 3377

---------------------------------------------------------------------------------

Report Check Netlist:

+------+------------------+-------+---------+-------+------------------+

| |Item |Errors |Warnings |Status |Description |

+------+------------------+-------+---------+-------+------------------+

|1 |multi\_driven\_nets | 0| 0|Passed |Multi driven nets |

+------+------------------+-------+---------+-------+------------------+

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Start Renaming Generated Instances

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Finished Renaming Generated Instances : Time (s): cpu = 00:00:12 ; elapsed = 00:00:13 . Memory (MB): peak = 1701.156 ; gain = 311.801 ; free physical = 1300 ; free virtual = 3377

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Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

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Start Rebuilding User Hierarchy

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Finished Rebuilding User Hierarchy : Time (s): cpu = 00:00:12 ; elapsed = 00:00:13 . Memory (MB): peak = 1701.156 ; gain = 311.801 ; free physical = 1300 ; free virtual = 3377

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---------------------------------------------------------------------------------

Start Renaming Generated Ports

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Finished Renaming Generated Ports : Time (s): cpu = 00:00:12 ; elapsed = 00:00:13 . Memory (MB): peak = 1701.156 ; gain = 311.801 ; free physical = 1300 ; free virtual = 3377

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Start Handling Custom Attributes

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Finished Handling Custom Attributes : Time (s): cpu = 00:00:12 ; elapsed = 00:00:13 . Memory (MB): peak = 1701.156 ; gain = 311.801 ; free physical = 1300 ; free virtual = 3377

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---------------------------------------------------------------------------------

Start Renaming Generated Nets

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---------------------------------------------------------------------------------

Finished Renaming Generated Nets : Time (s): cpu = 00:00:12 ; elapsed = 00:00:13 . Memory (MB): peak = 1701.156 ; gain = 311.801 ; free physical = 1300 ; free virtual = 3377

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---------------------------------------------------------------------------------

Start Writing Synthesis Report

---------------------------------------------------------------------------------

Report BlackBoxes:

+-+--------------+----------+

| |BlackBox name |Instances |

+-+--------------+----------+

+-+--------------+----------+

Report Cell Usage:

+------+-----+------+

| |Cell |Count |

+------+-----+------+

|1 |LUT1 | 1|

|2 |LUT2 | 1|

|3 |LUT4 | 1|

|4 |LUT5 | 1|

|5 |LUT6 | 8|

|6 |LD | 1|

|7 |OBUF | 1|

+------+-----+------+

Report Instance Areas:

+------+---------+-------+------+

| |Instance |Module |Cells |

+------+---------+-------+------+

|1 |top | | 14|

+------+---------+-------+------+

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Finished Writing Synthesis Report : Time (s): cpu = 00:00:12 ; elapsed = 00:00:13 . Memory (MB): peak = 1701.156 ; gain = 311.801 ; free physical = 1300 ; free virtual = 3377

---------------------------------------------------------------------------------

Synthesis finished with 0 errors, 0 critical warnings and 2 warnings.

Synthesis Optimization Runtime : Time (s): cpu = 00:00:09 ; elapsed = 00:00:10 . Memory (MB): peak = 1701.156 ; gain = 48.016 ; free physical = 1355 ; free virtual = 3433

Synthesis Optimization Complete : Time (s): cpu = 00:00:12 ; elapsed = 00:00:13 . Memory (MB): peak = 1701.164 ; gain = 311.801 ; free physical = 1355 ; free virtual = 3433

INFO: [Project 1-571] Translating synthesized netlist

INFO: [Netlist 29-17] Analyzing 1 Unisim elements for replacement

INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds

INFO: [Project 1-570] Preparing netlist for logic optimization

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1708.156 ; gain = 0.000 ; free physical = 1295 ; free virtual = 3372

INFO: [Project 1-111] Unisim Transformation Summary:

A total of 1 instances were transformed.

LD => LDCE: 1 instances

INFO: [Common 17-83] Releasing license: Synthesis

14 Infos, 5 Warnings, 0 Critical Warnings and 0 Errors encountered.

synth\_design completed successfully

synth\_design: Time (s): cpu = 00:00:13 ; elapsed = 00:00:14 . Memory (MB): peak = 1708.156 ; gain = 318.875 ; free physical = 1352 ; free virtual = 3429

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1708.156 ; gain = 0.000 ; free physical = 1352 ; free virtual = 3429

WARNING: [Constraints 18-5210] No constraints selected for write.

Resolution: This message can indicate that there are no constraints for the design, or it can indicate that the used\_in flags are set such that the constraints are ignored. This later case is used when running synth\_design to not write synthesis constraints to the resulting checkpoint. Instead, project constraints are read when the synthesized design is opened.

INFO: [Common 17-1381] The checkpoint '/home/jinson/vivado/Lab06\_clk\_odd/Lab06\_clk\_odd.runs/synth\_1/Lab06\_clk\_odd.dcp' has been generated.

INFO: [runtcl-4] Executing : report\_utilization -file Lab06\_clk\_odd\_utilization\_synth.rpt -pb Lab06\_clk\_odd\_utilization\_synth.pb

INFO: [Common 17-206] Exiting Vivado at Thu Apr 25 19:07:23 2019...