\*\*\* Running vivado

with args -log Lab06\_count.vds -m64 -product Vivado -mode batch -messageDb vivado.pb -notrace -source Lab06\_count.tcl

\*\*\*\*\*\* Vivado v2018.3 (64-bit)

\*\*\*\* SW Build 2405991 on Thu Dec 6 23:36:41 MST 2018

\*\*\*\* IP Build 2404404 on Fri Dec 7 01:43:56 MST 2018

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CRITICAL WARNING: [Common 17-741] No write access right to the local Tcl store at '/home/jinson/.Xilinx/Vivado/2018.3/XilinxTclStore'. XilinxTclStore is reverted to the installation area. If you want to use local Tcl Store, please change the access right and relaunch Vivado.

source Lab06\_count.tcl -notrace

Command: synth\_design -top Lab06\_count -part xc7a100tcsg324-1

Starting synth\_design

Attempting to get a license for feature 'Synthesis' and/or device 'xc7a100t'

INFO: [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a100t'

INFO: Launching helper process for spawning children vivado processes

INFO: Helper process launched with PID 4296

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Starting RTL Elaboration : Time (s): cpu = 00:00:01 ; elapsed = 00:00:02 . Memory (MB): peak = 1380.348 ; gain = 0.000 ; free physical = 106 ; free virtual = 2855

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INFO: [Synth 8-6157] synthesizing module 'Lab06\_count' [/home/jinson/vivado/Lab06\_count/Lab06\_count.srcs/sources\_1/new/Lab06\_count.v:23]

WARNING: [Synth 8-3848] Net dp in module/entity Lab06\_count does not have driver. [/home/jinson/vivado/Lab06\_count/Lab06\_count.srcs/sources\_1/new/Lab06\_count.v:56]

INFO: [Synth 8-6155] done synthesizing module 'Lab06\_count' (1#1) [/home/jinson/vivado/Lab06\_count/Lab06\_count.srcs/sources\_1/new/Lab06\_count.v:23]

WARNING: [Synth 8-3331] design Lab06\_count has unconnected port dp

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Finished RTL Elaboration : Time (s): cpu = 00:00:02 ; elapsed = 00:00:03 . Memory (MB): peak = 1386.273 ; gain = 5.926 ; free physical = 171 ; free virtual = 2860

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Report Check Netlist:

+------+------------------+-------+---------+-------+------------------+

| |Item |Errors |Warnings |Status |Description |

+------+------------------+-------+---------+-------+------------------+

|1 |multi\_driven\_nets | 0| 0|Passed |Multi driven nets |

+------+------------------+-------+---------+-------+------------------+

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Start Handling Custom Attributes

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Finished Handling Custom Attributes : Time (s): cpu = 00:00:02 ; elapsed = 00:00:04 . Memory (MB): peak = 1386.273 ; gain = 5.926 ; free physical = 146 ; free virtual = 2835

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Finished RTL Optimization Phase 1 : Time (s): cpu = 00:00:02 ; elapsed = 00:00:04 . Memory (MB): peak = 1386.273 ; gain = 5.926 ; free physical = 146 ; free virtual = 2835

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INFO: [Device 21-403] Loading part xc7a100tcsg324-1

INFO: [Project 1-570] Preparing netlist for logic optimization

Processing XDC Constraints

Initializing timing engine

Parsing XDC File [/home/jinson/vivado/Lab06\_count/Lab06\_count.srcs/constrs\_1/new/Lab06\_count.xdc]

WARNING: [Vivado 12-584] No ports matched 'order'. [/home/jinson/vivado/Lab06\_count/Lab06\_count.srcs/constrs\_1/new/Lab06\_count.xdc:10]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [/home/jinson/vivado/Lab06\_count/Lab06\_count.srcs/constrs\_1/new/Lab06\_count.xdc:10]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'out\_dp'. [/home/jinson/vivado/Lab06\_count/Lab06\_count.srcs/constrs\_1/new/Lab06\_count.xdc:11]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [/home/jinson/vivado/Lab06\_count/Lab06\_count.srcs/constrs\_1/new/Lab06\_count.xdc:11]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'order'. [/home/jinson/vivado/Lab06\_count/Lab06\_count.srcs/constrs\_1/new/Lab06\_count.xdc:20]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [/home/jinson/vivado/Lab06\_count/Lab06\_count.srcs/constrs\_1/new/Lab06\_count.xdc:20]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'out\_dp'. [/home/jinson/vivado/Lab06\_count/Lab06\_count.srcs/constrs\_1/new/Lab06\_count.xdc:21]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [/home/jinson/vivado/Lab06\_count/Lab06\_count.srcs/constrs\_1/new/Lab06\_count.xdc:21]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'order'. [/home/jinson/vivado/Lab06\_count/Lab06\_count.srcs/constrs\_1/new/Lab06\_count.xdc:29]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [/home/jinson/vivado/Lab06\_count/Lab06\_count.srcs/constrs\_1/new/Lab06\_count.xdc:29]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'out\_dp'. [/home/jinson/vivado/Lab06\_count/Lab06\_count.srcs/constrs\_1/new/Lab06\_count.xdc:30]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [/home/jinson/vivado/Lab06\_count/Lab06\_count.srcs/constrs\_1/new/Lab06\_count.xdc:30]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'out\_dp'. [/home/jinson/vivado/Lab06\_count/Lab06\_count.srcs/constrs\_1/new/Lab06\_count.xdc:40]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [/home/jinson/vivado/Lab06\_count/Lab06\_count.srcs/constrs\_1/new/Lab06\_count.xdc:40]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'order'. [/home/jinson/vivado/Lab06\_count/Lab06\_count.srcs/constrs\_1/new/Lab06\_count.xdc:42]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [/home/jinson/vivado/Lab06\_count/Lab06\_count.srcs/constrs\_1/new/Lab06\_count.xdc:42]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'up\_down'. [/home/jinson/vivado/Lab06\_count/Lab06\_count.srcs/constrs\_1/new/Lab06\_count.xdc:96]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [/home/jinson/vivado/Lab06\_count/Lab06\_count.srcs/constrs\_1/new/Lab06\_count.xdc:96]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

WARNING: [Vivado 12-584] No ports matched 'up\_down'. [/home/jinson/vivado/Lab06\_count/Lab06\_count.srcs/constrs\_1/new/Lab06\_count.xdc:97]

CRITICAL WARNING: [Common 17-55] 'set\_property' expects at least one object. [/home/jinson/vivado/Lab06\_count/Lab06\_count.srcs/constrs\_1/new/Lab06\_count.xdc:97]

Resolution: If [get\_<value>] was used to populate the object, check to make sure this command returns at least one valid object.

Finished Parsing XDC File [/home/jinson/vivado/Lab06\_count/Lab06\_count.srcs/constrs\_1/new/Lab06\_count.xdc]

INFO: [Project 1-236] Implementation specific constraints were found while reading constraint file [/home/jinson/vivado/Lab06\_count/Lab06\_count.srcs/constrs\_1/new/Lab06\_count.xdc]. These constraints will be ignored for synthesis but will be used in implementation. Impacted constraints are listed in the file [.Xil/Lab06\_count\_propImpl.xdc].

Resolution: To avoid this warning, move constraints listed in [.Xil/Lab06\_count\_propImpl.xdc] to another XDC file and exclude this new file from synthesis with the used\_in\_synthesis property (File Properties dialog in GUI) and re-run elaboration/synthesis.

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1706.156 ; gain = 0.000 ; free physical = 106 ; free virtual = 2593

Completed Processing XDC Constraints

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1706.156 ; gain = 0.000 ; free physical = 106 ; free virtual = 2593

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1706.156 ; gain = 0.000 ; free physical = 106 ; free virtual = 2593

Constraint Validation Runtime : Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1706.156 ; gain = 0.000 ; free physical = 106 ; free virtual = 2593

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Finished Constraint Validation : Time (s): cpu = 00:00:07 ; elapsed = 00:00:10 . Memory (MB): peak = 1706.156 ; gain = 325.809 ; free physical = 213 ; free virtual = 2700

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Start Loading Part and Timing Information

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Loading part: xc7a100tcsg324-1

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Finished Loading Part and Timing Information : Time (s): cpu = 00:00:07 ; elapsed = 00:00:10 . Memory (MB): peak = 1706.156 ; gain = 325.809 ; free physical = 213 ; free virtual = 2700

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Start Applying 'set\_property' XDC Constraints

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Finished applying 'set\_property' XDC Constraints : Time (s): cpu = 00:00:07 ; elapsed = 00:00:10 . Memory (MB): peak = 1706.156 ; gain = 325.809 ; free physical = 215 ; free virtual = 2702

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INFO: [Synth 8-5818] HDL ADVISOR - The operator resource <adder> is shared. To prevent sharing consider applying a KEEP on the output of the operator [/home/jinson/vivado/Lab06\_count/Lab06\_count.srcs/sources\_1/new/Lab06\_count.v:70]

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Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:07 ; elapsed = 00:00:10 . Memory (MB): peak = 1706.156 ; gain = 325.809 ; free physical = 206 ; free virtual = 2693

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Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

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Start RTL Component Statistics

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Detailed RTL Component Info :

+---Adders :

2 Input 4 Bit Adders := 1

2 Input 3 Bit Adders := 1

+---Registers :

4 Bit Registers := 1

3 Bit Registers := 1

+---Muxes :

2 Input 2 Bit Muxes := 1

2 Input 1 Bit Muxes := 1

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Finished RTL Component Statistics

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Start RTL Hierarchical Component Statistics

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Hierarchical RTL Component report

Module Lab06\_count

Detailed RTL Component Info :

+---Adders :

2 Input 4 Bit Adders := 1

2 Input 3 Bit Adders := 1

+---Registers :

4 Bit Registers := 1

3 Bit Registers := 1

+---Muxes :

2 Input 2 Bit Muxes := 1

2 Input 1 Bit Muxes := 1

---------------------------------------------------------------------------------

Finished RTL Hierarchical Component Statistics

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---------------------------------------------------------------------------------

Start Part Resource Summary

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Part Resources:

DSPs: 240 (col length:80)

BRAMs: 270 (col length: RAMB18 80 RAMB36 40)

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Finished Part Resource Summary

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Start Cross Boundary and Area Optimization

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Warning: Parallel synthesis criteria is not met

WARNING: [Synth 8-3331] design Lab06\_count has unconnected port dp

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Finished Cross Boundary and Area Optimization : Time (s): cpu = 00:00:08 ; elapsed = 00:00:11 . Memory (MB): peak = 1706.156 ; gain = 325.809 ; free physical = 187 ; free virtual = 2679

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Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

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Start Applying XDC Timing Constraints

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Finished Applying XDC Timing Constraints : Time (s): cpu = 00:00:12 ; elapsed = 00:00:15 . Memory (MB): peak = 1706.156 ; gain = 325.809 ; free physical = 112 ; free virtual = 2561

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Start Timing Optimization

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Finished Timing Optimization : Time (s): cpu = 00:00:12 ; elapsed = 00:00:15 . Memory (MB): peak = 1706.156 ; gain = 325.809 ; free physical = 112 ; free virtual = 2561

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Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

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Start Technology Mapping

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Finished Technology Mapping : Time (s): cpu = 00:00:12 ; elapsed = 00:00:15 . Memory (MB): peak = 1714.164 ; gain = 333.816 ; free physical = 133 ; free virtual = 2559

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Report RTL Partitions:

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| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

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Start IO Insertion

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Start Flattening Before IO Insertion

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Finished Flattening Before IO Insertion

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Start Final Netlist Cleanup

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Finished Final Netlist Cleanup

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---------------------------------------------------------------------------------

Finished IO Insertion : Time (s): cpu = 00:00:13 ; elapsed = 00:00:16 . Memory (MB): peak = 1714.164 ; gain = 333.816 ; free physical = 135 ; free virtual = 2560

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Report Check Netlist:

+------+------------------+-------+---------+-------+------------------+

| |Item |Errors |Warnings |Status |Description |

+------+------------------+-------+---------+-------+------------------+

|1 |multi\_driven\_nets | 0| 0|Passed |Multi driven nets |

+------+------------------+-------+---------+-------+------------------+

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Start Renaming Generated Instances

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Finished Renaming Generated Instances : Time (s): cpu = 00:00:13 ; elapsed = 00:00:16 . Memory (MB): peak = 1714.164 ; gain = 333.816 ; free physical = 135 ; free virtual = 2560

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Report RTL Partitions:

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| |RTL Partition |Replication |Instances |

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+-+--------------+------------+----------+

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Start Rebuilding User Hierarchy

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Finished Rebuilding User Hierarchy : Time (s): cpu = 00:00:13 ; elapsed = 00:00:16 . Memory (MB): peak = 1714.164 ; gain = 333.816 ; free physical = 135 ; free virtual = 2560

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Start Renaming Generated Ports

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Finished Renaming Generated Ports : Time (s): cpu = 00:00:13 ; elapsed = 00:00:16 . Memory (MB): peak = 1714.164 ; gain = 333.816 ; free physical = 135 ; free virtual = 2560

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Start Handling Custom Attributes

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Finished Handling Custom Attributes : Time (s): cpu = 00:00:13 ; elapsed = 00:00:16 . Memory (MB): peak = 1714.164 ; gain = 333.816 ; free physical = 135 ; free virtual = 2560

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Start Renaming Generated Nets

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Finished Renaming Generated Nets : Time (s): cpu = 00:00:13 ; elapsed = 00:00:16 . Memory (MB): peak = 1714.164 ; gain = 333.816 ; free physical = 135 ; free virtual = 2560

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Start Writing Synthesis Report

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Report BlackBoxes:

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| |BlackBox name |Instances |

+-+--------------+----------+

+-+--------------+----------+

Report Cell Usage:

+------+-------+------+

| |Cell |Count |

+------+-------+------+

|1 |BUFG | 1|

|2 |CARRY4 | 6|

|3 |LUT1 | 3|

|4 |LUT3 | 2|

|5 |LUT4 | 18|

|6 |LUT5 | 1|

|7 |LUT6 | 1|

|8 |FDRE | 31|

|9 |IBUF | 10|

|10 |OBUF | 15|

|11 |OBUFT | 1|

+------+-------+------+

Report Instance Areas:

+------+---------+-------+------+

| |Instance |Module |Cells |

+------+---------+-------+------+

|1 |top | | 89|

+------+---------+-------+------+

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Finished Writing Synthesis Report : Time (s): cpu = 00:00:13 ; elapsed = 00:00:16 . Memory (MB): peak = 1714.164 ; gain = 333.816 ; free physical = 135 ; free virtual = 2560

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Synthesis finished with 0 errors, 0 critical warnings and 1 warnings.

Synthesis Optimization Runtime : Time (s): cpu = 00:00:09 ; elapsed = 00:00:11 . Memory (MB): peak = 1714.164 ; gain = 13.934 ; free physical = 189 ; free virtual = 2614

Synthesis Optimization Complete : Time (s): cpu = 00:00:13 ; elapsed = 00:00:16 . Memory (MB): peak = 1714.172 ; gain = 333.816 ; free physical = 189 ; free virtual = 2614

INFO: [Project 1-571] Translating synthesized netlist

INFO: [Netlist 29-17] Analyzing 6 Unisim elements for replacement

INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds

INFO: [Project 1-570] Preparing netlist for logic optimization

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1714.172 ; gain = 0.000 ; free physical = 128 ; free virtual = 2557

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

INFO: [Common 17-83] Releasing license: Synthesis

15 Infos, 13 Warnings, 10 Critical Warnings and 0 Errors encountered.

synth\_design completed successfully

synth\_design: Time (s): cpu = 00:00:14 ; elapsed = 00:00:17 . Memory (MB): peak = 1714.172 ; gain = 333.898 ; free physical = 185 ; free virtual = 2613

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1714.172 ; gain = 0.000 ; free physical = 185 ; free virtual = 2613

WARNING: [Constraints 18-5210] No constraints selected for write.

Resolution: This message can indicate that there are no constraints for the design, or it can indicate that the used\_in flags are set such that the constraints are ignored. This later case is used when running synth\_design to not write synthesis constraints to the resulting checkpoint. Instead, project constraints are read when the synthesized design is opened.

INFO: [Common 17-1381] The checkpoint '/home/jinson/vivado/Lab06\_count/Lab06\_count.runs/synth\_1/Lab06\_count.dcp' has been generated.

INFO: [runtcl-4] Executing : report\_utilization -file Lab06\_count\_utilization\_synth.rpt -pb Lab06\_count\_utilization\_synth.pb

INFO: [Common 17-206] Exiting Vivado at Sun Apr 28 17:24:33 2019...