\*\*\* Running vivado

with args -log Lab07\_movTimer\_2.vds -m64 -product Vivado -mode batch -messageDb vivado.pb -notrace -source Lab07\_movTimer\_2.tcl

\*\*\*\*\*\* Vivado v2018.3 (64-bit)

\*\*\*\* SW Build 2405991 on Thu Dec 6 23:36:41 MST 2018

\*\*\*\* IP Build 2404404 on Fri Dec 7 01:43:56 MST 2018

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CRITICAL WARNING: [Common 17-741] No write access right to the local Tcl store at '/home/jinson/.Xilinx/Vivado/2018.3/XilinxTclStore'. XilinxTclStore is reverted to the installation area. If you want to use local Tcl Store, please change the access right and relaunch Vivado.

source Lab07\_movTimer\_2.tcl -notrace

Command: synth\_design -top Lab07\_movTimer\_2 -part xc7a100tcsg324-1

Starting synth\_design

Attempting to get a license for feature 'Synthesis' and/or device 'xc7a100t'

INFO: [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a100t'

INFO: Launching helper process for spawning children vivado processes

INFO: Helper process launched with PID 93244

---------------------------------------------------------------------------------

Starting RTL Elaboration : Time (s): cpu = 00:00:02 ; elapsed = 00:00:02 . Memory (MB): peak = 1361.094 ; gain = 0.000 ; free physical = 826 ; free virtual = 2594

---------------------------------------------------------------------------------

INFO: [Synth 8-6157] synthesizing module 'Lab07\_movTimer\_2' [/home/jinson/vivado/Lab07\_movTimer\_2/Lab07\_movTimer\_2.srcs/sources\_1/new/Lab07\_movTimer\_2.sv:23]

INFO: [Synth 8-226] default block is never used [/home/jinson/vivado/Lab07\_movTimer\_2/Lab07\_movTimer\_2.srcs/sources\_1/new/Lab07\_movTimer\_2.sv:60]

INFO: [Synth 8-226] default block is never used [/home/jinson/vivado/Lab07\_movTimer\_2/Lab07\_movTimer\_2.srcs/sources\_1/new/Lab07\_movTimer\_2.sv:101]

INFO: [Synth 8-226] default block is never used [/home/jinson/vivado/Lab07\_movTimer\_2/Lab07\_movTimer\_2.srcs/sources\_1/new/Lab07\_movTimer\_2.sv:142]

INFO: [Synth 8-226] default block is never used [/home/jinson/vivado/Lab07\_movTimer\_2/Lab07\_movTimer\_2.srcs/sources\_1/new/Lab07\_movTimer\_2.sv:195]

INFO: [Synth 8-226] default block is never used [/home/jinson/vivado/Lab07\_movTimer\_2/Lab07\_movTimer\_2.srcs/sources\_1/new/Lab07\_movTimer\_2.sv:253]

INFO: [Synth 8-226] default block is never used [/home/jinson/vivado/Lab07\_movTimer\_2/Lab07\_movTimer\_2.srcs/sources\_1/new/Lab07\_movTimer\_2.sv:311]

INFO: [Synth 8-226] default block is never used [/home/jinson/vivado/Lab07\_movTimer\_2/Lab07\_movTimer\_2.srcs/sources\_1/new/Lab07\_movTimer\_2.sv:378]

INFO: [Synth 8-226] default block is never used [/home/jinson/vivado/Lab07\_movTimer\_2/Lab07\_movTimer\_2.srcs/sources\_1/new/Lab07\_movTimer\_2.sv:450]

INFO: [Synth 8-226] default block is never used [/home/jinson/vivado/Lab07\_movTimer\_2/Lab07\_movTimer\_2.srcs/sources\_1/new/Lab07\_movTimer\_2.sv:522]

INFO: [Synth 8-226] default block is never used [/home/jinson/vivado/Lab07\_movTimer\_2/Lab07\_movTimer\_2.srcs/sources\_1/new/Lab07\_movTimer\_2.sv:603]

INFO: [Synth 8-226] default block is never used [/home/jinson/vivado/Lab07\_movTimer\_2/Lab07\_movTimer\_2.srcs/sources\_1/new/Lab07\_movTimer\_2.sv:686]

INFO: [Synth 8-226] default block is never used [/home/jinson/vivado/Lab07\_movTimer\_2/Lab07\_movTimer\_2.srcs/sources\_1/new/Lab07\_movTimer\_2.sv:757]

INFO: [Synth 8-226] default block is never used [/home/jinson/vivado/Lab07\_movTimer\_2/Lab07\_movTimer\_2.srcs/sources\_1/new/Lab07\_movTimer\_2.sv:822]

INFO: [Synth 8-226] default block is never used [/home/jinson/vivado/Lab07\_movTimer\_2/Lab07\_movTimer\_2.srcs/sources\_1/new/Lab07\_movTimer\_2.sv:887]

INFO: [Synth 8-226] default block is never used [/home/jinson/vivado/Lab07\_movTimer\_2/Lab07\_movTimer\_2.srcs/sources\_1/new/Lab07\_movTimer\_2.sv:943]

INFO: [Synth 8-226] default block is never used [/home/jinson/vivado/Lab07\_movTimer\_2/Lab07\_movTimer\_2.srcs/sources\_1/new/Lab07\_movTimer\_2.sv:994]

INFO: [Synth 8-226] default block is never used [/home/jinson/vivado/Lab07\_movTimer\_2/Lab07\_movTimer\_2.srcs/sources\_1/new/Lab07\_movTimer\_2.sv:1045]

INFO: [Synth 8-226] default block is never used [/home/jinson/vivado/Lab07\_movTimer\_2/Lab07\_movTimer\_2.srcs/sources\_1/new/Lab07\_movTimer\_2.sv:1087]

INFO: [Synth 8-226] default block is never used [/home/jinson/vivado/Lab07\_movTimer\_2/Lab07\_movTimer\_2.srcs/sources\_1/new/Lab07\_movTimer\_2.sv:1127]

INFO: [Synth 8-226] default block is never used [/home/jinson/vivado/Lab07\_movTimer\_2/Lab07\_movTimer\_2.srcs/sources\_1/new/Lab07\_movTimer\_2.sv:1167]

INFO: [Synth 8-155] case statement is not full and has no default [/home/jinson/vivado/Lab07\_movTimer\_2/Lab07\_movTimer\_2.srcs/sources\_1/new/Lab07\_movTimer\_2.sv:58]

INFO: [Synth 8-6155] done synthesizing module 'Lab07\_movTimer\_2' (1#1) [/home/jinson/vivado/Lab07\_movTimer\_2/Lab07\_movTimer\_2.srcs/sources\_1/new/Lab07\_movTimer\_2.sv:23]

WARNING: [Synth 8-3917] design Lab07\_movTimer\_2 has port dp driven by constant 1

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Finished RTL Elaboration : Time (s): cpu = 00:00:02 ; elapsed = 00:00:03 . Memory (MB): peak = 1395.520 ; gain = 34.426 ; free physical = 835 ; free virtual = 2605

---------------------------------------------------------------------------------

Report Check Netlist:

+------+------------------+-------+---------+-------+------------------+

| |Item |Errors |Warnings |Status |Description |

+------+------------------+-------+---------+-------+------------------+

|1 |multi\_driven\_nets | 0| 0|Passed |Multi driven nets |

+------+------------------+-------+---------+-------+------------------+

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Start Handling Custom Attributes

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Finished Handling Custom Attributes : Time (s): cpu = 00:00:02 ; elapsed = 00:00:03 . Memory (MB): peak = 1395.520 ; gain = 34.426 ; free physical = 835 ; free virtual = 2605

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Finished RTL Optimization Phase 1 : Time (s): cpu = 00:00:02 ; elapsed = 00:00:03 . Memory (MB): peak = 1395.520 ; gain = 34.426 ; free physical = 835 ; free virtual = 2605

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INFO: [Device 21-403] Loading part xc7a100tcsg324-1

INFO: [Project 1-570] Preparing netlist for logic optimization

Processing XDC Constraints

Initializing timing engine

Parsing XDC File [/home/jinson/vivado/Lab07\_movTimer\_2/Lab07\_movTimer\_2.srcs/constrs\_1/new/Lab07\_movTimer\_2.xdc]

Finished Parsing XDC File [/home/jinson/vivado/Lab07\_movTimer\_2/Lab07\_movTimer\_2.srcs/constrs\_1/new/Lab07\_movTimer\_2.xdc]

INFO: [Project 1-236] Implementation specific constraints were found while reading constraint file [/home/jinson/vivado/Lab07\_movTimer\_2/Lab07\_movTimer\_2.srcs/constrs\_1/new/Lab07\_movTimer\_2.xdc]. These constraints will be ignored for synthesis but will be used in implementation. Impacted constraints are listed in the file [.Xil/Lab07\_movTimer\_2\_propImpl.xdc].

Resolution: To avoid this warning, move constraints listed in [.Xil/Lab07\_movTimer\_2\_propImpl.xdc] to another XDC file and exclude this new file from synthesis with the used\_in\_synthesis property (File Properties dialog in GUI) and re-run elaboration/synthesis.

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1729.863 ; gain = 0.000 ; free physical = 544 ; free virtual = 2348

Completed Processing XDC Constraints

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1729.863 ; gain = 0.000 ; free physical = 544 ; free virtual = 2348

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1729.863 ; gain = 0.000 ; free physical = 544 ; free virtual = 2348

Constraint Validation Runtime : Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1729.863 ; gain = 0.000 ; free physical = 544 ; free virtual = 2348

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Finished Constraint Validation : Time (s): cpu = 00:00:07 ; elapsed = 00:00:09 . Memory (MB): peak = 1729.863 ; gain = 368.770 ; free physical = 614 ; free virtual = 2418

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Start Loading Part and Timing Information

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Loading part: xc7a100tcsg324-1

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Finished Loading Part and Timing Information : Time (s): cpu = 00:00:07 ; elapsed = 00:00:10 . Memory (MB): peak = 1729.863 ; gain = 368.770 ; free physical = 614 ; free virtual = 2418

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Start Applying 'set\_property' XDC Constraints

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Finished applying 'set\_property' XDC Constraints : Time (s): cpu = 00:00:07 ; elapsed = 00:00:10 . Memory (MB): peak = 1729.863 ; gain = 368.770 ; free physical = 616 ; free virtual = 2420

---------------------------------------------------------------------------------

INFO: [Synth 8-5545] ROM "num" won't be mapped to RAM because address size (32) is larger than maximum supported(25)

INFO: [Synth 8-5546] ROM "num" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "d" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "d" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5545] ROM "num" won't be mapped to RAM because address size (32) is larger than maximum supported(25)

INFO: [Synth 8-5546] ROM "num" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "d" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "d" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5544] ROM "num" won't be mapped to Block RAM because address size (3) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "num" won't be mapped to Block RAM because address size (3) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "num" won't be mapped to Block RAM because address size (3) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "num" won't be mapped to Block RAM because address size (3) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "num" won't be mapped to Block RAM because address size (3) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "num" won't be mapped to Block RAM because address size (1) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "an" won't be mapped to Block RAM because address size (3) smaller than threshold (5)

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Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:08 ; elapsed = 00:00:10 . Memory (MB): peak = 1729.863 ; gain = 368.770 ; free physical = 606 ; free virtual = 2410

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Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

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Start RTL Component Statistics

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Detailed RTL Component Info :

+---Adders :

2 Input 9 Bit Adders := 1

2 Input 7 Bit Adders := 1

2 Input 6 Bit Adders := 2

2 Input 3 Bit Adders := 1

+---Registers :

9 Bit Registers := 1

8 Bit Registers := 1

7 Bit Registers := 2

6 Bit Registers := 1

3 Bit Registers := 1

+---Muxes :

2 Input 9 Bit Muxes := 1

8 Input 8 Bit Muxes := 1

8 Input 7 Bit Muxes := 13

6 Input 7 Bit Muxes := 2

10 Input 7 Bit Muxes := 2

3 Input 7 Bit Muxes := 1

2 Input 6 Bit Muxes := 3

2 Input 1 Bit Muxes := 3

21 Input 1 Bit Muxes := 1

3 Input 1 Bit Muxes := 1

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Finished RTL Component Statistics

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Start RTL Hierarchical Component Statistics

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Hierarchical RTL Component report

Module Lab07\_movTimer\_2

Detailed RTL Component Info :

+---Adders :

2 Input 9 Bit Adders := 1

2 Input 7 Bit Adders := 1

2 Input 6 Bit Adders := 2

2 Input 3 Bit Adders := 1

+---Registers :

9 Bit Registers := 1

8 Bit Registers := 1

7 Bit Registers := 2

6 Bit Registers := 1

3 Bit Registers := 1

+---Muxes :

2 Input 9 Bit Muxes := 1

8 Input 8 Bit Muxes := 1

8 Input 7 Bit Muxes := 13

6 Input 7 Bit Muxes := 2

10 Input 7 Bit Muxes := 2

3 Input 7 Bit Muxes := 1

2 Input 6 Bit Muxes := 3

2 Input 1 Bit Muxes := 3

21 Input 1 Bit Muxes := 1

3 Input 1 Bit Muxes := 1

---------------------------------------------------------------------------------

Finished RTL Hierarchical Component Statistics

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---------------------------------------------------------------------------------

Start Part Resource Summary

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Part Resources:

DSPs: 240 (col length:80)

BRAMs: 270 (col length: RAMB18 80 RAMB36 40)

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Finished Part Resource Summary

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Start Cross Boundary and Area Optimization

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Warning: Parallel synthesis criteria is not met

INFO: [Synth 8-5546] ROM "d" won't be mapped to RAM because it is too sparse

WARNING: [Synth 8-3917] design Lab07\_movTimer\_2 has port dp driven by constant 1

---------------------------------------------------------------------------------

Finished Cross Boundary and Area Optimization : Time (s): cpu = 00:00:15 ; elapsed = 00:00:18 . Memory (MB): peak = 1729.863 ; gain = 368.770 ; free physical = 570 ; free virtual = 2380

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Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

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Start Applying XDC Timing Constraints

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Finished Applying XDC Timing Constraints : Time (s): cpu = 00:00:20 ; elapsed = 00:00:23 . Memory (MB): peak = 1729.863 ; gain = 368.770 ; free physical = 445 ; free virtual = 2262

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Start Timing Optimization

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Finished Timing Optimization : Time (s): cpu = 00:00:20 ; elapsed = 00:00:23 . Memory (MB): peak = 1729.863 ; gain = 368.770 ; free physical = 445 ; free virtual = 2261

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Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

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Start Technology Mapping

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Finished Technology Mapping : Time (s): cpu = 00:00:20 ; elapsed = 00:00:23 . Memory (MB): peak = 1746.887 ; gain = 385.793 ; free physical = 441 ; free virtual = 2257

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Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

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Start IO Insertion

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---------------------------------------------------------------------------------

Start Flattening Before IO Insertion

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---------------------------------------------------------------------------------

Finished Flattening Before IO Insertion

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---------------------------------------------------------------------------------

Start Final Netlist Cleanup

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Finished Final Netlist Cleanup

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Finished IO Insertion : Time (s): cpu = 00:00:21 ; elapsed = 00:00:24 . Memory (MB): peak = 1746.887 ; gain = 385.793 ; free physical = 441 ; free virtual = 2257

---------------------------------------------------------------------------------

Report Check Netlist:

+------+------------------+-------+---------+-------+------------------+

| |Item |Errors |Warnings |Status |Description |

+------+------------------+-------+---------+-------+------------------+

|1 |multi\_driven\_nets | 0| 0|Passed |Multi driven nets |

+------+------------------+-------+---------+-------+------------------+

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Start Renaming Generated Instances

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Finished Renaming Generated Instances : Time (s): cpu = 00:00:21 ; elapsed = 00:00:24 . Memory (MB): peak = 1746.887 ; gain = 385.793 ; free physical = 441 ; free virtual = 2257

---------------------------------------------------------------------------------

Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

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Start Rebuilding User Hierarchy

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Finished Rebuilding User Hierarchy : Time (s): cpu = 00:00:21 ; elapsed = 00:00:24 . Memory (MB): peak = 1746.887 ; gain = 385.793 ; free physical = 441 ; free virtual = 2257

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Start Renaming Generated Ports

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Finished Renaming Generated Ports : Time (s): cpu = 00:00:21 ; elapsed = 00:00:24 . Memory (MB): peak = 1746.887 ; gain = 385.793 ; free physical = 441 ; free virtual = 2257

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Start Handling Custom Attributes

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Finished Handling Custom Attributes : Time (s): cpu = 00:00:21 ; elapsed = 00:00:24 . Memory (MB): peak = 1746.887 ; gain = 385.793 ; free physical = 441 ; free virtual = 2257

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Start Renaming Generated Nets

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Finished Renaming Generated Nets : Time (s): cpu = 00:00:21 ; elapsed = 00:00:24 . Memory (MB): peak = 1746.887 ; gain = 385.793 ; free physical = 441 ; free virtual = 2257

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Start Writing Synthesis Report

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Report BlackBoxes:

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| |BlackBox name |Instances |

+-+--------------+----------+

+-+--------------+----------+

Report Cell Usage:

+------+-------+------+

| |Cell |Count |

+------+-------+------+

|1 |BUFG | 2|

|2 |CARRY4 | 168|

|3 |LUT1 | 54|

|4 |LUT2 | 159|

|5 |LUT3 | 320|

|6 |LUT4 | 207|

|7 |LUT5 | 192|

|8 |LUT6 | 363|

|9 |MUXF7 | 17|

|10 |MUXF8 | 5|

|11 |FDRE | 85|

|12 |FDSE | 8|

|13 |IBUF | 5|

|14 |OBUF | 16|

+------+-------+------+

Report Instance Areas:

+------+---------+-------+------+

| |Instance |Module |Cells |

+------+---------+-------+------+

|1 |top | | 1601|

+------+---------+-------+------+

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Finished Writing Synthesis Report : Time (s): cpu = 00:00:21 ; elapsed = 00:00:24 . Memory (MB): peak = 1746.887 ; gain = 385.793 ; free physical = 441 ; free virtual = 2257

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Synthesis finished with 0 errors, 0 critical warnings and 1 warnings.

Synthesis Optimization Runtime : Time (s): cpu = 00:00:17 ; elapsed = 00:00:20 . Memory (MB): peak = 1746.887 ; gain = 51.449 ; free physical = 496 ; free virtual = 2313

Synthesis Optimization Complete : Time (s): cpu = 00:00:21 ; elapsed = 00:00:24 . Memory (MB): peak = 1746.895 ; gain = 385.793 ; free physical = 496 ; free virtual = 2313

INFO: [Project 1-571] Translating synthesized netlist

INFO: [Netlist 29-17] Analyzing 190 Unisim elements for replacement

INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds

WARNING: [Netlist 29-101] Netlist 'Lab07\_movTimer\_2' is not ideal for floorplanning, since the cellview 'Lab07\_movTimer\_2' contains a large number of primitives. Please consider enabling hierarchy in synthesis if you want to do floorplanning.

INFO: [Project 1-570] Preparing netlist for logic optimization

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1746.895 ; gain = 0.000 ; free physical = 437 ; free virtual = 2254

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

INFO: [Common 17-83] Releasing license: Synthesis

51 Infos, 3 Warnings, 0 Critical Warnings and 0 Errors encountered.

synth\_design completed successfully

synth\_design: Time (s): cpu = 00:00:22 ; elapsed = 00:00:25 . Memory (MB): peak = 1746.895 ; gain = 385.875 ; free physical = 492 ; free virtual = 2309

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1746.895 ; gain = 0.000 ; free physical = 492 ; free virtual = 2309

WARNING: [Constraints 18-5210] No constraints selected for write.

Resolution: This message can indicate that there are no constraints for the design, or it can indicate that the used\_in flags are set such that the constraints are ignored. This later case is used when running synth\_design to not write synthesis constraints to the resulting checkpoint. Instead, project constraints are read when the synthesized design is opened.

INFO: [Common 17-1381] The checkpoint '/home/jinson/vivado/Lab07\_movTimer\_2/Lab07\_movTimer\_2.runs/synth\_1/Lab07\_movTimer\_2.dcp' has been generated.

INFO: [runtcl-4] Executing : report\_utilization -file Lab07\_movTimer\_2\_utilization\_synth.rpt -pb Lab07\_movTimer\_2\_utilization\_synth.pb

INFO: [Common 17-206] Exiting Vivado at Thu May 2 17:17:55 2019...