\*\*\* Running vivado

with args -log Lab07\_timer.vdi -applog -m64 -product Vivado -messageDb vivado.pb -mode batch -source Lab07\_timer.tcl -notrace

\*\*\*\*\*\* Vivado v2018.3 (64-bit)

\*\*\*\* SW Build 2405991 on Thu Dec 6 23:36:41 MST 2018

\*\*\*\* IP Build 2404404 on Fri Dec 7 01:43:56 MST 2018

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CRITICAL WARNING: [Common 17-741] No write access right to the local Tcl store at '/home/jinson/.Xilinx/Vivado/2018.3/XilinxTclStore'. XilinxTclStore is reverted to the installation area. If you want to use local Tcl Store, please change the access right and relaunch Vivado.

source Lab07\_timer.tcl -notrace

Command: link\_design -top Lab07\_timer -part xc7a100tcsg324-1

Design is defaulting to srcset: sources\_1

Design is defaulting to constrset: constrs\_1

INFO: [Netlist 29-17] Analyzing 167 Unisim elements for replacement

INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds

WARNING: [Netlist 29-101] Netlist 'Lab07\_timer' is not ideal for floorplanning, since the cellview 'Lab07\_timer' contains a large number of primitives. Please consider enabling hierarchy in synthesis if you want to do floorplanning.

INFO: [Project 1-479] Netlist was created with Vivado 2018.3

INFO: [Device 21-403] Loading part xc7a100tcsg324-1

INFO: [Project 1-570] Preparing netlist for logic optimization

Parsing XDC File [/home/jinson/vivado/Lab07\_timer/Lab07\_timer.srcs/constrs\_1/new/Lab07\_timer.xdc]

Finished Parsing XDC File [/home/jinson/vivado/Lab07\_timer/Lab07\_timer.srcs/constrs\_1/new/Lab07\_timer.xdc]

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1537.609 ; gain = 0.000 ; free physical = 857 ; free virtual = 2406

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

7 Infos, 1 Warnings, 0 Critical Warnings and 0 Errors encountered.

link\_design completed successfully

Command: opt\_design

Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'

INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t'

Running DRC as a precondition to command opt\_design

Starting DRC Task

INFO: [DRC 23-27] Running DRC with 4 threads

INFO: [Project 1-461] DRC finished with 0 Errors

INFO: [Project 1-462] Please refer to the DRC report (report\_drc) for more information.

Time (s): cpu = 00:00:00.93 ; elapsed = 00:00:01 . Memory (MB): peak = 1579.625 ; gain = 38.016 ; free physical = 850 ; free virtual = 2399

Starting Cache Timing Information Task

INFO: [Timing 38-35] Done setting XDC timing constraints.

Ending Cache Timing Information Task | Checksum: 27e7222f

Time (s): cpu = 00:00:06 ; elapsed = 00:00:06 . Memory (MB): peak = 2052.125 ; gain = 472.500 ; free physical = 453 ; free virtual = 2018

Starting Logic Optimization Task

Phase 1 Retarget

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

INFO: [Opt 31-49] Retargeted 0 cell(s).

Phase 1 Retarget | Checksum: 27e7222f

Time (s): cpu = 00:00:00.07 ; elapsed = 00:00:00.06 . Memory (MB): peak = 2130.125 ; gain = 0.000 ; free physical = 384 ; free virtual = 1949

INFO: [Opt 31-389] Phase Retarget created 0 cells and removed 0 cells

Phase 2 Constant propagation

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

Phase 2 Constant propagation | Checksum: 11ecdaa58

Time (s): cpu = 00:00:00.08 ; elapsed = 00:00:00.08 . Memory (MB): peak = 2130.125 ; gain = 0.000 ; free physical = 384 ; free virtual = 1949

INFO: [Opt 31-389] Phase Constant propagation created 0 cells and removed 0 cells

Phase 3 Sweep

Phase 3 Sweep | Checksum: 8269b07b

Time (s): cpu = 00:00:00.11 ; elapsed = 00:00:00.11 . Memory (MB): peak = 2130.125 ; gain = 0.000 ; free physical = 384 ; free virtual = 1949

INFO: [Opt 31-389] Phase Sweep created 0 cells and removed 0 cells

Phase 4 BUFG optimization

Phase 4 BUFG optimization | Checksum: 8269b07b

Time (s): cpu = 00:00:00.13 ; elapsed = 00:00:00.14 . Memory (MB): peak = 2130.125 ; gain = 0.000 ; free physical = 384 ; free virtual = 1949

INFO: [Opt 31-662] Phase BUFG optimization created 0 cells of which 0 are BUFGs and removed 0 cells.

Phase 5 Shift Register Optimization

Phase 5 Shift Register Optimization | Checksum: 770b240f

Time (s): cpu = 00:00:00.25 ; elapsed = 00:00:00.23 . Memory (MB): peak = 2130.125 ; gain = 0.000 ; free physical = 384 ; free virtual = 1949

INFO: [Opt 31-389] Phase Shift Register Optimization created 0 cells and removed 0 cells

Phase 6 Post Processing Netlist

Phase 6 Post Processing Netlist | Checksum: 770b240f

Time (s): cpu = 00:00:00.25 ; elapsed = 00:00:00.24 . Memory (MB): peak = 2130.125 ; gain = 0.000 ; free physical = 384 ; free virtual = 1949

INFO: [Opt 31-389] Phase Post Processing Netlist created 0 cells and removed 0 cells

Opt\_design Change Summary

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-------------------------------------------------------------------------------------------------------------------------

| Phase | #Cells created | #Cells Removed | #Constrained objects preventing optimizations |

-------------------------------------------------------------------------------------------------------------------------

| Retarget | 0 | 0 | 0 |

| Constant propagation | 0 | 0 | 0 |

| Sweep | 0 | 0 | 0 |

| BUFG optimization | 0 | 0 | 0 |

| Shift Register Optimization | 0 | 0 | 0 |

| Post Processing Netlist | 0 | 0 | 0 |

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Starting Connectivity Check Task

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00 . Memory (MB): peak = 2130.125 ; gain = 0.000 ; free physical = 384 ; free virtual = 1949

Ending Logic Optimization Task | Checksum: 770b240f

Time (s): cpu = 00:00:00.26 ; elapsed = 00:00:00.25 . Memory (MB): peak = 2130.125 ; gain = 0.000 ; free physical = 384 ; free virtual = 1949

Starting Power Optimization Task

INFO: [Pwropt 34-132] Skipping clock gating for clocks with a period < 2.00 ns.

Ending Power Optimization Task | Checksum: 770b240f

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.01 . Memory (MB): peak = 2130.125 ; gain = 0.000 ; free physical = 383 ; free virtual = 1949

Starting Final Cleanup Task

Ending Final Cleanup Task | Checksum: 770b240f

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2130.125 ; gain = 0.000 ; free physical = 383 ; free virtual = 1949

Starting Netlist Obfuscation Task

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2130.125 ; gain = 0.000 ; free physical = 383 ; free virtual = 1949

Ending Netlist Obfuscation Task | Checksum: 770b240f

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2130.125 ; gain = 0.000 ; free physical = 383 ; free virtual = 1949

INFO: [Common 17-83] Releasing license: Implementation

23 Infos, 1 Warnings, 0 Critical Warnings and 0 Errors encountered.

opt\_design completed successfully

opt\_design: Time (s): cpu = 00:00:08 ; elapsed = 00:00:09 . Memory (MB): peak = 2130.125 ; gain = 588.516 ; free physical = 383 ; free virtual = 1949

Netlist sorting complete. Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00 . Memory (MB): peak = 2130.125 ; gain = 0.000 ; free physical = 383 ; free virtual = 1949

INFO: [Timing 38-480] Writing timing data to binary archive.

Writing placer database...

Writing XDEF routing.

Writing XDEF routing logical nets.

Writing XDEF routing special nets.

Write XDEF Complete: Time (s): cpu = 00:00:00.03 ; elapsed = 00:00:00 . Memory (MB): peak = 2162.141 ; gain = 0.000 ; free physical = 380 ; free virtual = 1946

Netlist sorting complete. Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00 . Memory (MB): peak = 2162.141 ; gain = 0.000 ; free physical = 379 ; free virtual = 1945

INFO: [Common 17-1381] The checkpoint '/home/jinson/vivado/Lab07\_timer/Lab07\_timer.runs/impl\_1/Lab07\_timer\_opt.dcp' has been generated.

INFO: [runtcl-4] Executing : report\_drc -file Lab07\_timer\_drc\_opted.rpt -pb Lab07\_timer\_drc\_opted.pb -rpx Lab07\_timer\_drc\_opted.rpx

Command: report\_drc -file Lab07\_timer\_drc\_opted.rpt -pb Lab07\_timer\_drc\_opted.pb -rpx Lab07\_timer\_drc\_opted.rpx

INFO: [IP\_Flow 19-234] Refreshing IP repositories

INFO: [IP\_Flow 19-1704] No user IP repositories specified

INFO: [IP\_Flow 19-2313] Loaded Vivado IP repository '/tools/Xilinx/Vivado/2018.3/data/ip'.

INFO: [DRC 23-27] Running DRC with 4 threads

INFO: [Coretcl 2-168] The results of DRC are in file /home/jinson/vivado/Lab07\_timer/Lab07\_timer.runs/impl\_1/Lab07\_timer\_drc\_opted.rpt.

report\_drc completed successfully

Command: place\_design

Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'

INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t'

INFO: [DRC 23-27] Running DRC with 4 threads

INFO: [Vivado\_Tcl 4-198] DRC finished with 0 Errors

INFO: [Vivado\_Tcl 4-199] Please refer to the DRC report (report\_drc) for more information.

Running DRC as a precondition to command place\_design

INFO: [DRC 23-27] Running DRC with 4 threads

INFO: [Vivado\_Tcl 4-198] DRC finished with 0 Errors

INFO: [Vivado\_Tcl 4-199] Please refer to the DRC report (report\_drc) for more information.

Starting Placer Task

INFO: [Place 30-611] Multithreading enabled for place\_design using a maximum of 4 CPUs

Phase 1 Placer Initialization

Phase 1.1 Placer Initialization Netlist Sorting

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2218.168 ; gain = 0.000 ; free physical = 335 ; free virtual = 1916

Phase 1.1 Placer Initialization Netlist Sorting | Checksum: 5e619d66

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.01 . Memory (MB): peak = 2218.168 ; gain = 0.000 ; free physical = 335 ; free virtual = 1916

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2218.168 ; gain = 0.000 ; free physical = 335 ; free virtual = 1916

Phase 1.2 IO Placement/ Clock Placement/ Build Placer Device

INFO: [Timing 38-35] Done setting XDC timing constraints.

Phase 1.2 IO Placement/ Clock Placement/ Build Placer Device | Checksum: 1925db418

Time (s): cpu = 00:00:00.77 ; elapsed = 00:00:00.58 . Memory (MB): peak = 2218.168 ; gain = 0.000 ; free physical = 313 ; free virtual = 1897

Phase 1.3 Build Placer Netlist Model

Phase 1.3 Build Placer Netlist Model | Checksum: 2650d5df1

Time (s): cpu = 00:00:00.86 ; elapsed = 00:00:00.66 . Memory (MB): peak = 2218.168 ; gain = 0.000 ; free physical = 312 ; free virtual = 1897

Phase 1.4 Constrain Clocks/Macros

Phase 1.4 Constrain Clocks/Macros | Checksum: 2650d5df1

Time (s): cpu = 00:00:00.86 ; elapsed = 00:00:00.66 . Memory (MB): peak = 2218.168 ; gain = 0.000 ; free physical = 312 ; free virtual = 1897

Phase 1 Placer Initialization | Checksum: 2650d5df1

Time (s): cpu = 00:00:00.86 ; elapsed = 00:00:00.67 . Memory (MB): peak = 2218.168 ; gain = 0.000 ; free physical = 312 ; free virtual = 1897

Phase 2 Global Placement

Phase 2.1 Floorplanning

Phase 2.1 Floorplanning | Checksum: 2650d5df1

Time (s): cpu = 00:00:00.87 ; elapsed = 00:00:00.68 . Memory (MB): peak = 2218.168 ; gain = 0.000 ; free physical = 309 ; free virtual = 1895

WARNING: [Place 46-29] place\_design is not in timing mode. Skip physical synthesis in placer

Phase 2 Global Placement | Checksum: 27c16452c

Time (s): cpu = 00:00:02 ; elapsed = 00:00:01 . Memory (MB): peak = 2218.168 ; gain = 0.000 ; free physical = 297 ; free virtual = 1884

Phase 3 Detail Placement

Phase 3.1 Commit Multi Column Macros

Phase 3.1 Commit Multi Column Macros | Checksum: 27c16452c

Time (s): cpu = 00:00:02 ; elapsed = 00:00:01 . Memory (MB): peak = 2218.168 ; gain = 0.000 ; free physical = 297 ; free virtual = 1884

Phase 3.2 Commit Most Macros & LUTRAMs

Phase 3.2 Commit Most Macros & LUTRAMs | Checksum: 1ed843cf1

Time (s): cpu = 00:00:03 ; elapsed = 00:00:02 . Memory (MB): peak = 2218.168 ; gain = 0.000 ; free physical = 296 ; free virtual = 1883

Phase 3.3 Area Swap Optimization

Phase 3.3 Area Swap Optimization | Checksum: 2529c5ff6

Time (s): cpu = 00:00:03 ; elapsed = 00:00:02 . Memory (MB): peak = 2218.168 ; gain = 0.000 ; free physical = 296 ; free virtual = 1883

Phase 3.4 Pipeline Register Optimization

Phase 3.4 Pipeline Register Optimization | Checksum: 2529c5ff6

Time (s): cpu = 00:00:03 ; elapsed = 00:00:02 . Memory (MB): peak = 2218.168 ; gain = 0.000 ; free physical = 296 ; free virtual = 1883

Phase 3.5 Small Shape Detail Placement

Phase 3.5 Small Shape Detail Placement | Checksum: 210314744

Time (s): cpu = 00:00:03 ; elapsed = 00:00:02 . Memory (MB): peak = 2218.168 ; gain = 0.000 ; free physical = 292 ; free virtual = 1880

Phase 3.6 Re-assign LUT pins

Phase 3.6 Re-assign LUT pins | Checksum: 210314744

Time (s): cpu = 00:00:03 ; elapsed = 00:00:02 . Memory (MB): peak = 2218.168 ; gain = 0.000 ; free physical = 292 ; free virtual = 1880

Phase 3.7 Pipeline Register Optimization

Phase 3.7 Pipeline Register Optimization | Checksum: 210314744

Time (s): cpu = 00:00:03 ; elapsed = 00:00:02 . Memory (MB): peak = 2218.168 ; gain = 0.000 ; free physical = 292 ; free virtual = 1880

Phase 3 Detail Placement | Checksum: 210314744

Time (s): cpu = 00:00:03 ; elapsed = 00:00:02 . Memory (MB): peak = 2218.168 ; gain = 0.000 ; free physical = 292 ; free virtual = 1880

Phase 4 Post Placement Optimization and Clean-Up

Phase 4.1 Post Commit Optimization

Phase 4.1 Post Commit Optimization | Checksum: 210314744

Time (s): cpu = 00:00:03 ; elapsed = 00:00:02 . Memory (MB): peak = 2218.168 ; gain = 0.000 ; free physical = 292 ; free virtual = 1880

Phase 4.2 Post Placement Cleanup

Phase 4.2 Post Placement Cleanup | Checksum: 210314744

Time (s): cpu = 00:00:03 ; elapsed = 00:00:02 . Memory (MB): peak = 2218.168 ; gain = 0.000 ; free physical = 294 ; free virtual = 1882

Phase 4.3 Placer Reporting

Phase 4.3 Placer Reporting | Checksum: 210314744

Time (s): cpu = 00:00:03 ; elapsed = 00:00:02 . Memory (MB): peak = 2218.168 ; gain = 0.000 ; free physical = 294 ; free virtual = 1882

Phase 4.4 Final Placement Cleanup

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2218.168 ; gain = 0.000 ; free physical = 294 ; free virtual = 1882

Phase 4.4 Final Placement Cleanup | Checksum: 20402bac9

Time (s): cpu = 00:00:03 ; elapsed = 00:00:02 . Memory (MB): peak = 2218.168 ; gain = 0.000 ; free physical = 294 ; free virtual = 1882

Phase 4 Post Placement Optimization and Clean-Up | Checksum: 20402bac9

Time (s): cpu = 00:00:03 ; elapsed = 00:00:02 . Memory (MB): peak = 2218.168 ; gain = 0.000 ; free physical = 294 ; free virtual = 1882

Ending Placer Task | Checksum: 1672792ed

Time (s): cpu = 00:00:03 ; elapsed = 00:00:02 . Memory (MB): peak = 2218.168 ; gain = 0.000 ; free physical = 305 ; free virtual = 1893

INFO: [Common 17-83] Releasing license: Implementation

41 Infos, 2 Warnings, 0 Critical Warnings and 0 Errors encountered.

place\_design completed successfully

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2218.168 ; gain = 0.000 ; free physical = 305 ; free virtual = 1893

INFO: [Timing 38-480] Writing timing data to binary archive.

Writing placer database...

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2218.168 ; gain = 0.000 ; free physical = 303 ; free virtual = 1892

Writing XDEF routing.

Writing XDEF routing logical nets.

Writing XDEF routing special nets.

Write XDEF Complete: Time (s): cpu = 00:00:00.27 ; elapsed = 00:00:00.09 . Memory (MB): peak = 2218.168 ; gain = 0.000 ; free physical = 298 ; free virtual = 1889

INFO: [Common 17-1381] The checkpoint '/home/jinson/vivado/Lab07\_timer/Lab07\_timer.runs/impl\_1/Lab07\_timer\_placed.dcp' has been generated.

INFO: [runtcl-4] Executing : report\_io -file Lab07\_timer\_io\_placed.rpt

report\_io: Time (s): cpu = 00:00:00.09 ; elapsed = 00:00:00.15 . Memory (MB): peak = 2218.168 ; gain = 0.000 ; free physical = 297 ; free virtual = 1885

INFO: [runtcl-4] Executing : report\_utilization -file Lab07\_timer\_utilization\_placed.rpt -pb Lab07\_timer\_utilization\_placed.pb

INFO: [runtcl-4] Executing : report\_control\_sets -verbose -file Lab07\_timer\_control\_sets\_placed.rpt

report\_control\_sets: Time (s): cpu = 00:00:00.05 ; elapsed = 00:00:00.09 . Memory (MB): peak = 2218.168 ; gain = 0.000 ; free physical = 304 ; free virtual = 1893

Command: route\_design

Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'

INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t'

Running DRC as a precondition to command route\_design

INFO: [DRC 23-27] Running DRC with 4 threads

INFO: [Vivado\_Tcl 4-198] DRC finished with 0 Errors

INFO: [Vivado\_Tcl 4-199] Please refer to the DRC report (report\_drc) for more information.

Starting Routing Task

INFO: [Route 35-254] Multithreading enabled for route\_design using a maximum of 4 CPUs

Checksum: PlaceDB: d4b48312 ConstDB: 0 ShapeSum: 92730fdb RouteDB: 0

Phase 1 Build RT Design

Phase 1 Build RT Design | Checksum: 1977f345c

Time (s): cpu = 00:00:23 ; elapsed = 00:00:19 . Memory (MB): peak = 2322.203 ; gain = 104.035 ; free physical = 154 ; free virtual = 1743

Post Restoration Checksum: NetGraph: dda9a974 NumContArr: b9d58ae8 Constraints: 0 Timing: 0

Phase 2 Router Initialization

INFO: [Route 35-64] No timing constraints were detected. The router will operate in resource-optimization mode.

Phase 2.1 Fix Topology Constraints

Phase 2.1 Fix Topology Constraints | Checksum: 1977f345c

Time (s): cpu = 00:00:23 ; elapsed = 00:00:19 . Memory (MB): peak = 2329.199 ; gain = 111.031 ; free physical = 138 ; free virtual = 1728

Phase 2.2 Pre Route Cleanup

Phase 2.2 Pre Route Cleanup | Checksum: 1977f345c

Time (s): cpu = 00:00:23 ; elapsed = 00:00:19 . Memory (MB): peak = 2329.199 ; gain = 111.031 ; free physical = 138 ; free virtual = 1728

Number of Nodes with overlaps = 0

Phase 2 Router Initialization | Checksum: eb0bdfd0

Time (s): cpu = 00:00:23 ; elapsed = 00:00:19 . Memory (MB): peak = 2337.465 ; gain = 119.297 ; free physical = 128 ; free virtual = 1719

Phase 3 Initial Routing

Phase 3 Initial Routing | Checksum: 14ca97d2d

Time (s): cpu = 00:00:24 ; elapsed = 00:00:20 . Memory (MB): peak = 2341.312 ; gain = 123.145 ; free physical = 127 ; free virtual = 1718

Phase 4 Rip-up And Reroute

Phase 4.1 Global Iteration 0

Number of Nodes with overlaps = 104

Number of Nodes with overlaps = 0

Phase 4.1 Global Iteration 0 | Checksum: 6b7ba009

Time (s): cpu = 00:00:24 ; elapsed = 00:00:20 . Memory (MB): peak = 2341.312 ; gain = 123.145 ; free physical = 127 ; free virtual = 1718

Phase 4 Rip-up And Reroute | Checksum: 6b7ba009

Time (s): cpu = 00:00:24 ; elapsed = 00:00:20 . Memory (MB): peak = 2341.312 ; gain = 123.145 ; free physical = 127 ; free virtual = 1718

Phase 5 Delay and Skew Optimization

Phase 5 Delay and Skew Optimization | Checksum: 6b7ba009

Time (s): cpu = 00:00:24 ; elapsed = 00:00:20 . Memory (MB): peak = 2341.312 ; gain = 123.145 ; free physical = 127 ; free virtual = 1718

Phase 6 Post Hold Fix

Phase 6.1 Hold Fix Iter

Phase 6.1 Hold Fix Iter | Checksum: 6b7ba009

Time (s): cpu = 00:00:24 ; elapsed = 00:00:20 . Memory (MB): peak = 2341.312 ; gain = 123.145 ; free physical = 127 ; free virtual = 1718

Phase 6 Post Hold Fix | Checksum: 6b7ba009

Time (s): cpu = 00:00:24 ; elapsed = 00:00:20 . Memory (MB): peak = 2341.312 ; gain = 123.145 ; free physical = 127 ; free virtual = 1718

Phase 7 Route finalize

Router Utilization Summary

Global Vertical Routing Utilization = 0.147365 %

Global Horizontal Routing Utilization = 0.184001 %

Routable Net Status\*

\*Does not include unroutable nets such as driverless and loadless.

Run report\_route\_status for detailed report.

Number of Failed Nets = 0

Number of Unrouted Nets = 0

Number of Partially Routed Nets = 0

Number of Node Overlaps = 0

Congestion Report

North Dir 1x1 Area, Max Cong = 15.3153%, No Congested Regions.

South Dir 1x1 Area, Max Cong = 31.5315%, No Congested Regions.

East Dir 1x1 Area, Max Cong = 35.2941%, No Congested Regions.

West Dir 1x1 Area, Max Cong = 33.8235%, No Congested Regions.

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Reporting congestion hotspots

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Direction: North

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Congested clusters found at Level 0

Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0

Direction: South

----------------

Congested clusters found at Level 0

Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0

Direction: East

----------------

Congested clusters found at Level 0

Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0

Direction: West

----------------

Congested clusters found at Level 0

Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0

Phase 7 Route finalize | Checksum: 6b7ba009

Time (s): cpu = 00:00:24 ; elapsed = 00:00:20 . Memory (MB): peak = 2341.312 ; gain = 123.145 ; free physical = 127 ; free virtual = 1718

Phase 8 Verifying routed nets

Verification completed successfully

Phase 8 Verifying routed nets | Checksum: 6b7ba009

Time (s): cpu = 00:00:24 ; elapsed = 00:00:20 . Memory (MB): peak = 2341.312 ; gain = 123.145 ; free physical = 126 ; free virtual = 1717

Phase 9 Depositing Routes

Phase 9 Depositing Routes | Checksum: 976e518a

Time (s): cpu = 00:00:24 ; elapsed = 00:00:20 . Memory (MB): peak = 2341.312 ; gain = 123.145 ; free physical = 126 ; free virtual = 1717

INFO: [Route 35-16] Router Completed Successfully

Time (s): cpu = 00:00:24 ; elapsed = 00:00:20 . Memory (MB): peak = 2341.312 ; gain = 123.145 ; free physical = 145 ; free virtual = 1736

Routing Is Done.

INFO: [Common 17-83] Releasing license: Implementation

54 Infos, 2 Warnings, 0 Critical Warnings and 0 Errors encountered.

route\_design completed successfully

route\_design: Time (s): cpu = 00:00:26 ; elapsed = 00:00:21 . Memory (MB): peak = 2341.312 ; gain = 123.145 ; free physical = 145 ; free virtual = 1736

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2341.312 ; gain = 0.000 ; free physical = 145 ; free virtual = 1736

INFO: [Timing 38-480] Writing timing data to binary archive.

Writing placer database...

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2341.312 ; gain = 0.000 ; free physical = 141 ; free virtual = 1733

Writing XDEF routing.

Writing XDEF routing logical nets.

Writing XDEF routing special nets.

Write XDEF Complete: Time (s): cpu = 00:00:00.23 ; elapsed = 00:00:00.07 . Memory (MB): peak = 2341.312 ; gain = 0.000 ; free physical = 138 ; free virtual = 1731

INFO: [Common 17-1381] The checkpoint '/home/jinson/vivado/Lab07\_timer/Lab07\_timer.runs/impl\_1/Lab07\_timer\_routed.dcp' has been generated.

INFO: [runtcl-4] Executing : report\_drc -file Lab07\_timer\_drc\_routed.rpt -pb Lab07\_timer\_drc\_routed.pb -rpx Lab07\_timer\_drc\_routed.rpx

Command: report\_drc -file Lab07\_timer\_drc\_routed.rpt -pb Lab07\_timer\_drc\_routed.pb -rpx Lab07\_timer\_drc\_routed.rpx

INFO: [IP\_Flow 19-1839] IP Catalog is up to date.

INFO: [DRC 23-27] Running DRC with 4 threads

INFO: [Coretcl 2-168] The results of DRC are in file /home/jinson/vivado/Lab07\_timer/Lab07\_timer.runs/impl\_1/Lab07\_timer\_drc\_routed.rpt.

report\_drc completed successfully

INFO: [runtcl-4] Executing : report\_methodology -file Lab07\_timer\_methodology\_drc\_routed.rpt -pb Lab07\_timer\_methodology\_drc\_routed.pb -rpx Lab07\_timer\_methodology\_drc\_routed.rpx

Command: report\_methodology -file Lab07\_timer\_methodology\_drc\_routed.rpt -pb Lab07\_timer\_methodology\_drc\_routed.pb -rpx Lab07\_timer\_methodology\_drc\_routed.rpx

INFO: [Timing 38-35] Done setting XDC timing constraints.

INFO: [DRC 23-133] Running Methodology with 4 threads

INFO: [Coretcl 2-1520] The results of Report Methodology are in file /home/jinson/vivado/Lab07\_timer/Lab07\_timer.runs/impl\_1/Lab07\_timer\_methodology\_drc\_routed.rpt.

report\_methodology completed successfully

INFO: [runtcl-4] Executing : report\_power -file Lab07\_timer\_power\_routed.rpt -pb Lab07\_timer\_power\_summary\_routed.pb -rpx Lab07\_timer\_power\_routed.rpx

Command: report\_power -file Lab07\_timer\_power\_routed.rpt -pb Lab07\_timer\_power\_summary\_routed.pb -rpx Lab07\_timer\_power\_routed.rpx

WARNING: [Power 33-232] No user defined clocks were found in the design!

Resolution: Please specify clocks using create\_clock/create\_generated\_clock for sequential elements. For pure combinatorial circuits, please specify a virtual clock, otherwise the vectorless estimation might be inaccurate

INFO: [Timing 38-35] Done setting XDC timing constraints.

Running Vector-less Activity Propagation...

Finished Running Vector-less Activity Propagation

66 Infos, 3 Warnings, 0 Critical Warnings and 0 Errors encountered.

report\_power completed successfully

INFO: [runtcl-4] Executing : report\_route\_status -file Lab07\_timer\_route\_status.rpt -pb Lab07\_timer\_route\_status.pb

INFO: [runtcl-4] Executing : report\_timing\_summary -max\_paths 10 -file Lab07\_timer\_timing\_summary\_routed.rpt -pb Lab07\_timer\_timing\_summary\_routed.pb -rpx Lab07\_timer\_timing\_summary\_routed.rpx -warn\_on\_violation

INFO: [Timing 38-91] UpdateTimingParams: Speed grade: -1, Delay Type: min\_max.

INFO: [Timing 38-191] Multithreading enabled for timing update using a maximum of 4 CPUs

WARNING: [Timing 38-313] There are no user specified timing constraints. Timing constraints are needed for proper timing analysis.

INFO: [runtcl-4] Executing : report\_incremental\_reuse -file Lab07\_timer\_incremental\_reuse\_routed.rpt

INFO: [Vivado\_Tcl 4-1062] Incremental flow is disabled. No incremental reuse Info to report.

INFO: [runtcl-4] Executing : report\_clock\_utilization -file Lab07\_timer\_clock\_utilization\_routed.rpt

INFO: [runtcl-4] Executing : report\_bus\_skew -warn\_on\_violation -file Lab07\_timer\_bus\_skew\_routed.rpt -pb Lab07\_timer\_bus\_skew\_routed.pb -rpx Lab07\_timer\_bus\_skew\_routed.rpx

INFO: [Timing 38-91] UpdateTimingParams: Speed grade: -1, Delay Type: min\_max.

INFO: [Timing 38-191] Multithreading enabled for timing update using a maximum of 4 CPUs

INFO: [Common 17-206] Exiting Vivado at Thu May 2 17:36:41 2019...

\*\*\* Running vivado

with args -log Lab07\_timer.vdi -applog -m64 -product Vivado -messageDb vivado.pb -mode batch -source Lab07\_timer.tcl -notrace

\*\*\*\*\*\* Vivado v2018.3 (64-bit)

\*\*\*\* SW Build 2405991 on Thu Dec 6 23:36:41 MST 2018

\*\*\*\* IP Build 2404404 on Fri Dec 7 01:43:56 MST 2018

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CRITICAL WARNING: [Common 17-741] No write access right to the local Tcl store at '/home/jinson/.Xilinx/Vivado/2018.3/XilinxTclStore'. XilinxTclStore is reverted to the installation area. If you want to use local Tcl Store, please change the access right and relaunch Vivado.

source Lab07\_timer.tcl -notrace

Command: open\_checkpoint Lab07\_timer\_routed.dcp

Starting open\_checkpoint Task

Time (s): cpu = 00:00:00.02 ; elapsed = 00:00:00.07 . Memory (MB): peak = 1382.262 ; gain = 0.000 ; free physical = 1127 ; free virtual = 2677

INFO: [Netlist 29-17] Analyzing 167 Unisim elements for replacement

INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds

WARNING: [Netlist 29-101] Netlist 'Lab07\_timer' is not ideal for floorplanning, since the cellview 'Lab07\_timer' contains a large number of primitives. Please consider enabling hierarchy in synthesis if you want to do floorplanning.

INFO: [Project 1-479] Netlist was created with Vivado 2018.3

INFO: [Device 21-403] Loading part xc7a100tcsg324-1

INFO: [Project 1-570] Preparing netlist for logic optimization

INFO: [Timing 38-478] Restoring timing data from binary archive.

INFO: [Timing 38-479] Binary timing data restore complete.

INFO: [Project 1-856] Restoring constraints from binary archive.

INFO: [Project 1-853] Binary constraint restore complete.

Reading XDEF placement.

Reading placer database...

Reading XDEF routing.

Read XDEF File: Time (s): cpu = 00:00:00.15 ; elapsed = 00:00:00.20 . Memory (MB): peak = 2030.258 ; gain = 0.000 ; free physical = 401 ; free virtual = 1951

Restored from archive | CPU: 0.190000 secs | Memory: 2.427315 MB |

Finished XDEF File Restore: Time (s): cpu = 00:00:00.15 ; elapsed = 00:00:00.20 . Memory (MB): peak = 2030.258 ; gain = 0.000 ; free physical = 401 ; free virtual = 1951

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2030.258 ; gain = 0.000 ; free physical = 400 ; free virtual = 1951

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

INFO: [Project 1-604] Checkpoint was created with Vivado v2018.3 (64-bit) build 2405991

open\_checkpoint: Time (s): cpu = 00:00:10 ; elapsed = 00:00:11 . Memory (MB): peak = 2030.258 ; gain = 647.996 ; free physical = 399 ; free virtual = 1950

Command: write\_bitstream -force Lab07\_timer.bit

Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'

INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t'

Running DRC as a precondition to command write\_bitstream

INFO: [IP\_Flow 19-234] Refreshing IP repositories

INFO: [IP\_Flow 19-1704] No user IP repositories specified

INFO: [IP\_Flow 19-2313] Loaded Vivado IP repository '/tools/Xilinx/Vivado/2018.3/data/ip'.

INFO: [DRC 23-27] Running DRC with 4 threads

WARNING: [DRC CFGBVS-1] Missing CFGBVS and CONFIG\_VOLTAGE Design Properties: Neither the CFGBVS nor CONFIG\_VOLTAGE voltage property is set in the current\_design. Configuration bank voltage select (CFGBVS) must be set to VCCO or GND, and CONFIG\_VOLTAGE must be set to the correct configuration voltage, in order to determine the I/O voltage support for the pins in bank 0. It is suggested to specify these either using the 'Edit Device Properties' function in the GUI or directly in the XDC file using the following syntax:

set\_property CFGBVS value1 [current\_design]

#where value1 is either VCCO or GND

set\_property CONFIG\_VOLTAGE value2 [current\_design]

#where value2 is the voltage provided to configuration bank 0

Refer to the device configuration user guide for more information.

INFO: [Vivado 12-3199] DRC finished with 0 Errors, 1 Warnings

INFO: [Vivado 12-3200] Please refer to the DRC report (report\_drc) for more information.

INFO: [Designutils 20-2272] Running write\_bitstream with 4 threads.

Loading data files...

Loading site data...

Loading route data...

Processing options...

Creating bitmap...

Creating bitstream...

Bitstream compression saved 26540672 bits.

Writing bitstream ./Lab07\_timer.bit...

INFO: [Vivado 12-1842] Bitgen Completed Successfully.

INFO: [Project 1-120] WebTalk data collection is mandatory when using a WebPACK part without a full Vivado license. To see the specific WebTalk data collected for your design, open the usage\_statistics\_webtalk.html or usage\_statistics\_webtalk.xml file in the implementation directory.

CRITICAL WARNING: [Common 17-570] Unable to write the webtalk settings file. Please check that the appropriate environment variable (APPDATA or HOME) is properly set.

CRITICAL WARNING: [Common 17-570] Unable to write the webtalk settings file. Please check that the appropriate environment variable (APPDATA or HOME) is properly set.

INFO: [Common 17-186] '/home/jinson/vivado/Lab07\_timer/Lab07\_timer.runs/impl\_1/usage\_statistics\_webtalk.xml' has been successfully sent to Xilinx on Thu May 2 17:37:24 2019. For additional details about this file, please refer to the WebTalk help file at /tools/Xilinx/Vivado/2018.3/doc/webtalk\_introduction.html.

INFO: [Common 17-83] Releasing license: Implementation

23 Infos, 2 Warnings, 2 Critical Warnings and 0 Errors encountered.

write\_bitstream completed successfully

write\_bitstream: Time (s): cpu = 00:00:10 ; elapsed = 00:00:15 . Memory (MB): peak = 2476.094 ; gain = 445.836 ; free physical = 445 ; free virtual = 1891

INFO: [Common 17-206] Exiting Vivado at Thu May 2 17:37:24 2019...