\*\*\* Running vivado

with args -log Lab07\_timer.vds -m64 -product Vivado -mode batch -messageDb vivado.pb -notrace -source Lab07\_timer.tcl

\*\*\*\*\*\* Vivado v2018.3 (64-bit)

\*\*\*\* SW Build 2405991 on Thu Dec 6 23:36:41 MST 2018

\*\*\*\* IP Build 2404404 on Fri Dec 7 01:43:56 MST 2018

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CRITICAL WARNING: [Common 17-741] No write access right to the local Tcl store at '/home/jinson/.Xilinx/Vivado/2018.3/XilinxTclStore'. XilinxTclStore is reverted to the installation area. If you want to use local Tcl Store, please change the access right and relaunch Vivado.

source Lab07\_timer.tcl -notrace

Command: synth\_design -top Lab07\_timer -part xc7a100tcsg324-1

Starting synth\_design

Attempting to get a license for feature 'Synthesis' and/or device 'xc7a100t'

INFO: [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a100t'

INFO: Launching helper process for spawning children vivado processes

INFO: Helper process launched with PID 97046

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Starting RTL Elaboration : Time (s): cpu = 00:00:02 ; elapsed = 00:00:02 . Memory (MB): peak = 1362.086 ; gain = 0.000 ; free physical = 1021 ; free virtual = 2564

---------------------------------------------------------------------------------

INFO: [Synth 8-6157] synthesizing module 'Lab07\_timer' [/home/jinson/vivado/Lab07\_timer/Lab07\_timer.srcs/sources\_1/new/Lab07\_timer.sv:23]

INFO: [Synth 8-6155] done synthesizing module 'Lab07\_timer' (1#1) [/home/jinson/vivado/Lab07\_timer/Lab07\_timer.srcs/sources\_1/new/Lab07\_timer.sv:23]

WARNING: [Synth 8-3917] design Lab07\_timer has port dp driven by constant 1

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Finished RTL Elaboration : Time (s): cpu = 00:00:02 ; elapsed = 00:00:03 . Memory (MB): peak = 1386.512 ; gain = 24.426 ; free physical = 1031 ; free virtual = 2576

---------------------------------------------------------------------------------

Report Check Netlist:

+------+------------------+-------+---------+-------+------------------+

| |Item |Errors |Warnings |Status |Description |

+------+------------------+-------+---------+-------+------------------+

|1 |multi\_driven\_nets | 0| 0|Passed |Multi driven nets |

+------+------------------+-------+---------+-------+------------------+

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Start Handling Custom Attributes

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Finished Handling Custom Attributes : Time (s): cpu = 00:00:02 ; elapsed = 00:00:03 . Memory (MB): peak = 1386.512 ; gain = 24.426 ; free physical = 1031 ; free virtual = 2576

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Finished RTL Optimization Phase 1 : Time (s): cpu = 00:00:02 ; elapsed = 00:00:03 . Memory (MB): peak = 1386.512 ; gain = 24.426 ; free physical = 1031 ; free virtual = 2576

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INFO: [Device 21-403] Loading part xc7a100tcsg324-1

INFO: [Project 1-570] Preparing netlist for logic optimization

Processing XDC Constraints

Initializing timing engine

Parsing XDC File [/home/jinson/vivado/Lab07\_timer/Lab07\_timer.srcs/constrs\_1/new/Lab07\_timer.xdc]

Finished Parsing XDC File [/home/jinson/vivado/Lab07\_timer/Lab07\_timer.srcs/constrs\_1/new/Lab07\_timer.xdc]

INFO: [Project 1-236] Implementation specific constraints were found while reading constraint file [/home/jinson/vivado/Lab07\_timer/Lab07\_timer.srcs/constrs\_1/new/Lab07\_timer.xdc]. These constraints will be ignored for synthesis but will be used in implementation. Impacted constraints are listed in the file [.Xil/Lab07\_timer\_propImpl.xdc].

Resolution: To avoid this warning, move constraints listed in [.Xil/Lab07\_timer\_propImpl.xdc] to another XDC file and exclude this new file from synthesis with the used\_in\_synthesis property (File Properties dialog in GUI) and re-run elaboration/synthesis.

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1720.863 ; gain = 0.000 ; free physical = 773 ; free virtual = 2319

Completed Processing XDC Constraints

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1720.863 ; gain = 0.000 ; free physical = 774 ; free virtual = 2319

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1720.863 ; gain = 0.000 ; free physical = 774 ; free virtual = 2319

Constraint Validation Runtime : Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1720.863 ; gain = 0.000 ; free physical = 774 ; free virtual = 2319

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Finished Constraint Validation : Time (s): cpu = 00:00:07 ; elapsed = 00:00:09 . Memory (MB): peak = 1720.863 ; gain = 358.777 ; free physical = 843 ; free virtual = 2389

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Start Loading Part and Timing Information

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Loading part: xc7a100tcsg324-1

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Finished Loading Part and Timing Information : Time (s): cpu = 00:00:07 ; elapsed = 00:00:09 . Memory (MB): peak = 1720.863 ; gain = 358.777 ; free physical = 843 ; free virtual = 2389

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---------------------------------------------------------------------------------

Start Applying 'set\_property' XDC Constraints

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Finished applying 'set\_property' XDC Constraints : Time (s): cpu = 00:00:07 ; elapsed = 00:00:09 . Memory (MB): peak = 1720.863 ; gain = 358.777 ; free physical = 845 ; free virtual = 2391

---------------------------------------------------------------------------------

INFO: [Synth 8-5545] ROM "timer" won't be mapped to RAM because address size (32) is larger than maximum supported(25)

INFO: [Synth 8-5546] ROM "b" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5545] ROM "timer" won't be mapped to RAM because address size (32) is larger than maximum supported(25)

INFO: [Synth 8-5546] ROM "b" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5544] ROM "an" won't be mapped to Block RAM because address size (3) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "timer" won't be mapped to Block RAM because address size (1) smaller than threshold (5)

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Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:08 ; elapsed = 00:00:10 . Memory (MB): peak = 1720.863 ; gain = 358.777 ; free physical = 835 ; free virtual = 2381

---------------------------------------------------------------------------------

Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

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Start RTL Component Statistics

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Detailed RTL Component Info :

+---Adders :

2 Input 8 Bit Adders := 1

2 Input 3 Bit Adders := 1

+---Registers :

8 Bit Registers := 2

7 Bit Registers := 1

3 Bit Registers := 1

+---Muxes :

8 Input 8 Bit Muxes := 1

2 Input 8 Bit Muxes := 1

6 Input 7 Bit Muxes := 2

10 Input 7 Bit Muxes := 2

3 Input 7 Bit Muxes := 1

3 Input 1 Bit Muxes := 1

---------------------------------------------------------------------------------

Finished RTL Component Statistics

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---------------------------------------------------------------------------------

Start RTL Hierarchical Component Statistics

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Hierarchical RTL Component report

Module Lab07\_timer

Detailed RTL Component Info :

+---Adders :

2 Input 8 Bit Adders := 1

2 Input 3 Bit Adders := 1

+---Registers :

8 Bit Registers := 2

7 Bit Registers := 1

3 Bit Registers := 1

+---Muxes :

8 Input 8 Bit Muxes := 1

2 Input 8 Bit Muxes := 1

6 Input 7 Bit Muxes := 2

10 Input 7 Bit Muxes := 2

3 Input 7 Bit Muxes := 1

3 Input 1 Bit Muxes := 1

---------------------------------------------------------------------------------

Finished RTL Hierarchical Component Statistics

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Start Part Resource Summary

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Part Resources:

DSPs: 240 (col length:80)

BRAMs: 270 (col length: RAMB18 80 RAMB36 40)

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Finished Part Resource Summary

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Start Cross Boundary and Area Optimization

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Warning: Parallel synthesis criteria is not met

WARNING: [Synth 8-3917] design Lab07\_timer has port dp driven by constant 1

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Finished Cross Boundary and Area Optimization : Time (s): cpu = 00:00:12 ; elapsed = 00:00:14 . Memory (MB): peak = 1720.863 ; gain = 358.777 ; free physical = 807 ; free virtual = 2357

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Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

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Start Applying XDC Timing Constraints

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Finished Applying XDC Timing Constraints : Time (s): cpu = 00:00:16 ; elapsed = 00:00:19 . Memory (MB): peak = 1720.863 ; gain = 358.777 ; free physical = 686 ; free virtual = 2236

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Start Timing Optimization

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Finished Timing Optimization : Time (s): cpu = 00:00:16 ; elapsed = 00:00:19 . Memory (MB): peak = 1720.863 ; gain = 358.777 ; free physical = 686 ; free virtual = 2236

---------------------------------------------------------------------------------

Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

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Start Technology Mapping

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Finished Technology Mapping : Time (s): cpu = 00:00:17 ; elapsed = 00:00:19 . Memory (MB): peak = 1720.863 ; gain = 358.777 ; free physical = 683 ; free virtual = 2233

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Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

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Start IO Insertion

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Start Flattening Before IO Insertion

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Finished Flattening Before IO Insertion

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---------------------------------------------------------------------------------

Start Final Netlist Cleanup

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---------------------------------------------------------------------------------

Finished Final Netlist Cleanup

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Finished IO Insertion : Time (s): cpu = 00:00:17 ; elapsed = 00:00:20 . Memory (MB): peak = 1720.863 ; gain = 358.777 ; free physical = 684 ; free virtual = 2234

---------------------------------------------------------------------------------

Report Check Netlist:

+------+------------------+-------+---------+-------+------------------+

| |Item |Errors |Warnings |Status |Description |

+------+------------------+-------+---------+-------+------------------+

|1 |multi\_driven\_nets | 0| 0|Passed |Multi driven nets |

+------+------------------+-------+---------+-------+------------------+

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Start Renaming Generated Instances

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Finished Renaming Generated Instances : Time (s): cpu = 00:00:17 ; elapsed = 00:00:20 . Memory (MB): peak = 1720.863 ; gain = 358.777 ; free physical = 684 ; free virtual = 2234

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Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

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Start Rebuilding User Hierarchy

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Finished Rebuilding User Hierarchy : Time (s): cpu = 00:00:17 ; elapsed = 00:00:20 . Memory (MB): peak = 1720.863 ; gain = 358.777 ; free physical = 684 ; free virtual = 2234

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Start Renaming Generated Ports

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Finished Renaming Generated Ports : Time (s): cpu = 00:00:17 ; elapsed = 00:00:20 . Memory (MB): peak = 1720.863 ; gain = 358.777 ; free physical = 684 ; free virtual = 2234

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Start Handling Custom Attributes

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Finished Handling Custom Attributes : Time (s): cpu = 00:00:17 ; elapsed = 00:00:20 . Memory (MB): peak = 1720.863 ; gain = 358.777 ; free physical = 684 ; free virtual = 2234

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Start Renaming Generated Nets

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Finished Renaming Generated Nets : Time (s): cpu = 00:00:17 ; elapsed = 00:00:20 . Memory (MB): peak = 1720.863 ; gain = 358.777 ; free physical = 684 ; free virtual = 2234

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Start Writing Synthesis Report

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Report BlackBoxes:

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| |BlackBox name |Instances |

+-+--------------+----------+

+-+--------------+----------+

Report Cell Usage:

+------+-------+------+

| |Cell |Count |

+------+-------+------+

|1 |BUFG | 2|

|2 |CARRY4 | 166|

|3 |LUT1 | 51|

|4 |LUT2 | 175|

|5 |LUT3 | 301|

|6 |LUT4 | 224|

|7 |LUT5 | 113|

|8 |LUT6 | 239|

|9 |MUXF7 | 1|

|10 |FDRE | 73|

|11 |IBUF | 2|

|12 |OBUF | 16|

+------+-------+------+

Report Instance Areas:

+------+---------+-------+------+

| |Instance |Module |Cells |

+------+---------+-------+------+

|1 |top | | 1363|

+------+---------+-------+------+

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Finished Writing Synthesis Report : Time (s): cpu = 00:00:17 ; elapsed = 00:00:20 . Memory (MB): peak = 1720.863 ; gain = 358.777 ; free physical = 684 ; free virtual = 2234

---------------------------------------------------------------------------------

Synthesis finished with 0 errors, 0 critical warnings and 1 warnings.

Synthesis Optimization Runtime : Time (s): cpu = 00:00:14 ; elapsed = 00:00:16 . Memory (MB): peak = 1720.863 ; gain = 24.426 ; free physical = 738 ; free virtual = 2288

Synthesis Optimization Complete : Time (s): cpu = 00:00:17 ; elapsed = 00:00:20 . Memory (MB): peak = 1720.871 ; gain = 358.777 ; free physical = 738 ; free virtual = 2288

INFO: [Project 1-571] Translating synthesized netlist

INFO: [Netlist 29-17] Analyzing 167 Unisim elements for replacement

INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds

WARNING: [Netlist 29-101] Netlist 'Lab07\_timer' is not ideal for floorplanning, since the cellview 'Lab07\_timer' contains a large number of primitives. Please consider enabling hierarchy in synthesis if you want to do floorplanning.

INFO: [Project 1-570] Preparing netlist for logic optimization

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1722.863 ; gain = 0.000 ; free physical = 679 ; free virtual = 2229

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

INFO: [Common 17-83] Releasing license: Synthesis

20 Infos, 3 Warnings, 0 Critical Warnings and 0 Errors encountered.

synth\_design completed successfully

synth\_design: Time (s): cpu = 00:00:19 ; elapsed = 00:00:21 . Memory (MB): peak = 1722.863 ; gain = 360.852 ; free physical = 735 ; free virtual = 2285

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1722.863 ; gain = 0.000 ; free physical = 735 ; free virtual = 2285

WARNING: [Constraints 18-5210] No constraints selected for write.

Resolution: This message can indicate that there are no constraints for the design, or it can indicate that the used\_in flags are set such that the constraints are ignored. This later case is used when running synth\_design to not write synthesis constraints to the resulting checkpoint. Instead, project constraints are read when the synthesized design is opened.

INFO: [Common 17-1381] The checkpoint '/home/jinson/vivado/Lab07\_timer/Lab07\_timer.runs/synth\_1/Lab07\_timer.dcp' has been generated.

INFO: [runtcl-4] Executing : report\_utilization -file Lab07\_timer\_utilization\_synth.rpt -pb Lab07\_timer\_utilization\_synth.pb

INFO: [Common 17-206] Exiting Vivado at Thu May 2 17:35:38 2019...