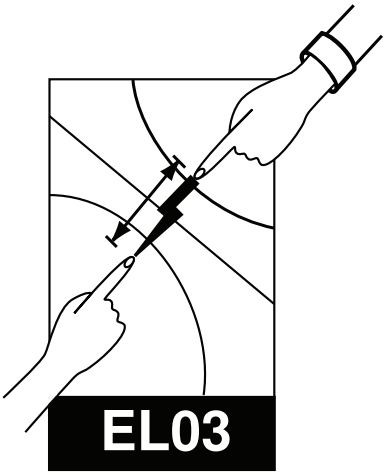
Introduction to digital data processing circuits



EL03

SWW, GD October 2024

Remember that you are responsible for your own safety when working in the laboratory. Always talk to a demonstrator or technician if you are concerned that anything may be unsafe.

TAKE NOTE: Before coming to the laboratory, read chapter 4 in your Electronics Manual[1] and do the theory exercises in sections 2 and 4.3 below. The exercises will be checked by a demonstrator at the start of the practical.

1 Introduction and objectives

Processing numbers and other data in binary digital systems involves transferring groups of binary digits (bits) between registers (data stores) and carrying out arithmetic, logical, or bitwise operations on them using logic circuits. The operations are orchestrated by control and timing circuits. The object of this practical is to introduce you to these elements.

2 Preliminary exercises

The background information needed to carry out the activities in this section can be obtained by studying the Electronics Manual, sections 3–4.1.

▶ Describe briefly the advantages of a digital over an analogue representation of numbers, especially the advantages of the binary system.

▶ What is the difference between combinational and sequential logic?

Write down the truth table for the basic function AND of three input variables A, B, C. Add columns to the table showing the OR, NAND (not and) and NOR (not or) functions.

Demonstrate the truth of de Morgan's law (the only non-trivial relation in Boolean Algebra):

$$\overline{A+B+C} = \overline{A}.\overline{B}.\overline{C} \tag{1}$$

by showing that the truth tables of the right-hand side and left-hand side are the same. Draw a logic circuit which produces $\overline{A}.\overline{B}.\overline{C}$ from inputs A, B and C.

[1] See `http://www-teaching.physics.ox.ac.uk/practical_course/ElectronicsManual.pdf` .

A	B	C	N
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

Table 1: Truth table for a function N with three inputs A-C

Table 1 shows the truth table of a function N of three inputs. Write down a Boolean expression for N then rearrange it to use only NOT and NOR functions. Draw a logic circuit using NOT and NOR gates which will generate this function.

3 The board

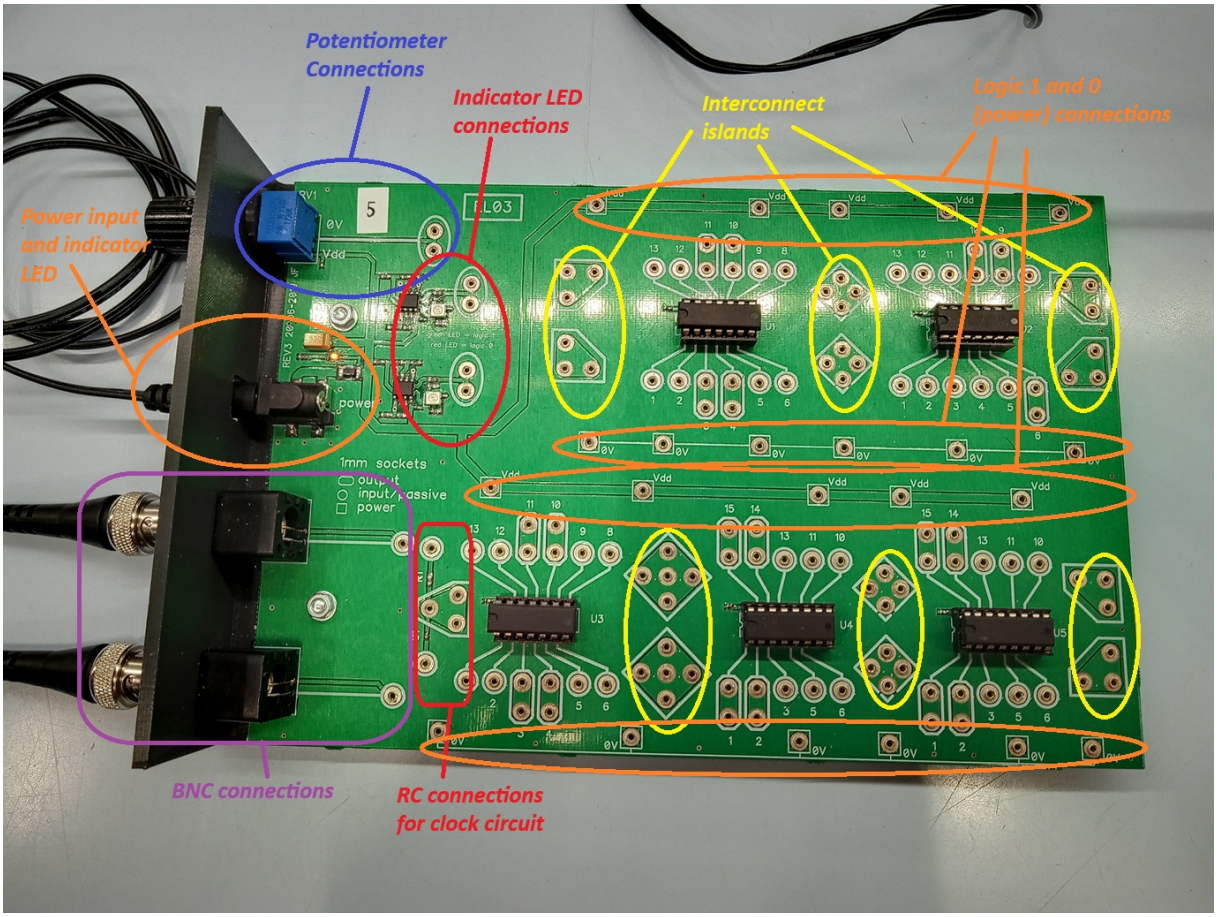


Figure 1: The EL03 board.

Fig. 1 shows the different sections of the EL03 board. The logic gates you will use are made from interconnected field effect transistors (FETs) formed on the surfaces of silicon chips. The technology is known as CMOS (Complementary Metal-Oxide Semiconductor).

The chips on your board are encapsulated in 14- or 16-pin dual in-line plastic (DIP) packages. The gates contained in each package and their connections to the pins are shown in Appendix A. These logic gates are part of a series known as 4000 Series, and the other markings on the chip include manufacturer's names or logos, package information, batch number, and date of manufacture.

> Identify the chip types by the four-digit number beginning "40" marked on them. (In some cases this may be difficult). Confirm your identifications with the diagram in Appendix A to make sure you have a clear understanding of the board layout.

Relevant pin connections from the chips have been brought out to sockets on the board so that circuits can be built by plugging in links between the sockets. The type of socket (input, output or power) is shown by the silkscreen markings on the board. The board has a number of unconnected islands (groups of pins) which can be used to expand the number of inputs that can be connected to one output. When connecting your circuits, be careful not to connect multiple outputs together, as this can damage the chips.

4000 series CMOS[2] will operate on any voltage from 5 to 15 V; we power the board using a plug-in 9 V AC-DC power supply. The ground of the supply is connected to 0 V on the board; the positive supply voltage on the board is called V_{dd}.

> Measure V_{dd} from one of the sockets on the board using the scope. Note the actual voltage.

There are two light-emitting diodes (LEDs) indicator circuits located on the board, which will illuminate green when connected to a logic 1 and red for a logic 0. Visual indication of the state of a gate output can be checked by connecting it to one of these circuits.

> Connect the output of the variable potential on the left-hand side of the board to one of the LED indicator inputs. Adjust the potentiometer fully anticlockwise and note the LED colour. Adjust the potentiometer fully clockwise and again note the LED colour.

Fixed logic 0s and 1s for inputs can be obtained by connecting to the sockets on the 0 V and V_{dd} tracks, respectively.

The LED indicators are good for confirming static logic values, but cannot show time-varying signals. The board has two BNC connectors on the left-hand side which can be used to connect an output to the oscilloscope. The scope can then be used to monitor the waveform.

Finally, the board has an interconnected resistor and capacitor which are used to make the clock circuit in section 5.3.

[2]There are other types of CMOS, e.g. 74HC series, which operate from different supply voltages.

4 Design of combinatorial logic circuits

4.1 Properties of the gates

As you have read in the Electronics Manual, you should be familiar with the logical function of NOR and NAND gates. Logic gates produce an output depending on the state of their inputs. Theoretically, for inputs, logic 0 is any voltage between zero and just below $\frac{V_{dd}}{2}$, and logic 1 is any voltage between just above $\frac{V_{dd}}{2}$ and V_{dd}, but in practice logic 0 is below $\frac{V_{dd}}{3}$ and logic 1 is above $\frac{2V_{dd}}{3}$. You can see the specified voltage values for inputs and outputs in Appendix B; you can also see that the output transitions when the input voltage crosses $\frac{V_{dd}}{2}$. You will find that the voltages generated by the gate outputs are typically close to 0 V and V_{dd}

> Connect the inputs of one of the gates on the chip of type 4093 so that its output will change state when the state of *one* of its inputs changes. Connect this input to the output of the variable potential divider at the left-hand end of the board. Using the scope channels on DC to measure the input and output voltages, record the input voltage at which the output changes state.

▶ Is this voltage the same for both rising and falling input voltages?

The gates on this chip are designed to use positive feedback to create a significant difference in switching voltage for rising and falling inputs. They are called "Schmitt trigger" inputs, and the difference between the two switching voltages is called *hysteresis*.

▶ Calculate the hysteresis for your gate. Why is hysteresis useful? Where would it be used?

In the Electronics Manual, you will have seen the truth tables for different types of logic gates.

> Using connections to 0 V and V_{dd} as inputs, verify by measurement the truth table of one of the gates on the 4025 chip.

4.2 NOT gates (inverters)

In section 4.1 you should have noted that a NAND gate and a NOR gate can be used as a NOT gate (or inverter) when the other inputs are correctly set to 0 V or V_{dd}. (This is why we haven't supplied any NOT gates on the board.).

> Show that NOT gates can also be made from NAND or NOR gates by connecting all their inputs together (use one of the "islands" on the board to connect the inputs together.)

4.3 A combinational logic design example

A logic function of two input variables A and B that is a logic 1 when either A or B but not both are 1 is called the EXCLUSIVE OR (XOR) function, written $A \oplus B$.

> Write down the truth table and a Boolean expression for XOR. Manipulate this expression into one containing only NOT and NAND functions, and draw a diagram of a circuit to realise it using only NAND gates.
>
> On this circuit diagram label each gate with the type number of the chip it is on and its pin connections, similar to that shown in the Electronics Manual, figure M 4.7. Make sure you include all the inputs of the gates used.

▶ Connect the circuit, confirm its operation against its truth table, and have it verified by a demonstrator.

5 Design of sequential logic

Background information for this section can be found in the Electronics Manual, section 4.5.

5.1 Properties of the flip-flops

The 4027 chip contains two edge-triggered JK flip-flops. They need a rapidly rising edge on the clock pulse for predictable operation and to prevent damage, more rapid than we can achieve with manual operation of a potential divider. A steep edge can be obtained by feeding the output of the potential divider to one of the Schmitt NANDs wired as a NOT gate and using its output as the clock pulse. (Note that this produces an inverted clock pulse: if you don't like this, use two Schmitt NANDs in series.)

Build this NAND "clock speed-up circuit" and use its output as a clock to verify that the truth table of one of the 4027 JK flip-flops agrees with the one in the Manual.

▶ Is the flip-flop triggered by the positive going or negative going edges at its clock input?

JK-type flip-flops are the most useful because they can be made to perform any flip-flop function.

Point out using the truth table and check experimentally that:

1. a D-type flip-flop can be made with the J input as the D input if the state of the K input is the inverse of the state of the J input. (Feed the K input with an inverter driven by the J input.)
2. A T-type flip-flop, one whose output toggles (changes state) at each positive clock edge, can be made by connecting both J and K inputs to 1.

5.2 A shift register or serial data register

Shift registers are typically used to convert serial communications streams, like USB data, into bytes. Data bits enter the shift register one bit per clock cycle, move through a set of flip-flops, and appear in parallel form at the flip-flop outputs. An 8-bit register would need 8 clock pulses to output a byte of data, and a 16-bit register would need 16 clock cycles to output a word of data.

Build a 4-bit shift register (without the recirculation or control circuits mentioned in the Manual) using your four JK flip-flops by connecting Q_i to J_{i+1} and $\overline{Q_i}$ to K_{i+1}. Add an inverter between the J and K inputs of the first flip-flop as you did for the D-type flip-flop above. Connect all of the flip-flop clock inputs to the output of your speed-up circuit.

Load the register with a 4-bit serial word by applying each bit in turn to the input and sending a clock pulse. Check by examining the Q output of each flip-flop that the word has been read into the register correctly.

Our serial word is now available as a parallel word at the Q outputs if we want it.

▶ Which flip-flop contains the first bit entered?

Check that your serial word is correctly read out (i.e. appears at the Q output of the last flip-flop in the register) as a further four clock pulses are sent.

5.3 A simple clock circuit

A clock is a circuit that generates pulses at a constant rate.

Dismantle the shift register and connect up the circuit shown in figure 2 using R = 10 kΩ ± 2 % and C = 1 nF ± 10 % on the board and the same 2-input Schmitt NAND gate you investigated in section 4.1.

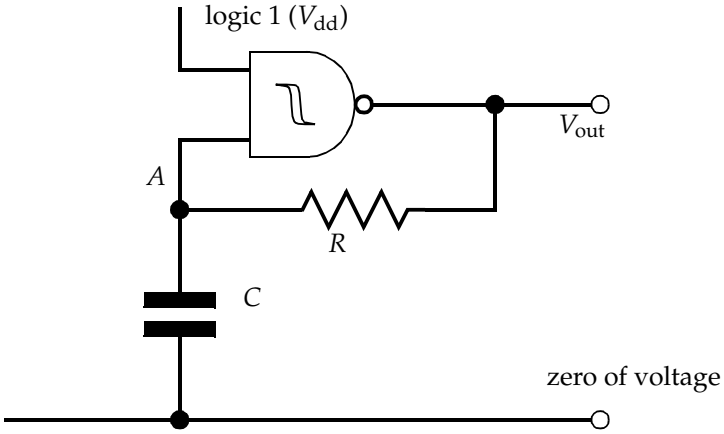


Figure 2: A simple clock circuit.

Make a sketch of the waveform at the output of the gate; label it with measured values for the pulse height, the mark time t_m (the pulse width when output equals 1), and the space time t_s (the time between pulses when the output equals 0).

Connect the second channel of your scope to A and draw the waveform there on the same sketch. Note the mark and space times for your waveform against those just measured without the oscilloscope connected to A.

▶ Describe briefly how the circuit works.

Theory predicts that the mark and space times of the pulse waveform produced by this clock are given by:

$$t_m = CR \ln\left(\frac{V_{dd} - V_l}{V_{dd} - V_h}\right) \qquad \text{and} \qquad t_s = CR \ln\left(\frac{V_h}{V_l}\right) \tag{2}$$

where V_h and V_l are the higher and lower input voltages at which the Schmitt trigger switches. Regular pulse trains are usually described by their period $t_m + t_s$ and their mark-to-space ratio $\frac{t_m}{t_s}$.

Using the values of V_h and V_l that you measured in section 4.1 and the expressions above, calculate the theoretical values for t_m and t_s.

▶ How do these compare with your measured values? Explain any discrepancy and explain any changes that you see in the pulse output when the second scope channel is connected and disconnected from A.

5.4 Frequency dividers and counters

Wire up three of the JK flip-flops as T-types and connect them as a ripple-through binary divider chain (section 4.5.3 in the Manual). Feed the first bistable (call it C) with the pulses from the clock and sketch, one above the other to show the time relationship between them, the clock waveform and the waveforms at the Q outputs of all three bistables A, B, C.

Your sketch should cover the time it takes for the slowest waveform to repeat itself. (Hint, trigger your scope from the slowest waveform.)

▶ Calling the clock frequency f, what frequencies does the divider chain make available?

The circuit can also be thought of as a 3-bit counter (see the Manual section 4.5.3) with output ABC, the A bit being the most significant.

▶ Which way does it count if you look at the outputs of the flip-flops ? How many clock pulses can be counted unambiguously ?

Leave the clock and divider connected for use in the next part.

5.5 Generating a waveform

Assume that for some reason we want to generate a repetitive waveform with the shape shown in figure 3.

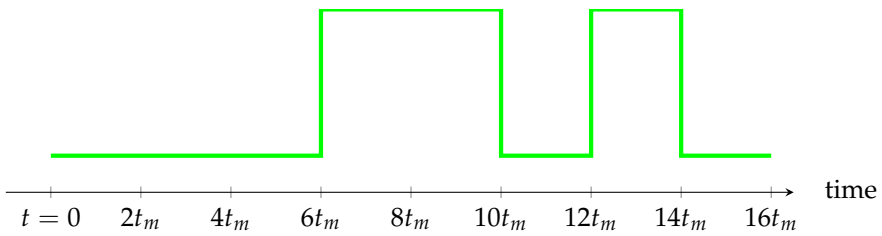


Figure 3: Waveform with the shape 00011010, where $t = 0$ is the instant at which the Q outputs of all the flip-flops in the divider chain make a transition from 0 to 1.

Use the waveforms from your divider chain and some combinational logic to generate the waveform.

Hint: to design the logic, sketch the desired waveform underneath your divider waveforms, think of the whole picture as a truth table rotated through 90 degrees, and look back at table 1. Use Boolean algebra to reduce the number of gates needed. Remember that your flip-flops provide both Q and $\overline{Q}$ outputs simultaneously.

Display your output waveform, together with the output of the slowest clock, on your scope.

▶ Ask a demonstrator to verify that your waveform is correct. You will see one or more unwanted thin spikes on your waveform. What is causing these? Could they be a problem; if so, why?

▶ Write a brief summary of what you have learned from this practical and discuss it with a demonstrator.

Optional A way to generate the waveform in section 5.5 without spikes is to feed the waveform into a D-type flip-flop which is clocked approximately 180° out of phase with the other flip-flops.

Design and construct such a circuit. Sketch the output showing its relation to the slowest clock waveform.

▶ Why does this eliminate the spikes?

Optional Another way to generate the waveform without spikes is to use a synchronous replacement for the ripple through binary divider, see the Manual section 4.5.5.

Design one and connect it up.

▶ Ask a demonstrator to verify that it is operating correctly.

Optional Derive the equation for t_m and t_s given in section 5.3.

A Connections to the gates and flip-flops in the packages

The packages shown in figure 4 are viewed from above. Pins are numbered anticlockwise, with pin 1 being at the notched end of the package. 0 V and V_{dd} are directly connected on the board.

The chips have their type number printed on them by the manufacturer, but these can be hard to read. Each chip has a "reference designator", e.g. "U1", printed next to it on the board; you can use these to identify which chip is which, using the captions in figure 4.

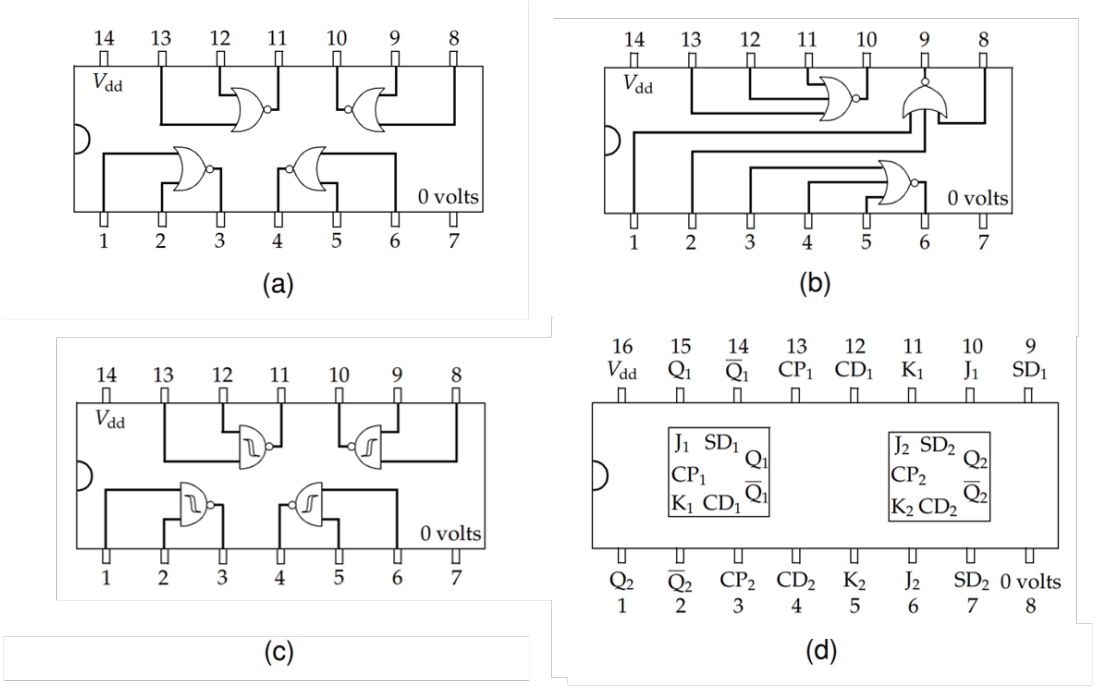


Figure 4: The packages used in EL03:

(a) U1: 4001 quad 2-input NOR;
(b) U2: 4025 triple 3-input NOR;
(c) U3: 4093 quad 2-input NAND, with Schmitt trigger input;
(d) U4 and U5: 4027 dual JK flip-flop.

For the 4027, the acronym CP stands for clock pulse input; the meanings of CD and SD are explained in the Manual section 4.5.1, but they are not used in this practical.

B Electrical characteristics for NOR gates

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	0.25	0.25	7.5	7.5	–	0.01	0.25	µA
	–	0,10	10	0.5	0.5	15	15	–	0.01	0.5	
	–	0,15	15	1	1	30	30	–	0.01	1	
	–	0,20	20	5	5	150	150	–	0.02	5	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5,4.5	–	5	1.5				—	—	1.5	V
	1,9	–	10	3				—	—	3	
	1.5,13.5	–	15	4				—	—	4	
Input High Voltage, V_{IH} Min.	0.5	–	5	3.5				3.5	—	—	
	1	–	10	7				7	—	—	
	1.5	–	15	11				11	—	—	
Input Current I_{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	–	$±10^{-5}$	±0.1	µA

Figure 5: NOR gate characteristics.

Figure 5 shows the static electrical characteristics for 4001 and 4025 NOR gates[3]. The key specifications are the input and output voltages for logic LOW and HIGH. Note that the output voltages are guaranteed to be better than the limits for the input voltages. This allows for any voltage loss and noise in long transmission lines between devices. It is not so important in our experiment where the connections are short. Logic circuits like these expect to operate with either LOW or HIGH inputs; if input voltages outside the expected range (i.e. 3 - 7 V for a 10 V supply) are applied at the input for any significant time (more than 4 µs), this can cause damage to the chip.

In normal operation, the actual voltage where the output transitions LOW-to-HIGH (or v.v.) is near $\frac{V_{dd}}{2}$, as shown in the picture. This was tested by applying a sine wave which transitioned from the LOW to HIGH input voltages in less than 4 µs.

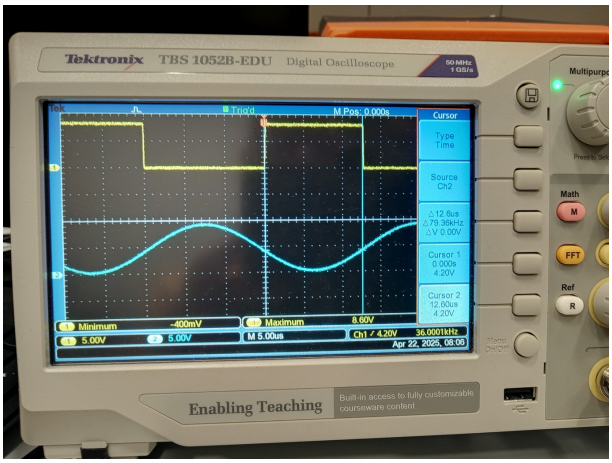


Figure 6: NOR gate transition voltages.

[3]Copied from the TI datasheet: `https://www.ti.com/lit/gpn/cd4001b` .