The python code here is used to generate the input to feed into the testbench in System Verilog and generates the output to compare with them generated by System Verilog. The code was done by two students separately, the python side will have a binary input sequence file, and the student who works on system Verilog side will take that input and copy past to the inputData file. The overOut file also copied the outputdata generated by the python code. Lastly, the student in system Verilog side will simulate the test bench in system Verilog side and then a file called outValues will be created and hold all the values generated by system Verilog. Eventually a diff -b command was used to check the correctness of the system. Runsynth.tcl file contains the information of the system which need to be synthesized.