视频编解码芯片规格书
——**AC5601** 芯片

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AC5601　Features

Kernel architecture

❋ Dual-core 32-bit CPU

❋ 32KB I-Cache，24KB D-Cache，Peripherals allowed to access the DDR through the cache

❋ 64K on-chip SRAM

❋ 240MHz maximum operating frequency

❋ 256 interrupt sources，8-level programmable priority

❋ Supports external I/O interrupts

❋ Supports soft interrupt(virtual interrupt)，priority can be configured

Video codec

❋ Single way：

1920x1080@30fps(H.264)

❋ Dual way：

1920x1080@30fps(H.264)+VGA(MJPEG)

720P@30fps(H.264)+VGA@30fps(H.264)

❋ Support M-JPEG codec，maximum support 720P@25fps，4:2:0

❋ JPEG single resolution：1920x1080

Video input and image processing

❋ Maximum resolution：1920x1080

❋ Support CSI、DVP interface

❋ Support RAW8/10/12 and YUV422 data format

❋ Support image AWB、AE、AF

❋ Support image 2DNR、3DNR

❋ Support image enhancement processing

❋ Support image deinterlace

❋ Support image scaling

❋ Support Dual-way image input

❋ Support video realtime recording

Video output and graphics processing

❋ Support DSI、DPI、DBI interface

❋ Support 8/16/18/24bits data bit-wide

❋ Support CVBS output

❋ Support image color enhancement

❋ Support multi-layer image output

❋ Support multi-layer OSD graphics overlay

❋ Supports image horizontal and vertical mirroring

❋ Support image 90/180/270degree rotation

❋ Maximum resolution 720P Vertical screen

Audio codec：
- ❊ Support multi-channel、multi-protocol audio voice codec though software
- ❊ Built-in coprocessor，support a variety of post-processing sound

Audio interface：
- ❊ 1 standard I2S interface,support 4 way 16bit、24bit audio cascade input
- ❊ Support 8KHz、16KHz、32KHz、44.1KHz、48KHz and other sampling frequency

Peripheral interface：
- ❊ Up to 104 programmable digital I/O pins
- ❊ 4 32-bit reloadable timer，can be used as timing、capture、PWM
- ❊ MC PWM
- ❊ Hardware watchdog
- ❊ 4 UART controller，of which 3 support with DMA cycle buffer
- ❊ 3 SPI host controller，support DMA
- ❊ 1 SPI FLASH interface
    -Support standard、dual、quad modes
    -Maximum support 16MB、80MHz
- ❊ 2 USB 2.0 high speed，support DMA
- ❊ 3 SDIO 2.0 interface，support DMA
- ❊ LADC controller，support 4 channels、16 data sources
- ❊ DAC controller，support left and right channels，16bit digital DAC
- ❊ RTC，support alarm clock and time base，support wake up chip
- ❊ Support 16 IO to wake up microcontroller
- ❊ IIC controller，support master mode and slave mode
- ❊ EMI controller，support DMA transmit
- ❊ AES128 and SHA1 ENCRYPT/DECRYPT
- ❊ Built-in AVOUT

Analog peripheral features：
- ❊ 3 clock oscillation circuit
- ❊ HTC（High precision on-chip oscillator）
- ❊ High speed USB 2.0 PHY
- ❊ 5 clock generators(PLL)，provide a variety of different frequencies of the system
- ❊ 16-bit stereo audio DAC, SNR > 88 dB
- ❊ 4-channel stereo ADC with 1-channel MIC amplifier, SNR > 72 dB
- ❊ 16-channel 10-bit ADC
- ❊ 2-channel 8-level low voltage detector
- ❊ Power on reset
- ❊ 4LDO: 3.3V-1.2V，3.3V-1.8V，3.3V-1.8V/2.5V，3.3V-2.8V
- ❊ 4Line 1Gbps/lane DSI phy
- ❊ 2Line 1Gbps/lane CSI phy
- ❊ DDRX PHY, support DDR1

❋ **External memory interface：**

❋ DDRX controller，support DDR1、16bit data bit-wide，DDR1 fastest support 250MHz，Maximum support 64MB

Supply Voltage：

符号	参数	最小	典型	最大	单位
VDDIO	IO Power	3.0	3.3	3.6	V
SVDD1/2/3	IO Power	3.0	3.3	3.6	V
		1.7	1.8	1.9	
DRVDD	DDR1 Power	2.3	2.5	2.7	V
DVDD12	Core Power	1.08	1.2	1.32	V

　　注：SVDD1 为 IO（PB3-PB15）的电源；
　　　　SVDD2 为 IO（PA5-PA15 PB0 PB1 PE0 PE1）的电源；
　　　　SVDD3 为 IO（PG0-PG15）的电源；

❋ 工作温度（-40℃ 至 +85℃）
❋ 存储温度（-65℃ 至 +150℃）

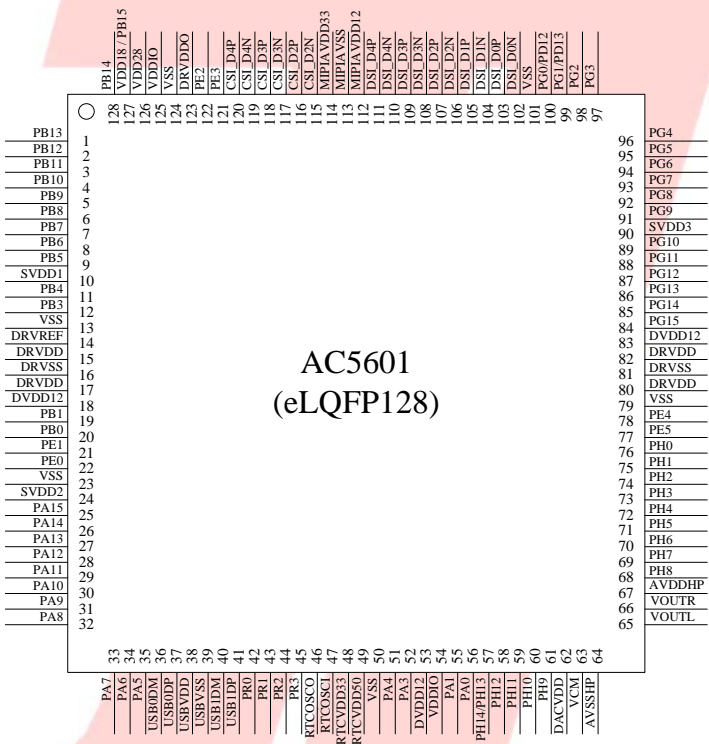## Package：

❋ eLQFP128(14mm X 14mm)
❋ 裸片

一、引脚定义

1.1 引脚分配

图 1-1　AC5601 _eLQFP128 引脚分配图

1.2 引脚描述

表 1-1　AC5601 _eLQFP128 引脚描述

Pin#	Name	I/O Type	Function	Other Function
1	PB13	I/O	GPIO	MII_RX1: MII Input1 RMII_RX1: RMII Input1 PWM1: Timer1 PWM Output SPI1_DID(1): SPI1 Data In (D)
2	PB12	I/O	GPIO	MII_RX0: MII Input0 RMII_RX0: RMII Input0 CAP3: Timer3 Capture ADC3: ADC Input Channel 3 SPI1_DOD(0): SPI1 Data Out (D)
3	PB11	I/O	GPIO	MII_CRS: MII CRS RMII_CRSDV: RMII CRSDV TMR1: Timer1 Clock In SPI1_CLKD: SPI1 Clock (D)
4	PB10	I/O	GPIO	MII_TXCK: MII Output Clock RMII_REFCLK: RMII REF Clock SPI2_DAT3B(3): SPI2 Data3 (B) SD1_DAT1C: SD1 Data1 (C)
5	PB9	I/O	GPIO	MII_RXERR: MII RXERR RMII_RXERR: RMII RXERR SPI2_CLKB: SPI2 Clock (B) SD1_DAT0C: SD1 Data0 (C)
6	PB8	I/O	GPIO	MII_TXEN: MII TXEN RMII_TXEN: RMII TXEN SPI2_DOB(0): SPI2 Data Out (B) SD1_CLKC: SD1 Clock (C)
7	PB7	I/O	GPIO	MII_TX1: MII Output1 RMII_TX1: RMII Output1 SPI2_DAT2B(2): SPI2 Data2 (B) SD1_CMDC: SD1 CMD (C)
8	PB6	I/O	GPIO	MII_TX0: MII Output0 RMII_TX0: RMII Output0 SPI2_DIB(1): SPI2 Data In (B) SD1_DAT3C: SD1 Data3 (C)
9	PB5	I/O	GPIO	MII_TX3: MII Output3 SPI2_CSB: SPI2 Chip Select(B) SD1_DAT2C: SD1 Data2 (C)
10	SVDD1	P	IO Power1	——

11	PB4	I/O	GPIO	IIC_SCL0_C: IIC0 SCL(C) UART3_TXB: Uart3 Data Out (B)
12	PB3	I/O	GPIO	ADC2: ADC Input Channel 2 IIC_SDA0_C: IIC0 SDA (C) Wakeup8: Port Wakeup 8 UART3_RXB: Uart3 Data In (B)
13	VSS	P	Digital Ground	——
14	DRVREF	P	DDR REF	——
15	DRVDD	P	DDR Power	——
16	DRVSS	P	DDR Ground	——
17	DRVDD	P	DDR Power	——
18	DVDD12	P	Core Power	——
19	PB1	I/O	GPIO	MII_RXDV: MII RXDV IIC_SDA1_A: IIC1 SDA (A)
20	PB0	I/O	GPIO	MII_RXCK: MII Input Clock IIC_SCL1_A: IIC1 SCL (A)
21	PE1	I/O	GPIO	SENSOR0_VSYN_B: SENSOR0 Vertical Synchronization (B) MII_COL_A: MII COL (A) SD0_DAT1D: SD0 Data1 (D) UART3_RXA: Uart3 Data In (A) LCDSS_DEN: LCD Data Enable
22	PE0	I/O	GPIO	SENSOR0_HSYN_B: Sensor0 Horizontal Synchronization (B) MII_TXERR_A: MII TXERR (A) SD0_DAT0D: SD0 Data0 (D) UART3_TXA: Uart3 Data Out (A)
23	VSS	P	Digital Ground	——
24	SVDD2	P	IO Power2	——
25	PA15	I/O	GPIO	SENSOR0_CLK_B: Sensor0 Clock (B) ALNK_MCKB: Audio Link Master Clock (B) LCDS_DAT23: LCD Data23
26	PA14	I/O	GPIO	SENSOR0_D9_B: Sensor0 Data9 (B) ALNK_WSB: Audio Link WS (B) SD0_CLKD: SD0 Clock (D) LCDS_DAT22: LCD Data22

27	PA13	I/O	GPIO	SENSOR0_D8_B: Sensor0 Data8 (B) ALNK_CKB: Audio Link Clock (B) SD0_CMDD: SD0 CMD (D) LCDS_DAT21: LCD Data21
28	PA12	I/O	GPIO	SENSOR0_D7_B: Sensor0 Data7 (B) ALNK_D3B: Audio Link Data3 (B) SD0_DAT2D: SD0 Data2 (D) LCDS_DAT20: LCD Data20
29	PA11	I/O	GPIO	SENSOR0_D6_B: Sensor0 Data6 (B) ALNK_D2B: Audio Link Data2 (B) SD0_DAT3D: SD0 Data3 (D) LCDS_DAT19: LCD Data19
30	PA10	I/O	GPIO	SENSOR0_D5_B: Sensor0 Data5 (B) ALNK_D1B: Audio Link Data1 (B) SD2_DAT3A: SD2 Data3 (A) LCDS_DAT18: LCD Data18
31	PA9	I/O	GPIO	SENSOR0_D4_B: Sensor0 Data4 (B) ALNK_D0B: Audio Link Data0 (B) SD2_DAT2A: SD2 Data2 (A) LCDS_DAT17: LCD Data17
32	PA8	I/O	GPIO	SENSOR0_D3_B: Sensor0 Data3 (B) SD2_DAT1A: SD2 Data1 (A) LCDS_DAT16: LCD Data16
33	PA7	I/O	GPIO	SENSOR0_D2_B: Sensor0 Data2 (B) SD2_DAT0A: SD2 Data0 (A) LCDS_DCLK: LCD Data Clock
34	PA6	I/O	GPIO	SENSOR0_D1_B: Sensor0 Data1 (B) SD2_CLKA: SD2 Clock (A) LCDS_VSYNC: LCD Vertical Synchronization
35	PA5	I/O	GPIO	SENSOR0_D0_B: Sensor0 Data0 (B) SD2_CMDA: SD2 CMD (A) LCDS_HSYNC: LCD Horizontal Synchronization
36	HUSB0DM	I/O	HUSB0DM	——
37	HUSB0DP	I/O	HUSB0DP	——
38	USBVDD	P	USB Power	——
39	USBVSS	P	USB Ground	——
40	HUSB1DM	I/O	HUSB1DM	——
41	HUSB1DP	I/O	HUSB1DP	——
42	PR0	I/O	RTC IO	PINR: PIN Reset

43	PR1	I/O	RTC IO	PINR: PIN Reset ADC13: ADC Input Channel 13
44	PR2	I/O	RTC IO	PINR: PIN Reset ADC12: ADC Input Channel 12
45	PR3	I/O	RTC IO	PINR: PIN Reset
46	RTCOSCO	I/O	RTC OSCO	——
47	RTCOSCI	I/O	RTC OSCI	——
48	RTCVDD33	P	RTC Power	——
49	RTCVDD50	P	RTC Power	——
50	VSS	P	Digital Ground	——
51	PA4	I/O	GPIO	SPI0_CLKA: SPI0 Clock (A) SFC_CLK: SFC Clock SD0_DAT0A: SD0 Data0 (A)
52	PA3	I/O	GPIO	SPI0_DOA(0): SPI0 Data Out (A) SFC_DO(0): SFC Data Out SD0_DAT2A: SD0 Data2 (A)
53	DVDD12	P	Core Power	——
54	VDDIO	P	IO Power	——
55	PA1	I/O	GPIO	IIC_SDA1_B: IIC1 SDA (B) SPI0_DIA(1): SPI0 Data In (A) SFC_DI(1): SFC Data In SD0_CMDA: SD0 CMD (A)
56	PA0	I/O	GPIO	SPI0_CSA: SPI0 Chip Select (A) SFC_CS: SFC Chip Select
57	PH14	I/O	GPIO	UART1_TXC: Uart1 Data Out (C) ADC10: ADC Channel 10 CLKOUT1: Clock Out1 IIC_SDA0_B: IIC0 SDA (B) Wakeup14: Port Wakeup 14 SPI1_DOC(0): SPI1 Data Out (C) LCDS_DAT14: LCD Data14
57	PH13	I/O	GPIO	UART0_RXC: Uart0 Data In (C) AVOUT: AV Output TMR3: Timer3 Clock In SD0_DAT3A: SD0 Data3 (A) SPI1_DIC(1): SPI1 Data In (C) LCDS_DAT13: LCD Data13

58	PH12	I/O	GPIO	UART0_TXC: Uart0 Data Out (C) ADC9: ADC Channel 9 PWM2: Timer2 PWM Output IIC_SCL0_B: IIC0 SCL (B) SPI1_CLKC: SPI1 Clock (C) LCDS_DAT12: LCD Data12
59	PH11	I/O	GPIO	LCD_DAT23A: LCD Data23 (A) MICR: MIC Right Channel SD1_DAT0A: SD1 Data0 (A) LCDS_DAT11: LCD Data11
60	PH10	I/O	GPIO	LCD_DAT22A: LCD Data22 (A) AMUX1R: Simulator Channel 1 Right SD1_CLKA: SD1 Clock (A) Wakeup13: Port Wakeup 13 UART2_TXB: Uart2 Data Out (B) SENSOR1_D0_A: Sensor1 Data0 (A) LCDS_DAT10: LCD Data10
61	PH9	I/O	GPIO	LCD_DAT21A: LCD Data21 (A) AMUX1L: Simulator Channel 1 Left SD1_CMDA: SD1 CMD (A) UART2_RXB: Uart2 Data In (B) SENSOR1_D1_A: Sensor1 Data1 (A) LCDS_DAT9: LCD Data9
62	DACVDD	P	DAC Power	——
63	VCM	P	VCM	——
64	AVSSHP	P	Head Phone Ground	___
65	VOUTL	O	DAC Left Channel	DACL
66	VOUTR	O	DAC Right Channel	DACR
67	AVDDHP	P	Head Phone Power	___
68	PH8	I/O	GPIO	LCD_DAT20A: LCD Data20 (A) AMUX0R: Simulator Channel 0 Right SD1_DAT3A: SD1 Data3 (A) SENSOR1_D2_A: Sensor1 Data2 (A) LCDS_DAT8: LCD Data8

69	PH7	I/O	GPIO	LCD_DAT19A: LCD Data19 (A) AMUX0L: Simulator Channel 0 Left SD1_DAT2A: SD1 Data2 (A) Wakeup12: Port Wakeup 12 SENSOR1_D3_A: Sensor1 Data3 (A) LCDS_DAT7: LCD Data7
70	PH6	I/O	GPIO	LCD_DAT18A: LCD Data18 (A) MICL:MIC Left Channel SENSOR1_D4_A: Sensor1 Data4 (A) LCDS_DAT6: LCD Data6
71	PH5	I/O	GPIO	LCD_VSYNCAA: LCD Vertical Synchronization UART1_RXB: Uart1 Data In (B) SD1_DAT1A: SD1 Data1 (A) SENSOR1_D5_A: Sensor1 Data5 (A) LCDS_DAT5: LCD Data5
72	PH4	I/O	GPIO	LCD_HSYNCAA: LCD Horizontal Synchronization EMI_RDAA: EMI Read SENSOR1_D6_A: Sensor1 Data6 (A) LCDS_DAT4: LCD Data 4
73	PH3	I/O	GPIO	LCD_DENAA: LCD Data Enable EMI_WRAA: EMI Write SENSOR1_D7_A: Sensor1 Data7 (A) LCDS_DAT3: LCD Data 3
74	PH2	I/O	GPIO	LCD_DCLKAA: LCD Data Clock UART1_TXB: Uart1 Data Out (B) SENSOR1_D8_A: Sensor1 Data8 (A) LCDS_DAT2: LCD Data 2
75	PH1	I/O	GPIO	LCD_DAT17A: LCD Data17 (A) UART2_RXD: Uart2 Data In (D) TMR2: Timer2 Clock In SENSOR1_D9_A: Sensor1 Data9 (A) LCDS_DAT1: LCD Data 1
76	PH0	I/O	GPIO	LCD_DAT16A: LCD Data16 (A) UART2_TXD: Uart2 Data Out (D) SPI1_DIA(1): SPI1 Data In (A) CAP2: Timer2 Capture SENSOR1_CLK_A: Sensor1 Clock (A) LCDS_DAT0: LCD Data 0

77	PE5	I/O	GPIO	ADC8: ADC Channel 8 IIC_SDA1_D: IIC1 SDA (D) SPI1_DOA(0): SPI1 Data Out (A) Wakeup11: Port Wakeup 11 SENSOR1_VSYN_A: SENSOR1 Vertical Synchronization (A)
78	PE4	I/O	GPIO	IIC_SCL1_D: IIC1 SCL (D) SPI1_CLKA: SPI1 Clock (A) Wakeup10: Port Wakeup 10 SENSOR1_HSYN_A: Sensor1 Horizontal Synchronization (A)
79	VSS	P	Digital Ground	——
80	DRVDD	P	DDR Power	——
81	DRVSS	P	DDR Ground	——
82	DRVDD	P	DDR Power	——
83	DVDD12	P	Core Power	——
84	PG15	I/O	GPIO	LCD_DAT15A: LCD Data15 (A) EMI_D15A: EMI Data15 (A)
85	PG14	I/O	GPIO	LCD_DAT14A: LCD Data14 (A) EMI_D14A: EMI Data14 (A)
86	PG13	I/O	GPIO	LCD_DAT13A: LCD Data13 (A) EMI_D13A: EMI Data13 (A) 电机 PWM_H3_A SD2_DAT1B: SD2 Data1 (B)
87	PG12	I/O	GPIO	LCD_DAT12A: LCD Data12 (A) EMI_D12A: EMI Data12 (A) 电机 PWM_L3_A SD2_DAT0B: SD2 Data0 (B)
88	PG11	I/O	GPIO	LCD_DAT11A: LCD Data11 (A) EMI_D11A: EMI Data11 (A) 电机 PWM_H2_A SD2_CLKB: SD2 Clock (B)
89	PG10	I/O	GPIO	LCD_DAT10A: LCD Data10 (A) EMI_D10A: EMI Data10 (A) 电机 PWM_L2_A SD2_CMDA: SD2 CMD (A)
90	SVDD3	P	IO Power3	——

91	PG9	I/0	GPIO	LCD_DAT9A: LCD Data9 (A) EMI_D9A: EMI Data9 (A) 电机 PWM_H1_A SD2_DAT3B: SD2 Data3 (B)
92	PG8	I/0	GPIO	LCD_DAT8A: LCD Data8 (A) EMI_D8A: EMI Data8 (A) 电机 PWM_L1_A SD2_DAT2B: SD2 Data2 (B)
93	PG7	I/0	GPIO	LCD_DAT7A: LCD Data7 (A) EMI_D7A: EMI Data7 (A) UART0_RXB: Uart0 Data In (B) IIC_SDA0_A: IIC0 SDA (A)
94	PG6	I/0	GPIO	LCD_DAT6A: LCD Data6 (A) EMI_D6A: EMI Data6 (A) UART0_TXB: Uart0 Data Out (B) IIC_SCL0_A: IIC0 SCL (A)
95	PG5	I/0	GPIO	LCD_DAT5A: LCD Data5 (A) EMI_D5A: EMI Data5 (A) LCD_VSYNCAB: LCD Vertical Synchronization SD0_DAT1C: SD0 Data1 (C)
96	PG4	I/0	GPIO	LCD_DAT4A: LCD Data4 (A) EMI_D4A: EMI Data4 (A) LCD_HSYNCAB: LCD Horizontal Synchronization EMI_RDAB: EMI Read SD0_DAT0C: SD0 Data0 (C)
97	PG3	I/0	GPIO	LCD_DAT3A: LCD Data3 (A) EMI_D3A: EMI Data3 (A) LCD_DCLKAB: LCD Data Clock SD0_CLKC: SD0 Clock (C)
98	PG2	I/0	GPIO	LCD_DAT2A: LCD Data2 (A) EMI_D2A: EMI Data2 (A) LCD_DENAB: LCD Data Enable EMI_WRAB: EMI Write SD0_CMDC: SD0 CMD (C)
99	PG1	I/0	GPIO	LCD_DAT1A: LCD Data1 (A) EMI_D1A: EMI Data1 (A) SD0_DAT2C: SD0 Data2 (C)
99	PD13	I/0	GPIO	OSC01
100	PG0	I/0	GPIO	LCD_DAT0A: LCD Data0 (A) EMI_D0A: EMI Data0 (A) SD0_DAT3C: SD0 Data3 (C)
100	PD12	I/0	GPIO	OSCI1

101	VSS	P	Digital Ground	——
102	DSI_D0N	O	MIPI DSI lane	MIPI DSI data (0/1/2/3) lane (p/n) MIPI DSI clock lane (p/n)
103	DSI_D0P	O	MIPI DSI lane	MIPI DSI data (0/1/2/3) lane (p/n) MIPI DSI clock lane (p/n)
104	DSI_D1N	O	MIPI DSI lane	MIPI DSI data (0/1/2/3) lane (p/n) MIPI DSI clock lane (p/n)
105	DSI_D1P	O	MIPI DSI lane	MIPI DSI data (0/1/2/3) lane (p/n) MIPI DSI clock lane (p/n)
106	DSI_D2N	O	MIPI DSI lane	MIPI DSI data (0/1/2/3) lane (p/n) MIPI DSI clock lane (p/n)
107	DSI_D2P	O	MIPI DSI lane	MIPI DSI data (0/1/2/3) lane (p/n) MIPI DSI clock lane (p/n)
108	DSI_D3N	O	MIPI DSI lane	MIPI DSI data (0/1/2/3) lane (p/n) MIPI DSI clock lane (p/n)
109	DSI_D3P	O	MIPI DSI lane	MIPI DSI data (0/1/2/3) lane (p/n) MIPI DSI clock lane (p/n)
110	DSI_D4N	O	MIPI DSI lane	MIPI DSI data (0/1/2/3) lane (p/n) MIPI DSI clock lane (p/n)
111	DSI_D4P	O	MIPI DSI lane	MIPI DSI data (0/1/2/3) lane (p/n) MIPI DSI clock lane (p/n)
112	MIPIAVDD12	P	MIPI AVDD	——
113	MIPIAVSS	P	MIPI AVSS	——
114	MIPI_AVDD33	P	MIPI Power	——
115	CSI_D2N	I	MIPI CSI lane	MIPI CSI clock lane (p/n)
116	CSI_D2P	I	MIPI CSI lane	MIPI CSI clock lane (p/n)
117	CSI_D3N	I	MIPI CSI lane	MIPI CSI data (0/1) lane (p/n)
118	CSI_D3P	I	MIPI CSI lane	MIPI CSI data (0/1) lane (p/n)
119	CSI_D4N	I	MIPI CSI lane	MIPI CSI data (0/1) lane (p/n)
120	CSI_D4P	I	MIPI CSI lane	MIPI CSI data (0/1) lane (p/n)
121	PE3	I/O	GPIO	LVD：LVD Test Pin ADC5：ADC Channel 5 IIC_SDA1_C：IIC1 SDA (C)

122	PE2	I/O	GPIO	VPP CLKOUT0: Clock Out0 IIC_SCL1_C：IIC1 SCL（C）
123	DRVDD0	P	DDR Power	——
124	VSS	P	Digital Ground	——
125	VDDIO	P	IO Power	——
126	AVDD28	P	AVDD28	——
127	AVDD18	P	AVDD18	___
127	PB15	I/O	GPIO	UART0_RXD: Uart0 Data In（D） MII_RX3: MII Input3 OSCO2
128	PB14	I/O	GPIO	UART0_TXD: Uart0 Data Out（D） MII_RX2: MII Input2 OSCI2 TMR0：Timer0 Clock In ADC4：ADC Channel 4 Wakeup9：Port Wakeup 9

（★说明：**1、P----Power Supply　　2、I----Input　　3、O----Output　　4、I/O----Bi-direction**）

二、电气特性

2.1　IO 输入、输出高低逻辑特性

表 2-1

输入特性						
符号	参数	最小	典型	最大	单位	测试条件
V_{IL}	Low-Level Input Voltage	-0.3	–	0.3*VDDIO	V	VDDIO = 3.3V
V_{IH}	High-Level Input Voltage	0.7*VDDIO	–	VDDIO+0.3	V	VDDIO = 3.3V
输出特性						
V_{OL}	Low-Level Output Voltage	–	–	0.1*VDDIO	V	VDDIO = 3.3V
V_{OH}	High-Level Output Voltage	0.9*VDDIO	–	–	V	VDDIO = 3.3V

2.2　IO 输出能力、上下拉电阻特性

表 2-2

Port　口	输出能力	上拉电阻	下拉电阻	备注
PA5 - PA15 PB0 - PB1 PB3 - PB15 PD12 - PD13 PE0 - PE1 PE3 - PE5 PG0 - PG15 PH0 - PH14	强驱：24mA 弱驱：8mA	10K	60K	——
PE2	8mA（无强弱驱之分）	10K	10K	——
PR0-PR3	8mA(片内串接 200Ω电阻)	10K	60K	RTC 模块需供电

（★说明：上下拉电阻的精度约为±20%)

2.3　DAC 特性

表 2-3

符号	参数	最小	典型	最大	单位	测试条件
SNR	Signal to Noise Ratio		94		dB	1KHz,SR=44.1KHz,静音文件, DACVDD　with 1u cap
THD+N	Total Harmonic Distortion+ Noise		-75		dB	1KHz,SR=44.1KHz, DACVDD　with 1u cap

三、封装

3.1　eLQFP_128PIN 封装图

图 3-1 AC5601_eLQFP128 封装图

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.14	—	0.22
b1	0.13	0.16	0.19
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	15.80	16.00	16.20
D1	13.90	14.00	14.10
E	15.80	16.00	16.20
E1	13.90	14.00	14.10
eB	15.05	—	15.35
e	0.40BSC		
L	0.45	—	0.75
L1	1.00REF		
θ	0	—	7

LF size (mil)	D2	E2
236*236	6.00	6.00
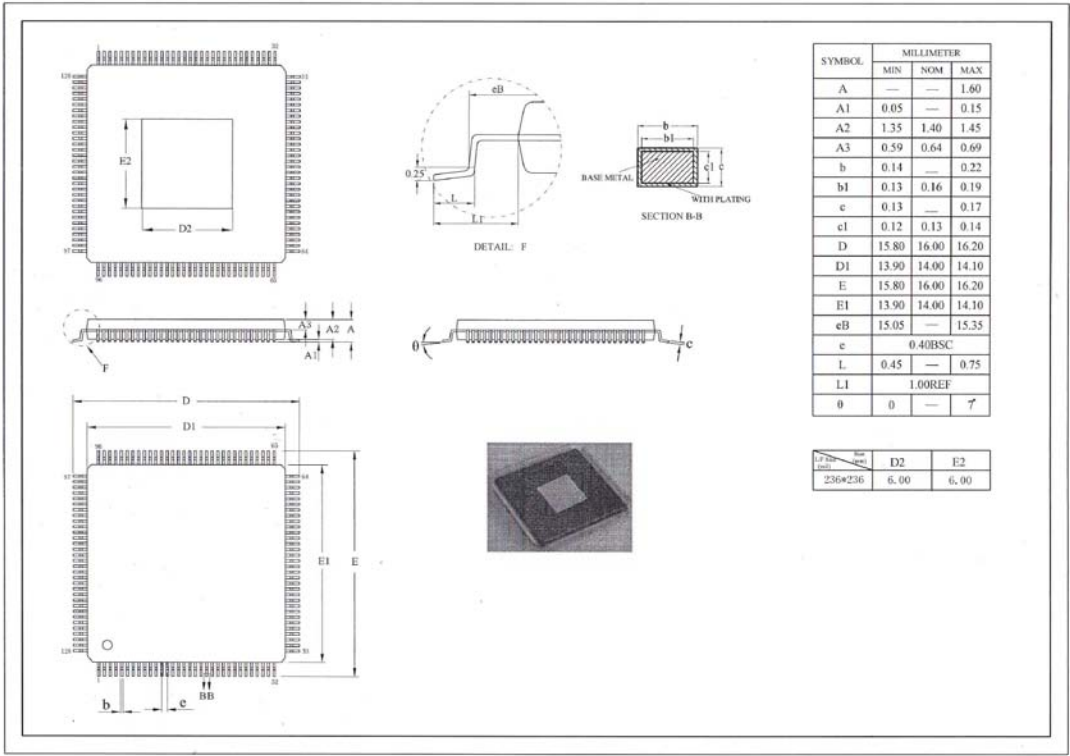
四、版本信息

日期	版本号	描述
2017.08.16	V1.0	原始版本。