ICN6211 Specification

MIPI® DSI BRIDGE TO RGB output

Revision 0.4

Chipone Technology (Beijing) Co., Ltd
13th Floor, Test Tower, Building 4, 31 Middle North Third Ring Rd.,
Haidian District, Beijing, 100088
PRC
Contact: Simon Liu
Email: simon_liu@chiponeic.com

Revision History

Rev	Date	Author	Description
0.1	2014-03-25	Simon_Liu	Initial version
0.2	2014-04-23	Simon_Liu	1. Update pin diagram and pin description 2. Add FRC/Hi-FRC function 3. Add RGB out clock phase control description
0.3	2014-06-19	Simon_Liu	Update package diagram
0.4	2014-07-04	Simon_Liu	VDD2 & VDD3 should be in same domain.

Table of Contents

Table of figures

1 Introduction

ICN6211 is a bridge chip which receives MIPI® DSI inputs and sends RGB outputs.

MIPI® DSI supports up to 4 lanes and each lane operates at 1Gbps maximum; the totally maximum input bandwidth is 4Gbps; and the MIPI defined ULPS(ultra-low-power state) is also supported. ICN6211 decodes MIPI® DSI 16bpp RGB565 and 18bpp RGB666 and 24bpp RGB888 packets.

The RGB output 18 or 24 bits pixel with pixel clock range of 25MHz to 154MHz.

ICN6211 support video resolution up to FHD (1920x1080) and WUXGA(1920x1200).

ICN6211 adopts QFN48 pins package.

1.1 Feature List

- Supports MIPI® D-PHY Version 1.00.00 and MIPI® DSI Version 1.02.00.
- Single Channel DSI Receiver with One, Two, Three and Four lanes configurable, each lanes operates up to 1Gbps.
- Receives 16bpp RGB565 and 18bpp RGB666 and 24bpp RGB888 packets defined by DSI.
- Supports MIPI Low State, Ultra-Low Power State, Shut Down mode.
- Output RGB with pixel clock range of 25MHz to 154MHz.
- RGB output supports flexible swap.
- Can adjust RGB Clock output phase(with 1/4, 1/2, 3/4 and fine adjust option) .
- Provides FRC/Hi-FRC function to improve 18bpp image performance.
- power supply : 1.8V/2.5V/3.3V for RGB output; 1.8V/2.5V/3.3V for MIPI and digital IO.
- provide I2C slave interface.
- package: QFN48-pins with e-pad.

2 Functional Block Diagram

Following figure shows a functional block diagram of the ICN6211.

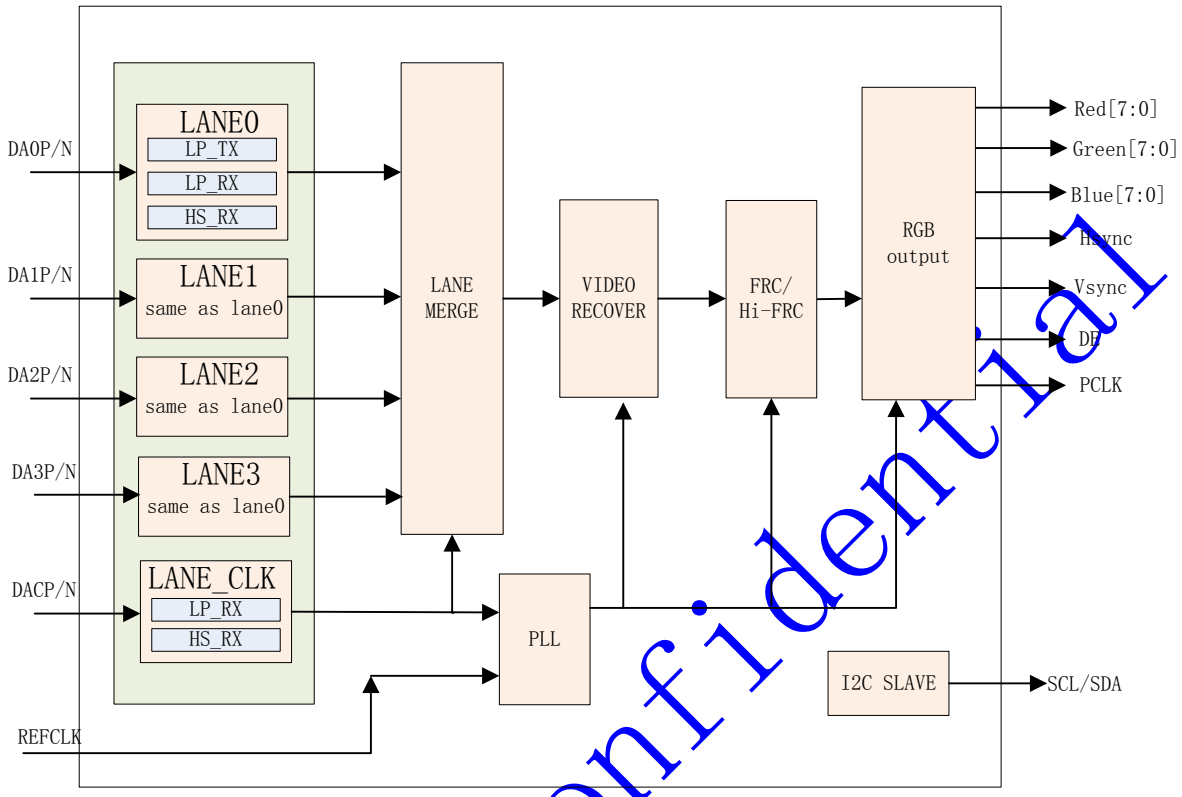


Figure 2-1 ICN6211 function block diagram

3 System Application Diagram

In the diagram below shows the ICN6211's system application.

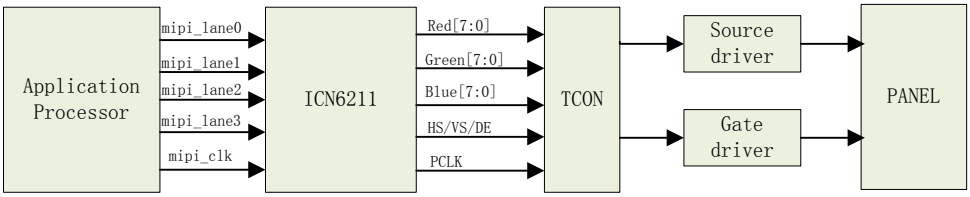


Figure 3-1 ICN6211 system application diagram

4 Pin Diagram

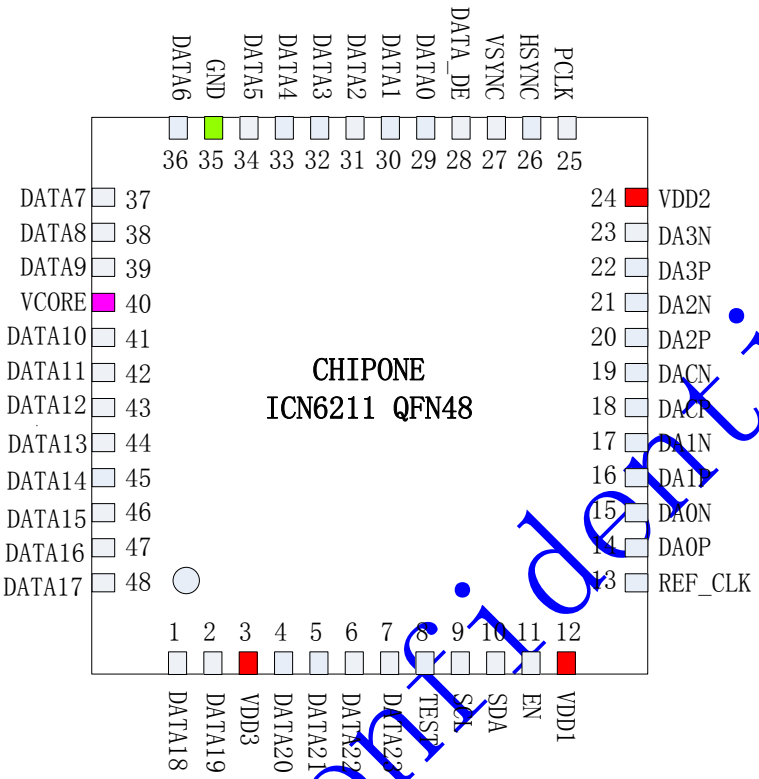


Figure 4-1 ICN6211 QFN48 pin diagram (Top View)

5 Pin Description

Name	Pin Number	I/O	Description
MIPI interface			
DA0P/DA0N	14/15	Input	MIPI® D-PHY, data LANE0.
DA1P/DA1N	16/17	Input	MIPI® D-PHY, data LANE1.
DA2P/DA2N	20/21	Input	MIPI® D-PHY, data LANE2.
DA3P/DA3N	22/23	Input	MIPI® D-PHY, data LANE3.
DACP/DACN	18/19	Input	MIPI® D-PHY, clock LANE.
RGB interface			
PCLK	25	Output	Pixel clock
HSYNC	26	Output	Horizontal sync signal
VSYNC	27	Output	Vertical sync signal
DATA_EN	28	Output	Data enable signal
DATA0	29	Output	DATA0 ~ DATA23 output video data. Red/Green/Blue color and bit order mapped onto DATA0 ~ DATA23 can be swapped flexibly, please refer to "RGB output swap table".
DATA1	30	Output	
DATA2	31	Output	
DATA3	32	Output	
DATA4	33	Output	
DATA5	34	Output	
DATA6	36	Output	
DATA7	37	Output	
DATA8	38	Output	
DATA9	39	Output	
DATA10	41	Output	
DATA11	42	Output	
DATA12	43	Output	
DATA13	44	Output	
DATA14	45	Output	
DATA15	46	Output	
DATA16	47	Output	

DATA17	48	Output	
DATA18	1	Output	
DATA19	2	Output	
DATA20	4	Output	
DATA21	5	Output	
DATA22	6	Output	
DATA23	7	Output	
MISC			
EN	11	input	When EN is low, this chip is reset.
REF_CLK	13	input	Optional reference clock for RGB output clock.
SCL	9	input	Local I2C bus, weakly PULL UP.
SDA	10	inout	Local I2C bus, weakly PULL UP.
TEST	8	input	For test, when work, connect to GND. Weakly PULL DOWN.
Power/Ground			
GND	35	Power	Ground
VDD1	12	Power	MIPI RX power supply, can be 1.8V/2.5V/3.3V
VDD2	24	Power	PLL power supply, can be 1.8V/2.5V/3.3V
VDD3	3	Power	RGB output power supply, can be 1.8V/2.5V/3.3V
VCORE	40	Power	Output from voltage regulator for digital core.

NOTE:

1. The use of two ceramic capacitors(2 x 1uF and 2 x 0.01uF) with pin VCORE provides good performance. At least, one 1uF and one 0.01uF capacitor is necessary. Also, the trace between the decoupling capacitor and pin should minimized.
2. REF_CLK can be used as the reference clock for RGB output. When it is not used, this pin should be connected to GND.
3. SCL/SDA/EN/TEST should be corresponding to VDD1 power supply.
4. VDD2 and VDD3 should be in the same power domain.

6 Function Description

6.1 MIPI Receiver

6.1.1 DSI Lane Merging

ICN6211 support four DSI data lanes, and may be configured to one, two or three DSI data lanes. Unused DSI input lanes should be left unconnected or driven to LP11 state.

Following figure illustrates the lane merging function for 4-lane, 3-lane, 2-lane and 1-lane separately.

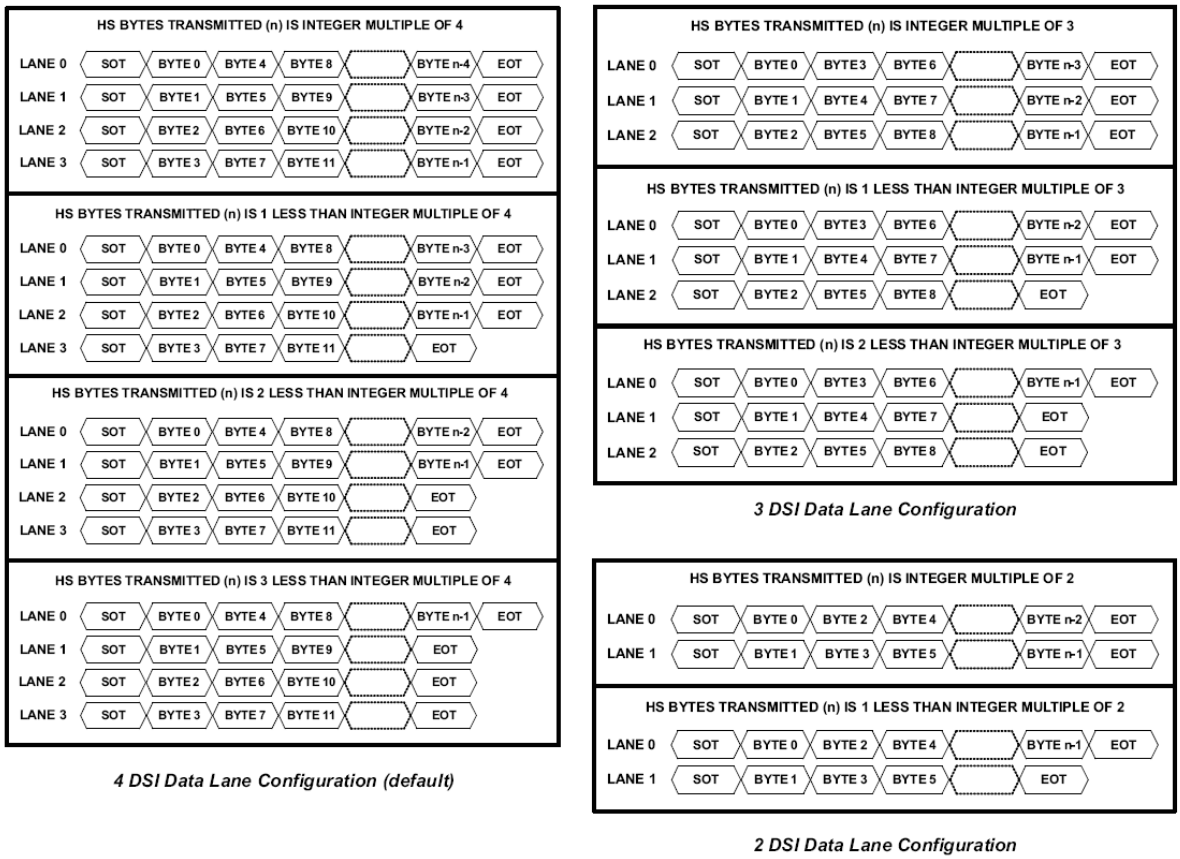


Figure 6-1 DSI multi-lanes HS Transmission Example

6.1.2 DSI Pixel Stream Packets

ICN6211 receives and interpret 18bpp(RGB666) , 24bpp(RGB888) DSI packets and translates to video stream.

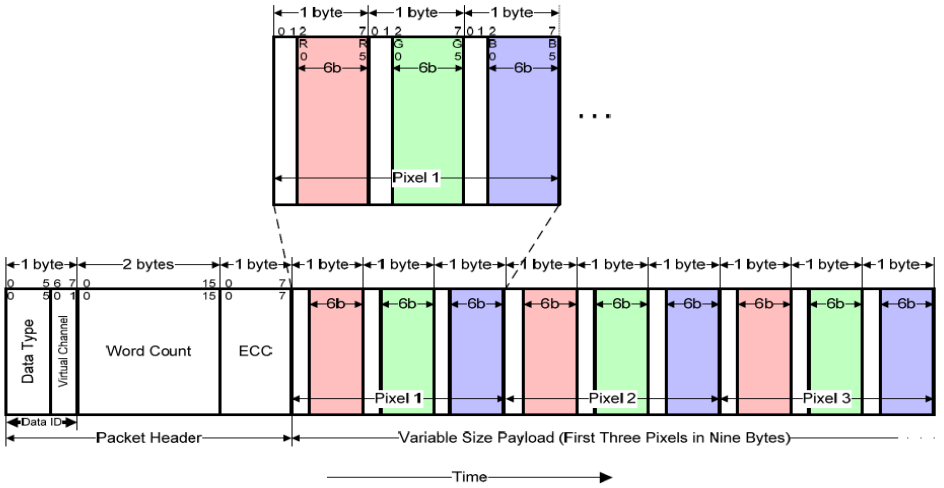


Figure 6-2 DSI RGB666 Color format, Loosely Long Packet

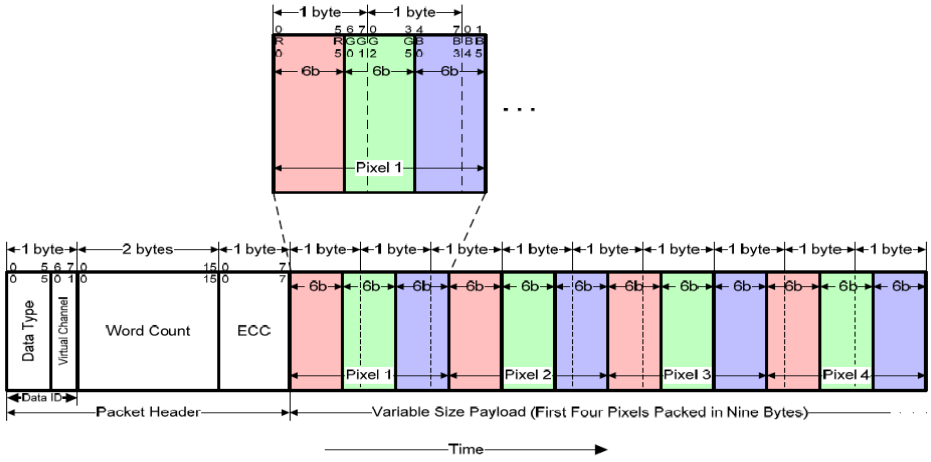


Figure 6-3 DSI RGB666 Color format, Tightly Long Packet

For the RGB666 tightly packet, the total line width(displayed plus non-displayed pixels) should be a multiple of four pixels(nine bytes).

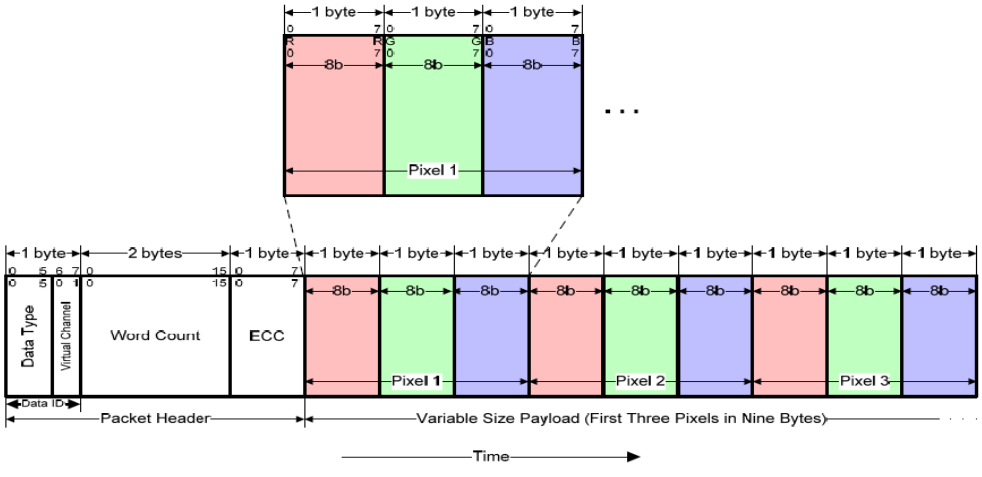


Figure 6-4 DSI RGB888 Color format, Long Packet

6.1.3 DSI Video Transmission sequence

ICN6211 supports Non-Burst Mode with Sync Pulses, Non-Burst Mode with Sync Events and Burst mode.

- Non-Burst Mode with Sync Pulses: enables the peripheral to accurately reconstruct original video timing, including sync pulse widths.
- Non-Burst Mode with Sync Events: similar to above, but accurate reconstruction of sync pulse widths is not required, so a single Sync Event is substituted.
- Burst mode: RGB pixel packets are time-compressed, leaving more time during a scan line for LP mode(saving power).

For all three sequences, the first line of a video frame shall start with a VSS packet, and all other lines start with VSE or HSS. The position of the synchronization packets in time is of utmost importance since this has a direct impact on the visual performance of the display panel; that is, the LVDS output video timing(HS-Horizontal sync and VS-Vertical sync) are generated based on the synchronization.

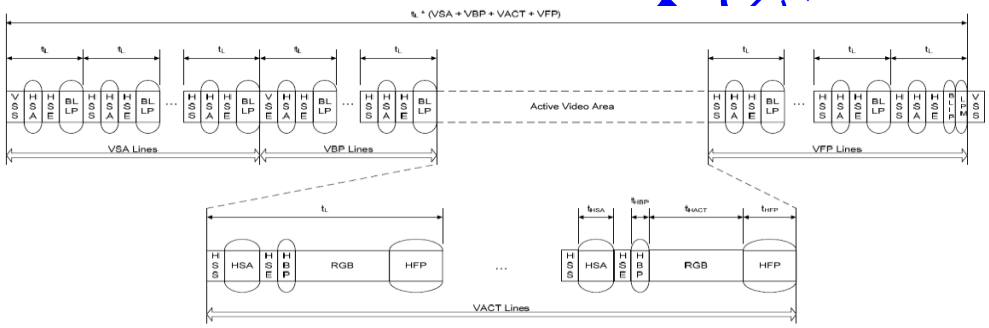


Figure 6-5 Non-Burst Mode with Sync Pulses

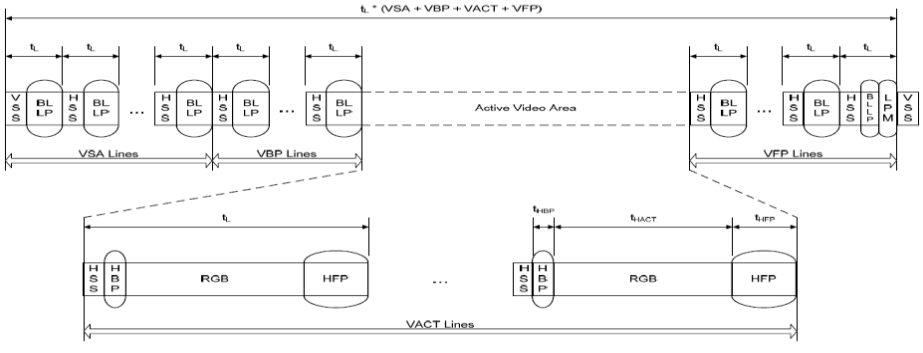


Figure 6-6 Non-Burst Mode with Sync Events

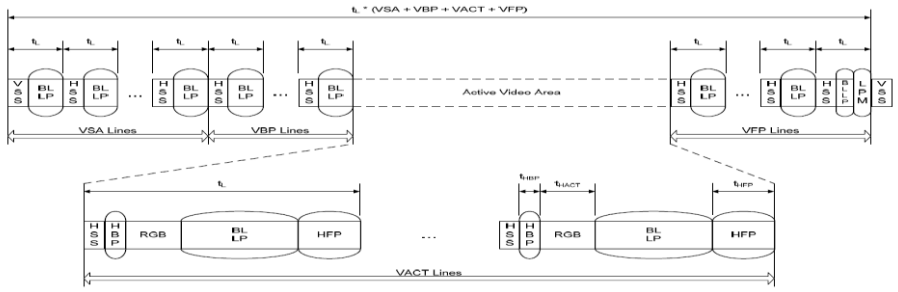


Figure 6-7 Burst mode

6.2 RGB output

ICN6211 supports RGB666 and RGB888 output.

In following table:

Group_0[7:0] = { DATA7, DATA6, DATA5, DATA4, DATA3, DATA2, DATA1, DATA0};

Group_1[7:0] = { DATA15, DATA14, DATA13, DATA12, DATA11, DATA10, DATA9, DATA8}

Group_2[7:0]= {DATA23, DATA22, DATA21, DATA20, DATA19, DATA18, DATA17, DATA16};

Red0[7:0], Green0[7:0], Blue[7:0] is the input video data.

For RGB666, color[5] is MSB & color[0] is LSB;

For RGB888, color[7] is MSB & color[0] is LSB.

Color may be red or green or blue.

Group_X may be Group_0 or Group_1 or Group_2.

RGB color swap mode

RGB_SWAP	000	001	010	011	100	101
Group_0	Red[7:0]	Red[7:0]	Green[7:0]	Green[7:0]	Blue[7:0]	Blue[7:0]
Group_1	Green[7:0]	Blue[7:0]	Red[7:0]	Blue[7:0]	Red[7:0]	Green[7:0]
Group_2	Blue[7:0]	Green[7:0]	Blue[7:0]	Red[7:0]	Green[7:0]	Red[7:0]

Data bit order mode

BIT_ORDER	RGB666				RGB888	
	000	001	010	011	100	101
Group_X[7]	invalid	invalid	Color[5]	Color[0]	Color[7]	Color[0]
Group_X[6]	invalid	invalid	Color[4]	Color[1]	Co]lor[6	Color[1]
Group_X[5]	Color[5]	Color[0]	Color[3]	Color[2]	Color[5]	Color[2]
Group_X[4]	Color[4]	Color[1]	Color[2]	Color[3]	Color[4]	Color[3]
Group_X[3]	Color[3]	Color[2]	Color[1]	Color[4]	Color[3]	Color[4]
Group_X[2]	Color[2]	Color[3]	Color[0]	Color[5]	Color[2]	Color[5]
Group_X[1]	Color[1]	Color[4]	invalid	invalid	Color[1]	Color[6]
Group_X[0]	Color[0]	Color[5]	invalid	invalid	Color[0]	Color[7]

6.3 RGB Clock phase adjust

ICN6211 provides RGB output clock phase adjust options, which can compensate the mismatch in case of routing or other reasons, such will make easier for PCB routing or system cable connection.

The output RGB clock can be aligned with data/hsync/vsync/data_de, or delayed by 1/4, 1/2, 3/4 phase. Further more, for each pahse, fine delay adjust can be added by fixed delay with the range between -2ns and +2ns.

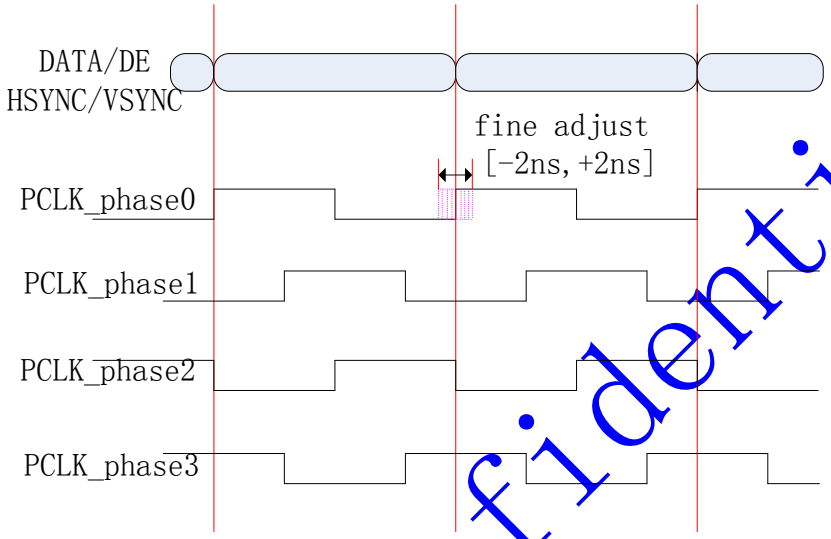


Figure 6-8 RGB output clock phase delay

6.4 Bist mode

ICN6211 goes into bist mode when configure register is enabled, five built-in images as below are displayed sequentially; and the interval time can be set (default is about 2ms).

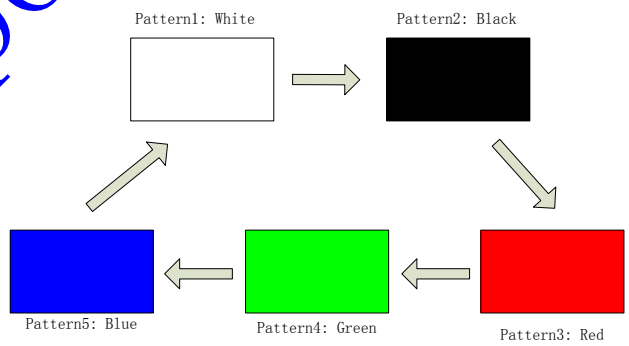


Figure 6-9 Bist mode pattern sequence

6.5 FRC/Hi-FRC function

If we display directly RGB888 video data on panel with capability of RGB666, the grey will be lost and the image's quality will be degraded. ICN6211 provides FRC/Hi-FRC functions to process the image data and provide a more attractive image performance for RGB666 panel.

6.6 DSI access local registers

6.6.1 Write local registers

There are two methods to write local registers.

These two method must be used under ESCAPE mode.

- Use Generic Short WRITE with 2 parameters(DI = 0x23)

The format is as below:

DI(0x23) + offset[7:0] + data + ECC.

Please note that the offset is only 8bits.

Also, this method can write only one data in each packet.

- Use Generic Long Write(DI = 0x29)

The format is as below:

DI(0x29) + WC[7:0] + WC[15:8] + ECC + offset[7:0] + data(1) + data(2) + …… + data(n) + CHKSUM[7:0] + CHKSUM[15:8].

where: n = WC[15:0] – 1..

In this case, the data length can be 65535 maximum.

6.6.2 Read local registers

Use Generic READ with 2 parameters(0x24), this method can be used under HS mode or ESCAPE MODE.

The format is as below:

DI(0x24) + offset[7:0] + length[7:0] + ECC.

Please note that the offset is only 8bits.

The read length can be 255 maximum.

6.7 I2C access local registers

ICN6211 support standard I2C protocol with speed up to 400K.

The chip device address is determined by the pin “ADDR” as below table:

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(W/R)
0	1	0	1	1	0	ADDR	0/1

When ADDR = 1, device address is 0x5A(Write) and 0x5B(Read);

When ADDR = 0, device address is 0x58(Write) and 0x59(Read).

following example is operation procedure with ADDR = 0.

- Write one byte to certain offset

  ST → 0x58 → ACK → OFFSET → ACK → DATA → ACK → STOP.

- Write more bytes to successive address.

  ST → 0x58 → ACK → OFFSET → ACK → DATA0 → ACK → DATA1 → …… → DATAn → ACK → STOP.

- Read data from certain offset.

  ST → 0x58 → ACK → OFFSET → ACK → RESTART → 0X59 → ACK → DATA0 → ACK → DATA1 → …… → DATAn → NACK → STOP.

7 DC and AC Electrical Characteristics

7.1 ABSOLUTE MAXIMUM RATING

		MIN	MAX	UNIT
Supply Voltage Range	VDD1 & VDD2 & VDD3	-0.3	3.66	V
Input Voltage Range	EN & SCL & SDA	-0.5	VDD1 + 0.3	V
	DSI input	-0.4	1.4	V
Storage Temperature	Ts	-65	105	℃
Electrostatic discharge	Human Body Model		±2	KV
	Charged-device model		±500	V

Note: Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device.

7.2 RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNIT
V_{DD}	VDD1 & VDD2 & VDD3 power supply	1.65		3.66	V
V_{PSN}	Supply noise on any V_{CC} pin	f(noise) > 1MHz		0.05	V
T_A	Operating free-air temperature	-40		85	℃
T_{CASE}	Case temperature			92.2	℃
V_{DSI_PIN}	DSI input pin voltage range	-50		1350	mV
$f_{(I2C)}$	Local I2C input frequency			400	KHz
f_{HS_CLK}	DSI HS clock input frequency	40		500	MHz
t_{setup}	DSI HS data to clock setup time(Figure 7-1)	0.15			UI
t_{hold}	DSI HS data to clock hold time(Figure 7-1)	0.15			UI

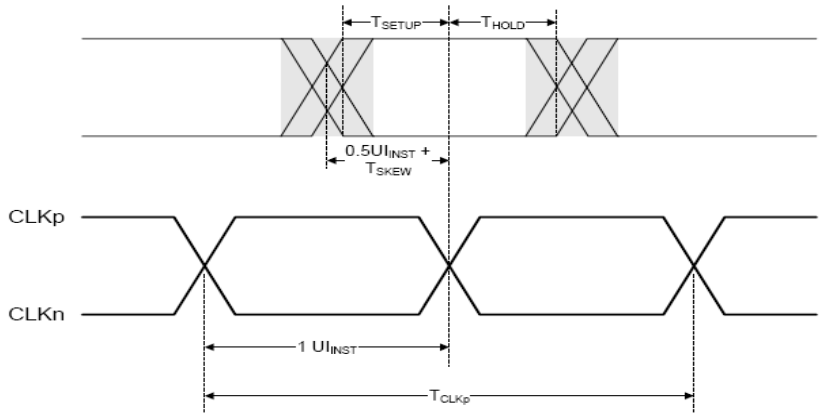


Figure 7-1 DSI HS UI timing definition

7.3 Electrical Characteristics

7.3.1 MIPI DSI INTERFACE

Refer to Figure 7-2.

parameter	Description	MIN	TYP	MAX	UNIT
V_{IL}	Low Power logic 1 input voltage	880			mV
V_{IH}	Low Power logic 0 input voltage			550	mV
$\|V_{ID}\|$	HS differential input voltage: $\|V_{dp} - V_{dn}\|$	70	200	270	mV
|VIDT|	HS differential input voltage threshold			50	mV
$V_{IL-ULPS}$	Low Power receiver logic 0 voltage, ULP state			300	mV
$V_{CMRX(DC)}$	Common-mode voltage HS receive mode	70		330	mV
$\triangle V_{CMRX(HF)}$	HS common-mode interference			100	mV
V_{IHHS}	HS single-ended input high voltage			460	mV
V_{ILHS}	HS single-ended input low voltage	-40			mV
$V_{TERM-EN}$	Single-ended threshold for HS termination enable			450	mV
Z_{ID}	Differential input impedance	80	100	124	Ω

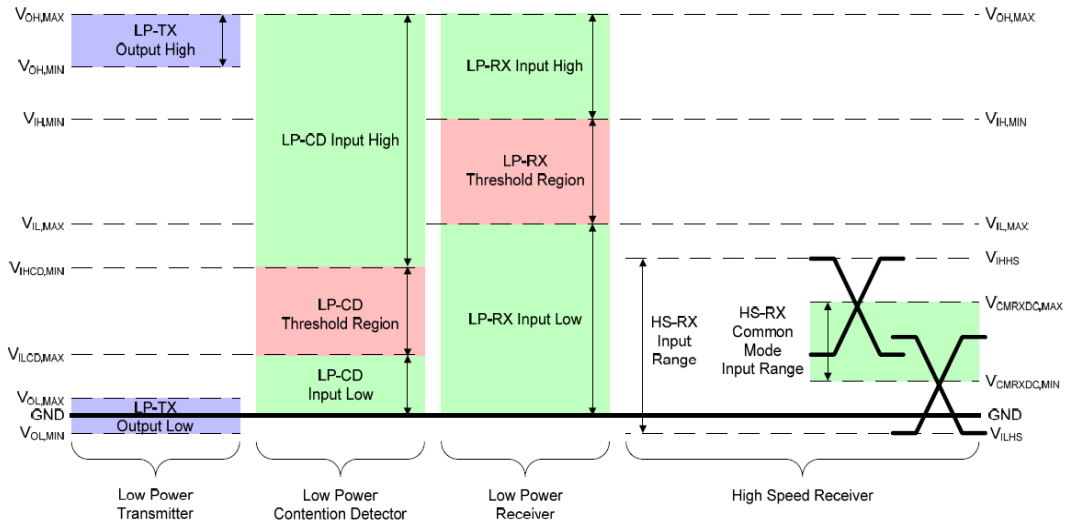


Figure 7-2 DSI HS/LP signaling and Contention Voltage

7.3.2 RGB output

parameter	Description	MIN	TYP	MAX	UNIT
VOH	output voltage, high level	0.8 * VDD3		VDD3	V
VOL	Output voltage, low level	0		0.2 * VDD3	V

7.4 SWITCHING CHARACTERISTICS

Parameter	Description	MIN	TYP	MAX	UNIT
DSI					
t_{GS}	DSI LP input pulse rejection			300	ps
RGB output (refer to Figure 7-4)					
FCLK	Output pixel clock	20		154	MHz
TCKH	Pixel clock HIGH period	40%	50%	60%	
TCKL	Pixel clock HIGH period	40%	50%	60%	
TDLY	DATA and sync signals related to PCLK	0		800	ps
REFCLK					
F_{REFCLK}	REFCLK Frequency	25		154	MHz

tr, tf	REFCLK rise and fall time	0.1		1	ns
t_{pj}	REFCLK peak-to-peak phase jitter			50	ps
Duty	REFCLK duty cycle	40%	50%	60%	
EN, ULPS, RESET (refer to Figure 7-5)					
t_{en}	Enable time from EN or ULPS			1	ms
t_{dis}	Disable time to standby			0.1	ms
t_{reset}	Reset time	10			ms

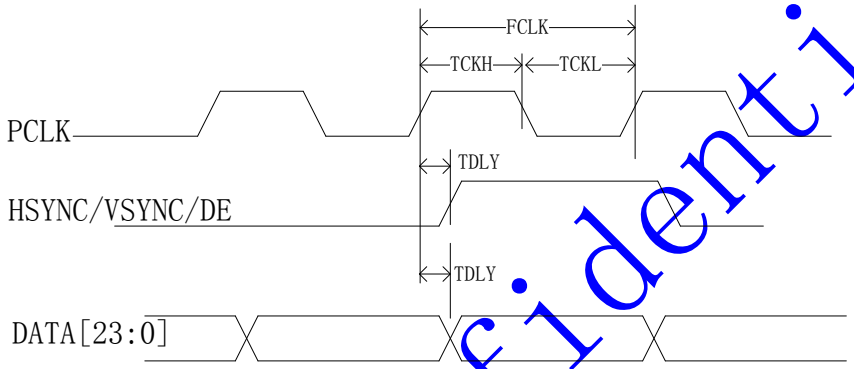


Figure 7-3 RGB output timing

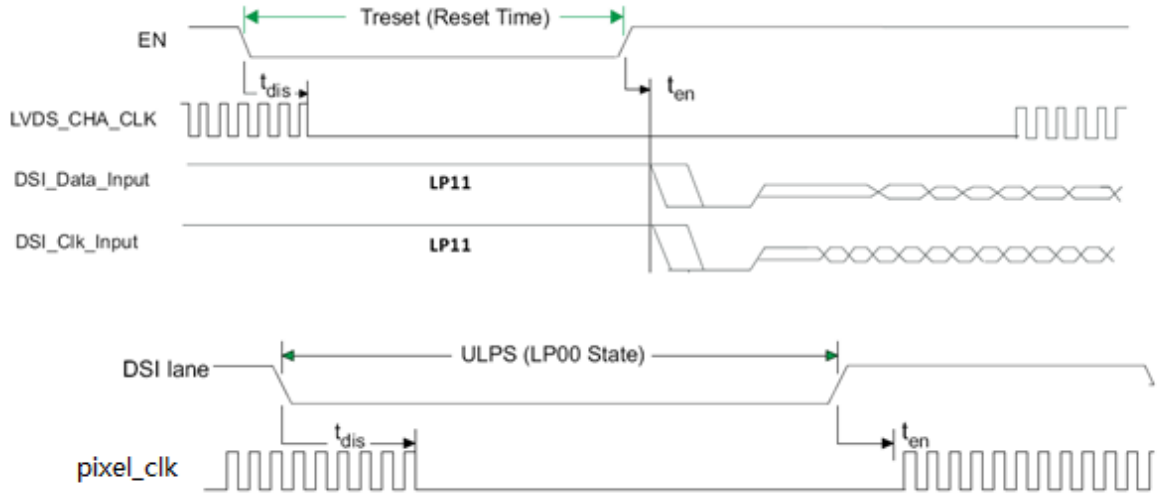
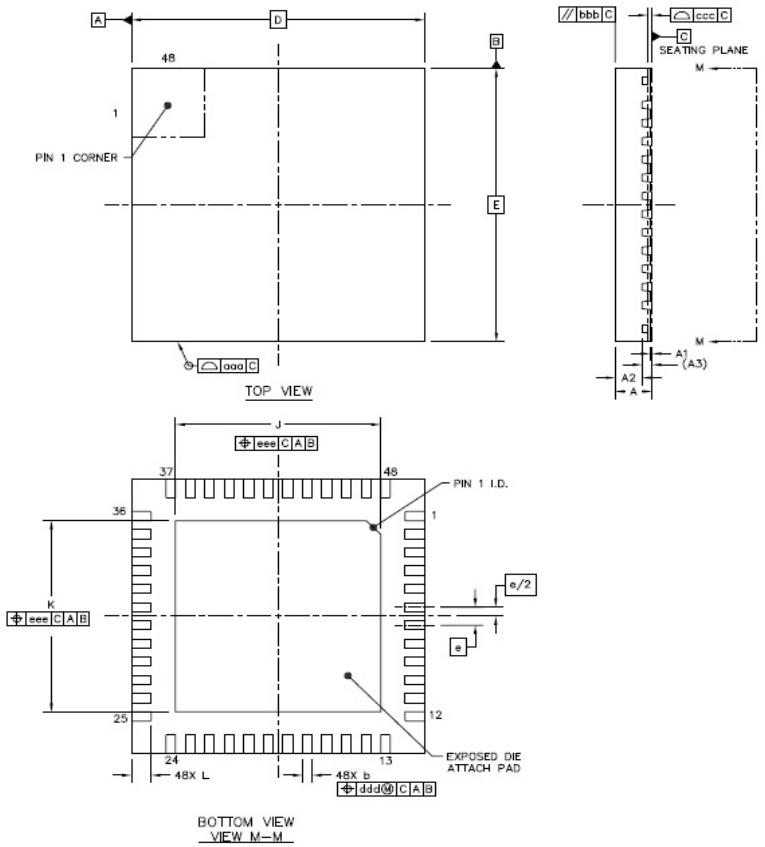


Figure 7-4 Power on and RESET and ULPS timing

8 Package information



Item	Symbol	Millimeter		
		Min	Typ	Max
Total Thickness	A	0.7	0.75	0.8
Stand Off	A1	0	0.035	0.05
Mold Thickness	A2	---	0.55	0.57
L/F Thickness	A3		0.203 REF	
Lead Width	b	0.15	0.20	0.25
Body Size	D		6 BSC	
	E		6 BSC	
Lead Pitch	e		0.4 BSC	
EP Size	J	4.1	4.2	4.3
	K	4.1	4.2	4.3
Lead Length	L	0.35	0.4	0.45
Package Edge Tolerance	aaa		0.1	
Mold Flatness	bbb		0.1	
Co Planarity	ccc		0.08	
Lead Offset	ddd		0.1	
Exposed Pad Offset	eee		0.1	

Important Notice

Chipone Technology (Beijing) Co., Ltd. (Chipone) reserves the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

Chipone warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with Chipone's standard warranty. Testing and other quality control techniques are utilized to the extent Chipone deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). CHIPONE SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF CHIPONE PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

Chipone assumes no liability for applications assistance or customer product design. Chipone does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of Chipone covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. Chipone's publication of information regarding any third party's products or services does not constitute Chipone's approval, warranty or endorsement thereof.