视频编解码芯片规格书

——AC5403 芯片

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AC5403 Features

Kernel architecture

- Dual-core 32-bit CPU
- 32KB I-Cache，24KB D-Cache，Peripherals allowed to access the DDR through the cache
- 64K on-chip SRAM
- 240MHz maximum operating frequency
- 256 interrupt sources，8-level programmable priority
- Supports external I/O interrupts
- Supports soft interrupt(virtual interrupt)，priority can be configured

Video codec

- Single way：
  2304x1440@25fps/2304x1296@30fps(H.264)
- Dual way：
  2304x1440@25fps(H.264)+VGA(MJPEG)
  1080P@30fps(H.264)+720P@30fps(H.264)
- Support M-JPEG codec，maximum support 2304x1440@25fps，4:2:0
- JPEG single resolution：2560x1920

Video input and image processing

- Maximum resolution：2304x1440
- Support CSI interface
- Support RAW8/10/12 and YUV422 data format
- Support image AWB、AE、AF
- Support image 2DNR、3DNR
- Support image enhancement processing
- Support image deinterlace
- Support image scaling
- Support Dual-way image input
- Support video realtime recording

Video output and graphics processing

- Support DSI、DBI interface
- Support CVBS output
- Support image color enhancement
- Support multi-layer image output
- Support multi-layer OSD graphics overlay
- Supports image horizontal and vertical mirroring
- Support image 90/180/270degree rotation
- Maximum resolution 720P Vertical screen

Audio codec：

- Support multi-channel、multi-protocol audio voice codec though software
- Built-in coprocessor，support a variety of post-processing sound

Audio interface：

- Support 8KHz、16KHz、32KHz、44.1KHz、48KHz and other sampling frequency

Peripheral interface：

- 41 programmable digital I/O pins
- 4 32-bit reloadable timer，can be used as timing、capture、PWM
- MC PWM
- Hardware watchdog
- 4 UART controller，of which 3 support with DMA cycle buffer
- 3 SPI host controller，support DMA
- 1 SPI FLASH interface
  -Support standard、dual、quad modes
  -Maximum support 16MB、80MHz
- 1 USB 2.0 high speed，support DMA
- 3 SDIO 2.0 interface，support DMA
- LADC controller，support 4 channels、16 data sources
- DAC controller，support left and right channels， 16bit digital DAC
- RTC，support alarm clock and time base，support wake up chip
- Support 14 IO to wake up microcontroller
- IIC controller，support master mode and slave mode
- EMI controller，support DMA transmit
- AES128 and SHA1 ENCRYPT/DECRYPT
- Built-in AVOUT

Analog peripheral features：

- 3 clock oscillation circuit
- HTC（High precision on-chip oscillator）
- High speed USB 2.0 PHY
- 5 clock generators(PLL)，provide a variety of different frequencies of the system
- 16-bit stereo audio DAC, SNR > 88 dB
- 4-channel stereo ADC with 1-channel MIC amplifier, SNR > 72 dB
- 7-channel 10-bit ADC
- 1-channel 8-level low voltage detector
- Power on reset
- 3LDO: 3.3V-1.2V，3.3V-1.8V/2.5V，3.3V-2.8V
- 2Line 1Gbps/lane DSI phy
- 2Line 1Gbps/lane CSI phy
- DDRX PHY, support DDR1 and DDR2

External memory interface：

- DDRX controller，support DDR1/DDR2、16bit data bit-wide，DDR1 fastest support 250MHz，DDR2 fastest support 400MHz
  -Maximum support 64MB

Supply Voltage：

符号	参数	最小	典型	最大	单位
VDDIO	IO Power	3.0	3.3	3.6	V
SVDD1/2/3	IO Power	3.0 1.7	3.3 1.8	3.6 1.9	V
DRVDD	DDR2 Power	1.7	1.8	1.9	V
DRVDD	DDR1 Power	2.3	2.5	2.7	V
VDD	Core Power	1.08	1.2	1.32	V

注：SVDD1 为 IO（PB5-PB10、PB14、PB15）的电源;
SVDD2 为 IO（PA11-PA14、PB0、PB1、PE0、PE1）的电源;
SVDD3 为 IO（PG2、PG8-PG15）的电源.

- 工作温度 (-40℃ 至 +85℃)
- 存储温度（-65℃ 至 +150℃）

Package：

- QFN88(10mm X 10mm)

一、引脚定义

1.1 引脚分配

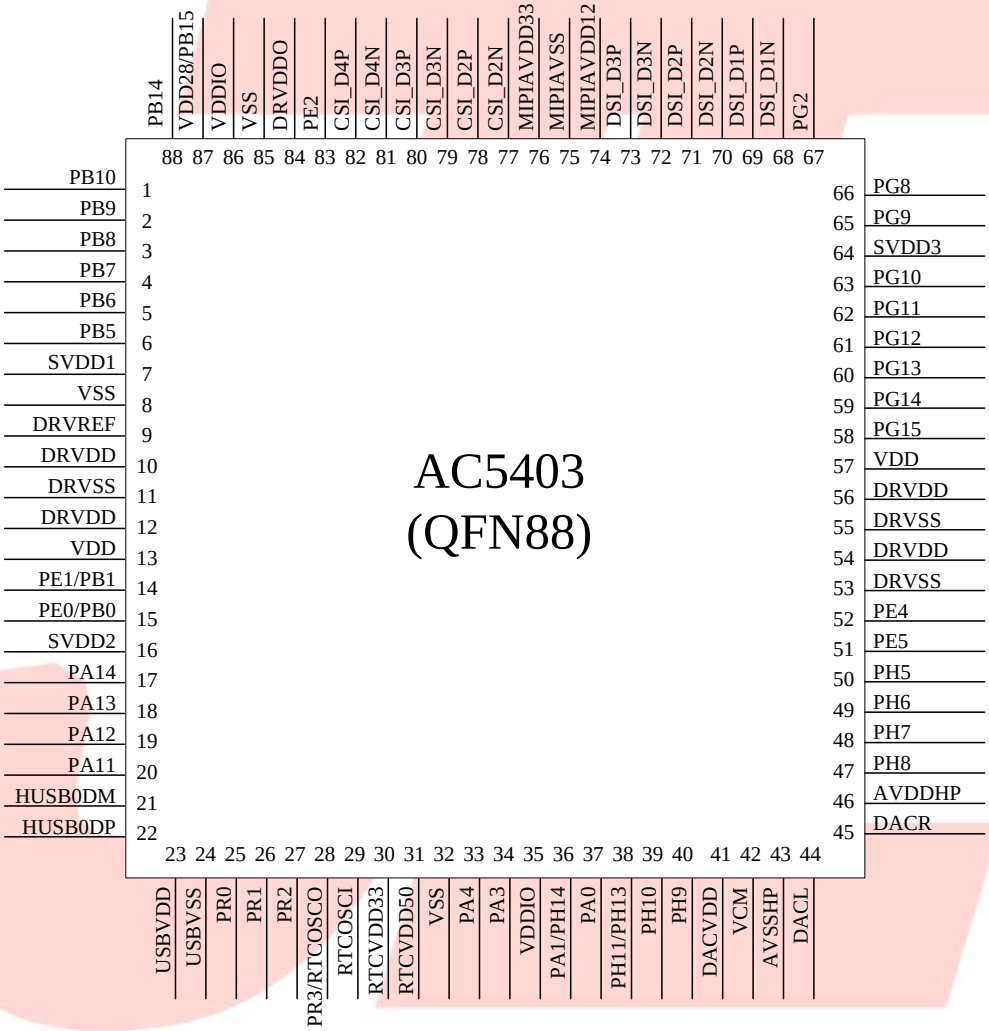


图 1-1 AC5403 _QFN88 引脚分配图

1.2 引脚描述

表 1-1 AC5403 _QFN88 引脚描述

Pin#	Name	I/O Type	Function	Other Function
1	PB10	I/O	GPIO	SPI2_DAT3B(3)：SPI2 Data3 (B) SD1_DAT1C：SD1 Data1 (C)
2	PB9	I/O	GPIO	SPI2_CLKB：SPI2 Clock (B) SD1_DAT0C：SD1 Data0 (C)
3	PB8	I/O	GPIO	SPI2_DOB(0)：SPI2 Data Out (B) SD1_CLKC：SD1 Clock (C)
4	PB7	I/O	GPIO	SPI2_DAT2B(2)：SPI2 Data2 (B) SD1_CMDC：SD1 CMD (C)
5	PB6	I/O	GPIO	SPI2_DIB(1)：SPI2 Data In (B) SD1_DAT3C：SD1 Data3 (C)
6	PB5	I/O	GPIO	SPI2_CSB：SPI2 Chip Select(B) SD1_DAT2C：SD1 Data2 (C)
7	SVDD1	P	IO Power1	——
8	VSS	P	Digital Ground	——
9	DRVREF	P	DDR REF	——
10	DRVDD	P	DDR Power	——
11	DRVSS	P	DDR Ground	——
12	DRVDD	P	DDR Power	——
13	VDD	P	Core Power	——
14	PB1	I/O	GPIO	IIC_SDA1_A：IIC1 SDA (A)
	PE1	I/O	GPIO	SD0_DAT1D：SD0 Data1 (D) UART3_RXA：Uart3 Data In (A)
15	PB0	I/O	GPIO	IIC_SCL1_A：IIC1 SCL (A)
	PE0	I/O	GPIO	SD0_DAT0D：SD0 Data0 (D) UART3_TXA：Uart3 Data Out (A)
16	SVDD2	P	IO Power2	——
17	PA14	I/O	GPIO	ALNK_WSB：Audio Link WS (B) SD0_CLKD：SD0 Clock (D)
18	PA13	I/O	GPIO	ALNK_CKB：Audio Link Clock (B) SD0_CMDD：SD0 CMD (D)

19	PA12	I/O	GPIO	ALNK_D3B: Audio Link Data3 (B) SDO_DAT2D: SDO Data2 (D)
20	PA11	I/O	GPIO	ALNK_D2B: Audio Link Data2 (B) SDO_DAT3D: SDO Data3 (D)
21	HUSBODM	I/O	HUSBODM	——
22	HUSBODP	I/O	HUSBODP	——
23	USBVDD	P	USB Power	——
24	USBVSS	P	USB Ground	——
25	PR0	I/O	RTC IO	PINR: PIN Reset
26	PR1	I/O	RTC IO	PINR: PIN Reset ADC13: ADC Input Channel 13
27	PR2	I/O	RTC IO	PINR: PIN Reset(Default) ADC12: ADC Input Channel 12
28	PR3	I/O	RTC IO	PINR: PIN Reset
	RTCOSCO	I/O	RTC OSCO	——
29	RTCOSCI	I/O	RTC OSCI	——
30	RTCVDD33	P	RTC Power	——
31	RTCVDD50	P	RTC Power	——
32	VSS	P	Digital Ground	——
33	PA4	I/O	GPIO	SPIO_CLKA: SPIO Clock (A) SFC_CLK: SFC Clock
34	PA3	I/O	GPIO	SPIO_DOA(0): SPIO Data Out (A) SFC_DO(0): SFC Data Out
35	VDDIO	P	IO Power	——
36	PA1	I/O	GPIO	IIC_SDA1_B: IIC1 SDA (B) SPIO_DIA(1): SPIO Data In (A) SFC_DI(1): SFC Data In
	PH14	I/O	GPIO	UART1_TXC: Uart1 Data Out (C) ADC10: ADC Channel 10 CLKOUT1: Clock Out1 IIC_SDA0_B: IIC0 SDA (B) Wakeup14: Port Wakeup 14 SPI1_DOC(0): SPI1 Data Out (C)
37	PA0	I/O	GPIO	SPIO_CSA: SPIO Chip Select (A) SFC_CS: SFC Chip Select

38	PH13	I/O	GPIO	UART0_RXC: Uart0 Data In (C) AVOUT: AV Output TMR3: Timer3 Clock In SPI1_DIC(1): SPI1 Data In (C)
	PH11	I/O	GPIO	MICR: MIC Right Channel SD1_DAT0A: SD1 Data0 (A)
39	PH10	I/O	GPIO	AMUX1R: Simulator Channel 1 Right SD1_CLKA: SD1 Clock (A) Wakeup13: Port Wakeup 13 UART2_TXB: Uart2 Data Out (B)
40	PH9	I/O	GPIO	AMUX1L: Simulator Channel 1 Left SD1_CMDA: SD1 CMD (A) UART2_RXB: Uart2 Data In (B)
41	DACVDD	P	DAC Power	———
42	VCM	P	VCM	———
43	AVSSHP	P	Head Phone Ground	———
44	DACL	O	DAC Left Channel	DACL
45	DACR	O	DAC Right Channel	DACR
46	AVDDHP	P	Head Phone Power	———
47	PH8	I/O	GPIO	AMUX0R: Simulator Channel 0 Right SD1_DAT3A: SD1 Data3 (A)
48	PH7	I/O	GPIO	AMUX0L: Simulator Channel 0 Left SD1_DAT2A: SD1 Data2 (A) Wakeup12: Port Wakeup 12
49	PH6	I/O	GPIO	MICL:MIC Left Channel
50	PH5	I/O	GPIO	UART1_RXB: Uart1 Data In (B) SD1_DAT1A: SD1 Data1 (A)
51	PE5	I/O	GPIO	ADC8: ADC Channel 8 IIC_SDA1_D: IIC1 SDA (D) SPI1_DOA(0): SPI1 Data Out (A) Wakeup11: Port Wakeup 11

52	PE4	I/O	GPIO	IIC_SCL1_D: IIC1 SCL (D) SPI1_CLKA: SPI1 Clock (A) Wakeup10: Port Wakeup 10
53	DRVSS	P	DDR Ground	——
54	DRVDD	P	DDR Power	——
55	DRVSS	P	DDR Ground	——
56	DRVDD	P	DDR Power	——
57	VDD	P	Core Power	——
58	PG15	I/O	GPIO	LCD_DAT15A: LCD Data15 (A) EMI_D15A: EMI Data15 (A)
59	PG14	I/O	GPIO	LCD_DAT14A: LCD Data14 (A) EMI_D14A: EMI Data14 (A)
60	PG13	I/O	GPIO	LCD_DAT13A: LCD Data13 (A) EMI_D13A: EMI Data13 (A) MC PWM_H3_A SD2_DAT1B: SD2 Data1 (B)
61	PG12	I/O	GPIO	LCD_DAT12A: LCD Data12 (A) EMI_D12A: EMI Data12 (A) MC PWM_L3_A SD2_DAT0B: SD2 Data0 (B)
62	PG11	I/O	GPIO	LCD_DAT11A: LCD Data11 (A) EMI_D11A: EMI Data11 (A) MC PWM_H2_A SD2_CLKB: SD2 Clock (B)
63	PG10	I/O	GPIO	LCD_DAT10A: LCD Data10 (A) EMI_D10A: EMI Data10 (A) MC PWM_L2_A SD2_CMDA: SD2 CMD (A)
64	SVDD3	P	IO Power3	——
65	PG9	I/O	GPIO	LCD_DAT9A: LCD Data9 (A) EMI_D9A: EMI Data9 (A) MC PWM_H1_A SD2_DAT3B: SD2 Data3 (B)
66	PG8	I/O	GPIO	LCD_DAT8A: LCD Data8 (A) EMI_D8A: EMI Data8 (A) MC PWM_L1_A SD2_DAT2B: SD2 Data2 (B)
67	PG2	I/O	GPIO	LCD_DENAB: LCD Data Enable EMI_WRAB: EMI Write

68	DSI_D1N	O	MIPI DSI lane	MIPI DSI data (0/1) lane (p/n) MIPI DSI clock lane (p/n)
69	DSI_D1P	O	MIPI DSI lane	MIPI DSI data (0/1) lane (p/n) MIPI DSI clock lane (p/n)
70	DSI_D2N	O	MIPI DSI lane	MIPI DSI data (0/1) lane (p/n) MIPI DSI clock lane (p/n)
71	DSI_D2P	O	MIPI DSI lane	MIPI DSI data (0/1) lane (p/n) MIPI DSI clock lane (p/n)
72	DSI_D3N	O	MIPI DSI lane	MIPI DSI data (0/1) lane (p/n) MIPI DSI clock lane (p/n)
73	DSI_D3P	O	MIPI DSI lane	MIPI DSI data (0/1) lane (p/n) MIPI DSI clock lane (p/n)
74	MIPIAVDD12	P	MIPI AVDD	——
75	MIPIAVSS	P	MIPI AVSS	——
76	MIPIAVDD33	P	MIPI Power	——
77	CSI_D2N	I	MIPI CSI lane	MIPI CSI clock lane (p/n)
78	CSI_D2P	I	MIPI CSI lane	MIPI CSI clock lane (p/n)
79	CSI_D3N	I	MIPI CSI lane	MIPI CSI data (0/1) lane (p/n)
80	CSI_D3P	I	MIPI CSI lane	MIPI CSI data (0/1) lane (p/n)
81	CSI_D4N	I	MIPI CSI lane	MIPI CSI data (0/1) lane (p/n)
82	CSI_D4P	I	MIPI CSI lane	MIPI CSI data (0/1) lane (p/n)
83	PE2	I/O	GPIO	VPP CLKOUT0: Clock Out0 IIC_SCL1_C: IIC1 SCL (C)
84	DRVDD0	P	DDR Power Output	——
85	VSS	P	Digital Ground	——
86	VDDIO	P	IO Power	——
87	VDD28	P	AVDD28	——
	PB15	I/O	GPIO	UART0_RXD: Uart0 Data In (D) OSC02

88	PB14	I/O	GPIO	UART0_TXD：Uart0 Data Out（D） OSCI2 TMR0：Timer0 Clock In ADC4：ADC Channel 4 Wakeup9：Port Wakeup 9

（★说明：1、P----Power Supply　　2、I----Input　　3、O----Output　　4、I/O----Bi-direction）

二、电气特性

2.1 IO 输入、输出高低逻辑特性

表 2-1

输入特性						
符号	参数	最小	典型	最大	单位	测试条件
V_{IL}	Low-Level Input Voltage	-0.3	–	0.3* VDDIO	V	VDDIO = 3.3V
V_{IH}	High-Level Input Voltage	0.7* VDDIO	–	VDDIO+0.3	V	VDDIO = 3.3V
输出特性						
V_{OL}	Low-Level Output Voltage	–	–	0.1* VDDIO	V	VDDIO = 3.3V
V_{OH}	High-Level Output Voltage	0.9* VDDIO	–	–	V	VDDIO = 3.3V

2.2 IO 输出能力、上下拉电阻特性

表 2-2

Port 口	输出能力	上拉电阻	下拉电阻	备注
PA0、PA1 PA3、PA4 PA11 - PA14 PB0、PB1 PB5 - PB10 PB14、PB15 PE0、PE1 PE4、PE5 PG2 PG8 - PG15 PH5 - PH11 PH13、PH14	强驱：24mA 弱驱：8mA	10K	60K	——
PE2	8mA（无强弱驱之分）	10K	10K	——
PR0-PR3	8mA(片内串接 200Ω电阻)	10K	60K	RTC 模块需供电

（★说明：上下拉电阻的精度约为±20%)

2.3 DAC 特性

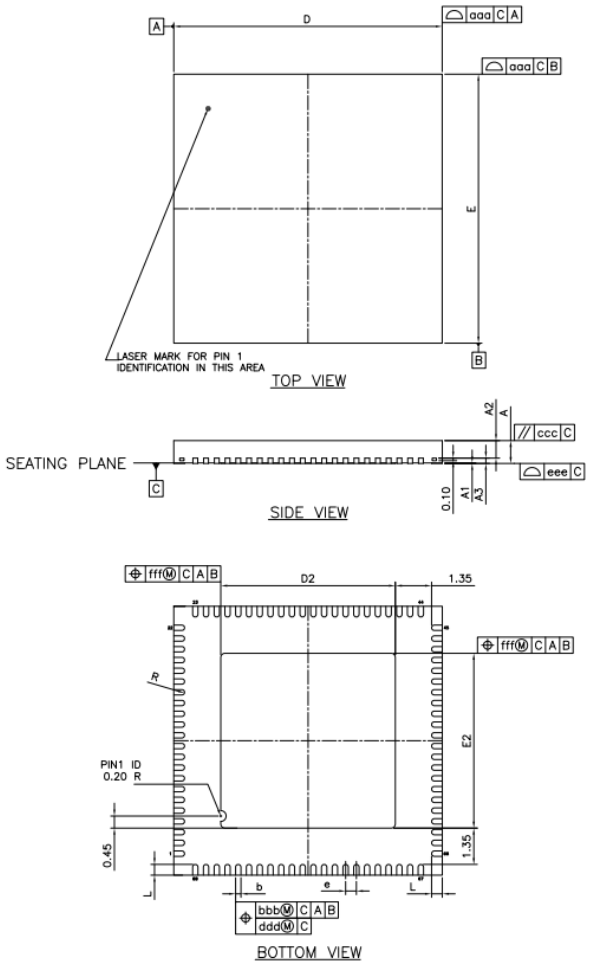
表 2-3

符号	参数	最小	典型	最大	单位	测试条件
SNR	Signal to Noise Ratio		94		dB	1KHz,SR=44.1KHz,静音文件, DACVDD with 1u cap
THD+N	Total Harmonic Distortion+ Noise		-75		dB	1KHz,SR=44.1KHz, DACVDD with 1u cap

三、封装

3.1 QFN_88PIN 封装图

图 3-1 AC5403_QFN88 封装图



Item		Symbol	MIN.	NOM.	MAX.
total height		A	0.80	0.85	0.90
stand off		A1	0.00	0.02	0.05
mold thickness		A2	0.60	0.65	0.70
leadframe thickness		A3		0.20 REF.	
lead width		b	0.15	0.20	0.25
package size	X	D	9.90	10.00	10.10
	Y	E	9.90	10.00	10.10
E-PAD size	X	D2	6.40	6.50	6.60
	Y	E2	6.40	6.50	6.60
lead length		L	0.30	0.40	0.50
lead pitch		e		0.40 bsc	
lead arc		R	0.075	---	---
Package profile of a surface		aaa		0.10	
Lead position		bbb		0.07	
Parallelism		ccc		0.10	
Lead position		ddd		0.05	
Lead profile of a surface		eee		0.08	
Epad position		fff		0.10	

四、版本信息

日期	版本号	描述
2017.07.12	V1.0	原始版本。