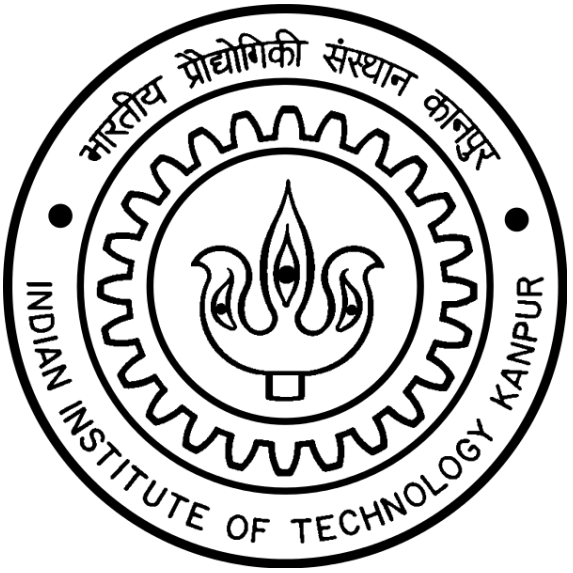
Gilbert Cell
Design and Layout



EE610A Course Project

Course Guide - Prof. Shafi Qureshi

Department of Electrical Engineering Indian Institute of Technology Kanpur

Submitted by:

Prateek Yadav (14492)

Jishant Singh (14288)

Acknowledgement

In this course project we needed Mentor Graphics EDA tools to design, simulate, make layout the analog circuit. For the same we acknowledge Prof. S. Qureshi, Mr. Dinesh and the VLSI/EDA lab resources and all the help provided in the project duration for lab demos and debugging various errors faced while making this project.

Abstract

A gilbert cell is Variable Gain Amplifier used in various communication systems. We aim to get used to the actual analog circuit design by employing circuit design techniques learnt in the course EE610A and make layout of this gilbert cell using TSMC 180nm technology.

Introduction

Gilbert cell is a Variable Gain Amplifier (VGA). It has a control voltage that is used to directly vary the gain of the differential amplifier. It is based on the observations that (a) small signal gain of the differential amplifier is a direct function of the tail current (I_{ss}), (b) we can steer the tail current into one of the differential pairs via control of the two transistors. The gain varies from 0 to maximum value which is defined by voltage headroom limitations. VGAs typically find applications in scenarios where the signal amplitude has a large variance, and hence require inverse changes in the gain which should be a handy control. More generally Gilbert cell is put to use as a mixer which is an analog voltage multiplier. It finds a wide application in the field of RF and communication systems for frequency transformation.

Functionality

A basic schematic of the discussed circuit is provided below (*Fig 2.1 - Fig 2.4*), which shows the inverted differential output points of two different VGA modules.

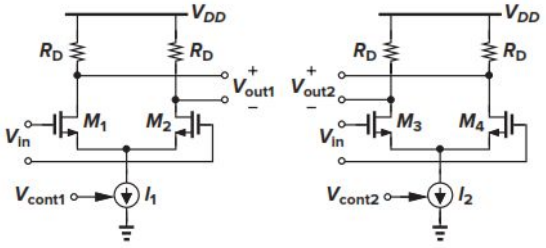


Figure 2.1 *Two stages providing variable gain.*

The above two VGA modules can be joined together to have a single double ended output as per the topology shown in Figure 2.2.

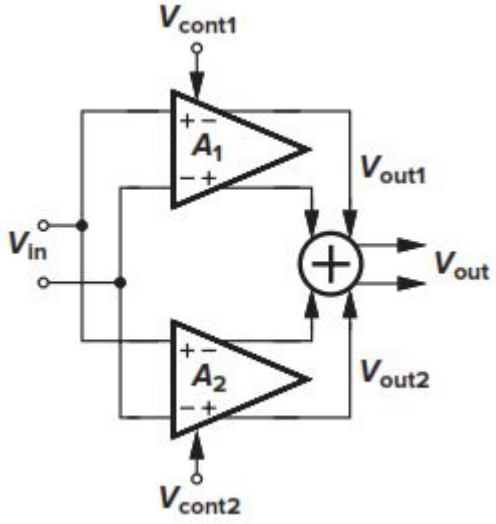


Figure 2.2 *Summation of output voltages of two differential amplifiers.*

Putting up the VGAs according to the above topology leads us to the circuit shown in Figure 2.3.

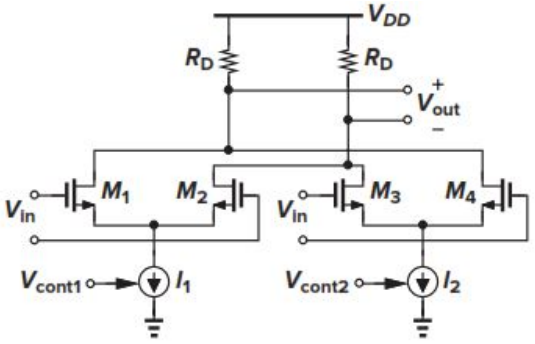


Figure 2.3 *Summation of two differential amplifiers in current domain.*

Above circuits requires two different current sources, which is quite redundant. To avoid this redundancy, a differential control voltage is introduced in the final gilbert cell topology as shown in Figure 2.4

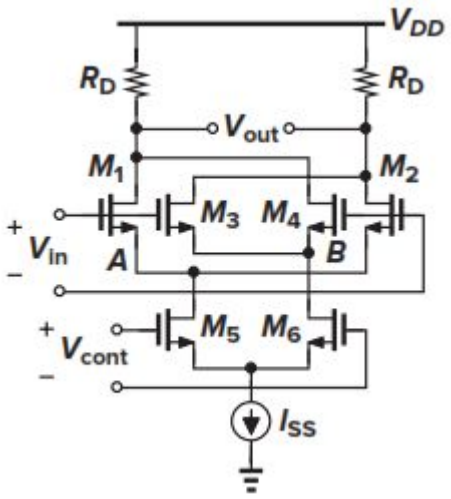


Figure 2.4 *Final Gilbert cell topology*

We provide V_{cont} such that either M_5 or M_6 operates. When M_5 operates then M_1-M_2 are active and when M_6 operates then M_3-M_4 are active for differential amplification of input signal V_{in}. In the above shown cascode structure of gilbert cell, it consumes a greater voltage headroom than a simple differential pair.

Design

Our motive was to design a layout for a Gilbert Cell. Hand analysis of the circuit suggested that resistances R_D is required to be of the order of 100kΩs. Hence passive resistor was not an efficient choice from the perspective of a compact layout. Active components were therefore used. P-MOS in diode connected configuration were used which gave a resistance of $(1/g_{mp} || r_o)$. Differential voltage gain formula is given by (for +ve control voltage, for -ve control voltage the gain sign is +ve)

$$A_{DM} = -\frac{g_{m,N}}{g_{m,P}} \quad \textit{[Eq. 1]}$$

Transconductance of the NMOS is given by

$$g_{m,N} = \sqrt{\mu_n C'_{ox} \frac{W}{L} I_{ss}} \quad \textit{[Eq. 2]}$$

and that of the PMOS is given by

$$g_{m,P} = \sqrt{\mu_p C'_{ox} \frac{W}{L} I_{ss}} \quad \textit{[Eq. 3]}$$

So for our design, the effective voltage gain reduces to

$$A_{DM} = -\sqrt{\frac{\mu_n W_N}{\mu_p W_P}} \quad \textit{[Eq. 4]}$$

(In all the above equation, symbols have their usual meaning as used in analog circuit coursework)

Although the I_{SS} doesn't appear in gain formula, but this effect the voltage overdrive requirements.

A current mirror configuration is used to emulate a constant current source. We used a basic topology for current mirror (Fig. 2.5), in which current flowing through M_1 is mirrored in M_2. For the I_{ref} we have used a PMOS.

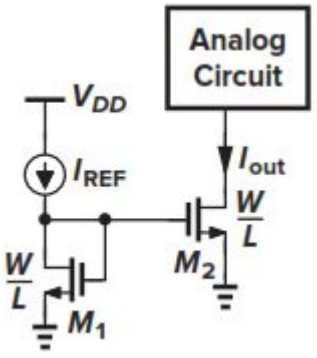


Figure 2.5 *Basic current mirror topology*

Using this topology we can have multiple current sources derived from this single current source reference and those too with different current as dictated by the below equation (in reference to Fig 2.5)

$$I_{out} = \frac{(W/L)_2}{(W/L)_1} I_{REF} \qquad \textit{[Eq. 5]}$$

Design Parameters

Following are the values of various parameters used in design

A_{DM} = 2.43 (V/V)

(W_P = 40λ , W_N = 100λ, μ_n=218 μA/V², μ_p=92 μA/V²)

Current Source parameters

Iref = 194.46 μA (MOS Dimensions given in schematic)

I_{SS} = (⅔)*Iref

Layout

Layout making can be a tedious task if the MOSFET sizes are very large. So we employed various techniques to make the MOSFET of squarish shape, which leads to minimum area of the overall layout.

Images

Images of various processes of circuit design is shown on next pages.

Conclusion

So in our design of gilbert cell we got to know about many design challenges and successfully made a gilbert cell with following parameters .

Area of design: 260 (μm)²

Gain: 2.43 (V/V)

Power Dissipation: 512 μW

VDD: 1.8V

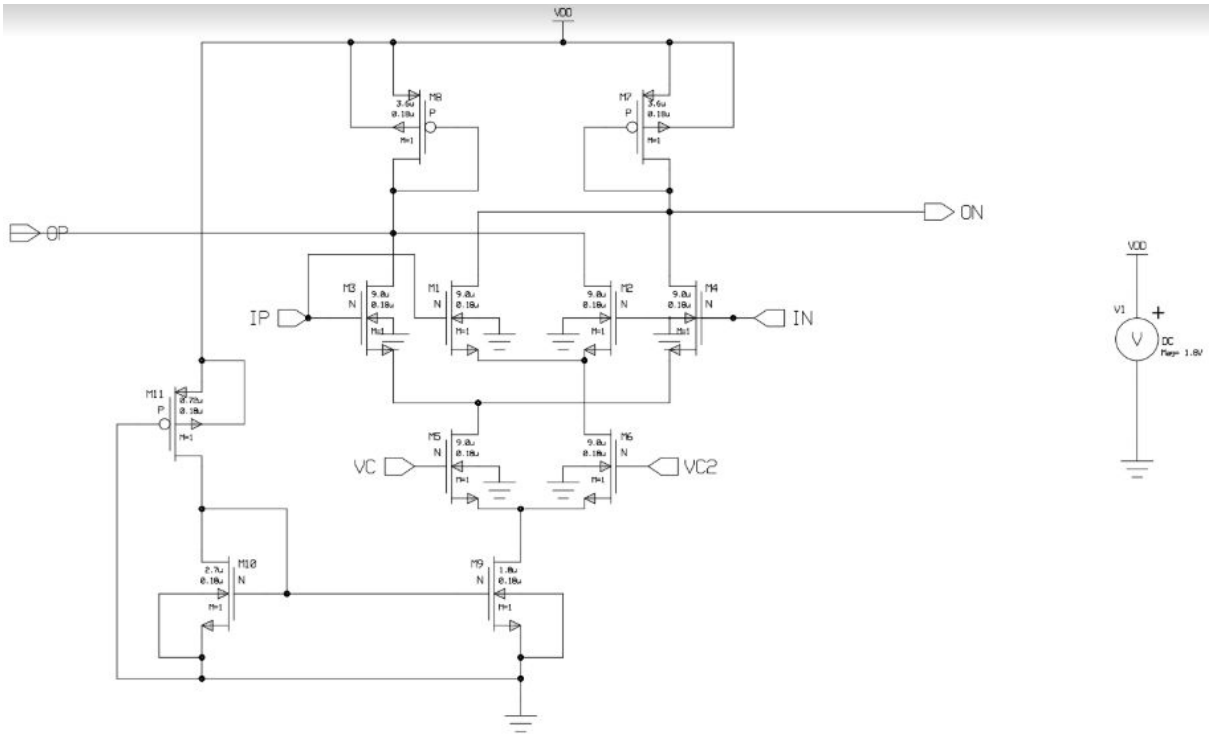


***Image 1**: Design Schematic*

***Image 2**: Circuit Layout*

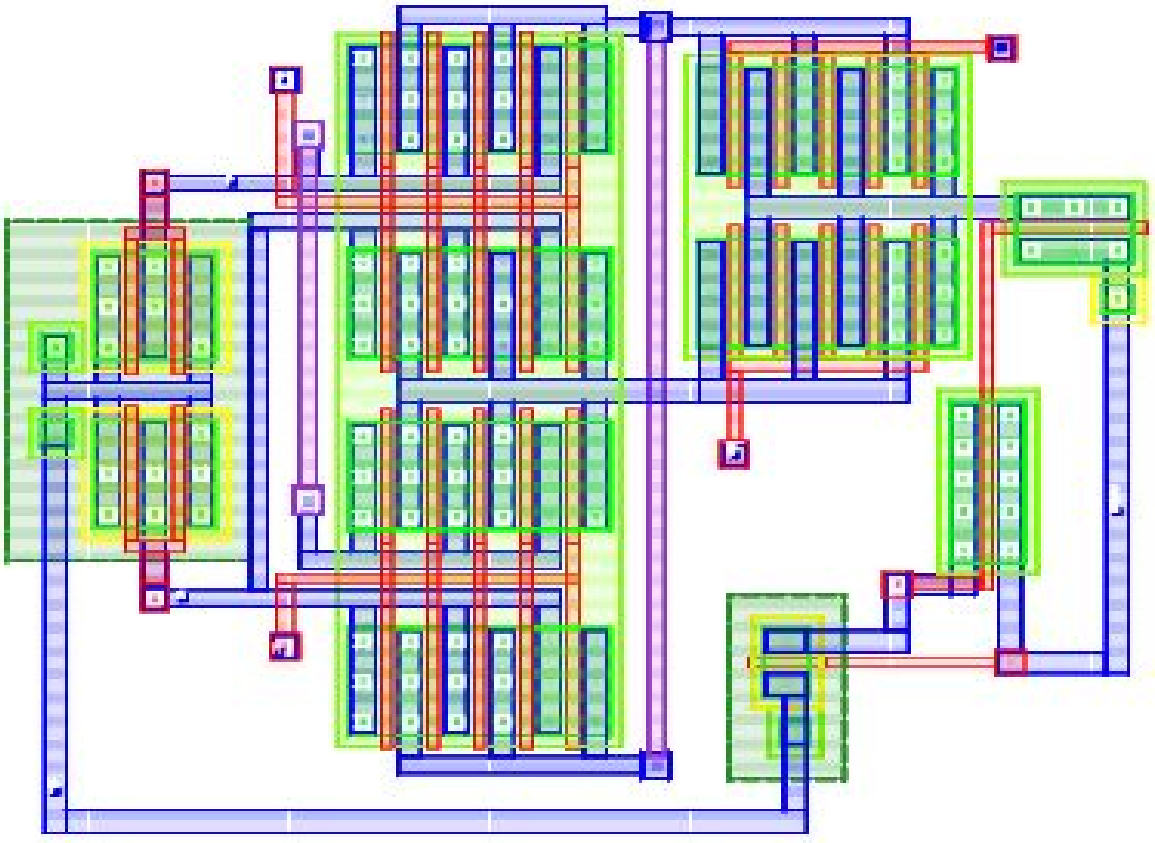


***Image 3**: PEX generation output*

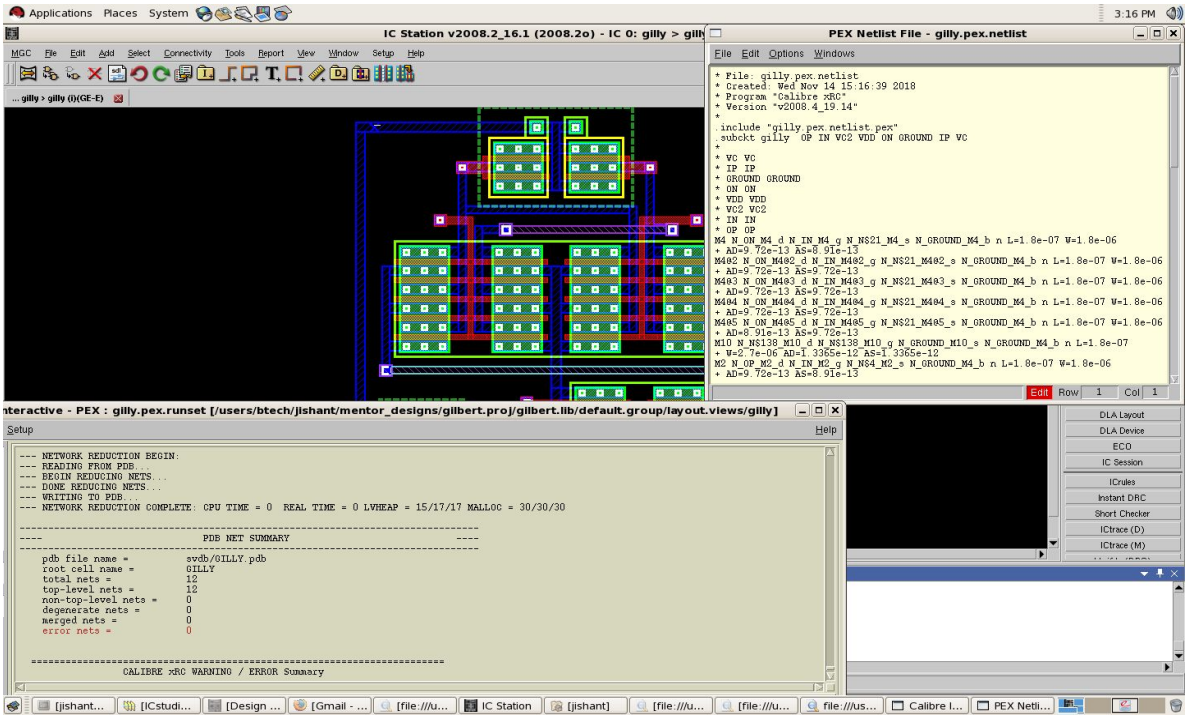
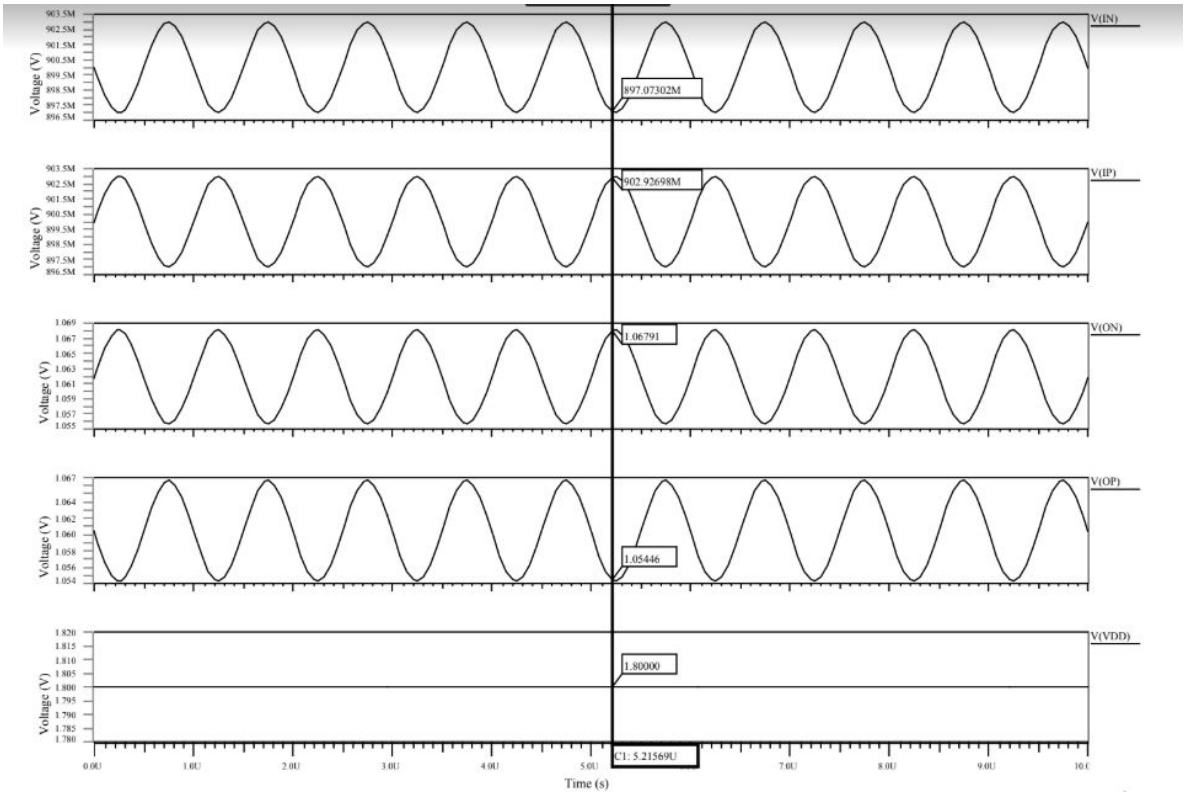


***Image 4**: Final Simulation*



References

- Ieeexplore.ieee.org. (2018). *Design of High Gain and Low Noise CMOS Gilbert Cell Mixer for Receiver Front End Design - IEEE Conference Publication*. [online] Available at: https://ieeexplore.ieee.org/document/7966800 [Accessed 14 Nov. 2018].
- Razavi, B. (2017). *Design of analog CMOS integrated circuits*. New York, NY: McGraw-Hill Education.