TWO BIT RIPPLE CARRY ADDER

DESIGN AND LAYOUT

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INTRODUCTION

In this project, we have attempted to design a 2-bit ripple carry adder. The function of this adder is to take two 2-bit numbers as inputs and compute their arithmetic sum. The objectives of this work are, first, to design the circuit of the aforementioned adder by sizing the transistors to achieve a fine balance between the propagation delay and the chip area, and second, to create an area efficient layout of the circuit. We have used standard logic gates like AND, OR, XOR, and the CMOS inverter to realize the circuit. Here, a 1-bit half adder is used to feed the carry bit to a 1-bit full adder, and the outputs of both these 1-bit adders is the arithmetic sum in binary format. We have simulated both the schematic and the layout with an extensive testbench. Approximate chip area has been calculated. We shall show the results of our work later in this report.

METHODOLOGY

As mentioned earlier, the circuit that we have implemented consists of the following logic gates:

I. AND
II. OR
III. XOR
IV. NOT

We have two 2-bit numbers A_1A_0, and B_1B_0 respectively. The minimum number of bits in the arithmetic sum can be three. Hence, it is safe to assume the sum to be $S_2S_1S_0$.

The first half of the circuit is a 1-bit half adder. It takes in the least significant bits of both the numbers, i.e., A_0 and B_0, and calculates their arithmetic sum, which at max can be 2 bits long. Let us say the sum is C_1S_0. This S_0 is the right most digit of the main arithmetic sum that we need to calculate. The second digit C_1 is then fed into the 1-bit full adder.

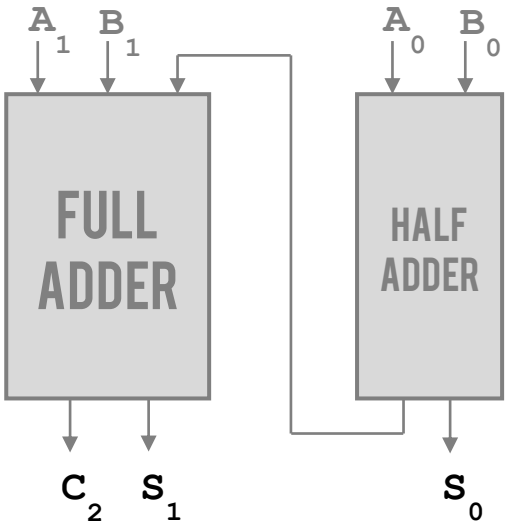


Figure 1. Block diagram of ripple carry adder

The logic level circuit of the 1-bit half adder is as shown.

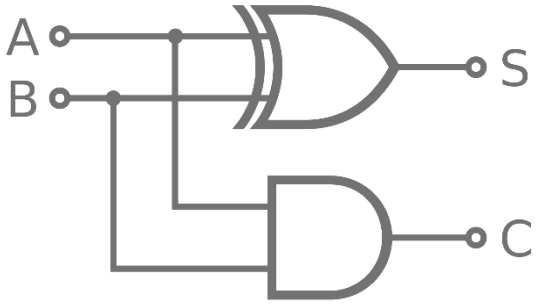


Figure 2. 1-bit half adder logic

The 1-bit full adder computes the arithmetic sum of the 2 input bits (A_1 and B_1), as well as the carry bit C_1. The resulting output is a 2-bit number C_2S_1. In our case, the bit C_2 acts as S_2. The logic level circuit of the 1-bit full adder is shown as follows.

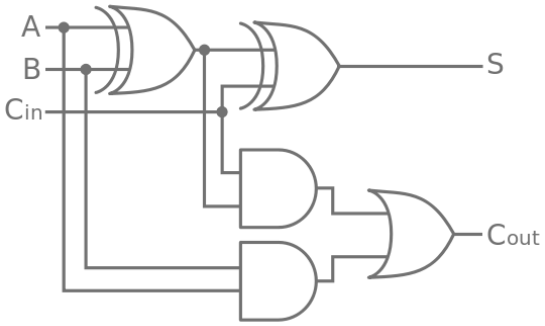


Figure 3. 1-bit full adder logic

SIZING

The minimum sized NMOS transistor that we took has a W/L ratio of 2.50. All the other transistors have been sized in proportion to this basic ratio, to achieve worst case delay not more than that of a minimum sized complementary CMOS inverter.

We have assumed,

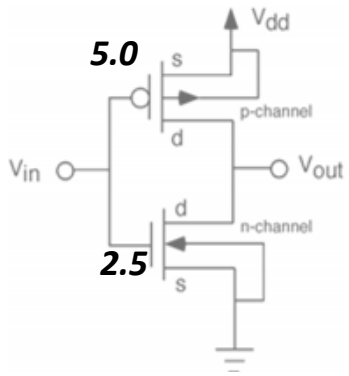
$$k_p' = k_n'/2$$

Hence, the ratio of W/L of a minimum sized PMOSFET and a minimum sized NMOSFET, such that they have identical resistances is,

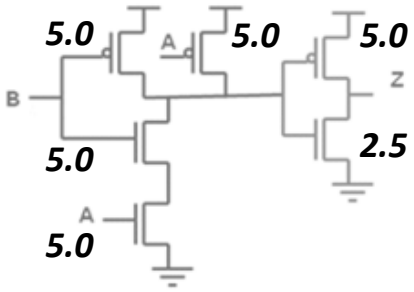
$$\beta = 2$$

Now, we will discuss the optimal sizing of each logic gate separately.

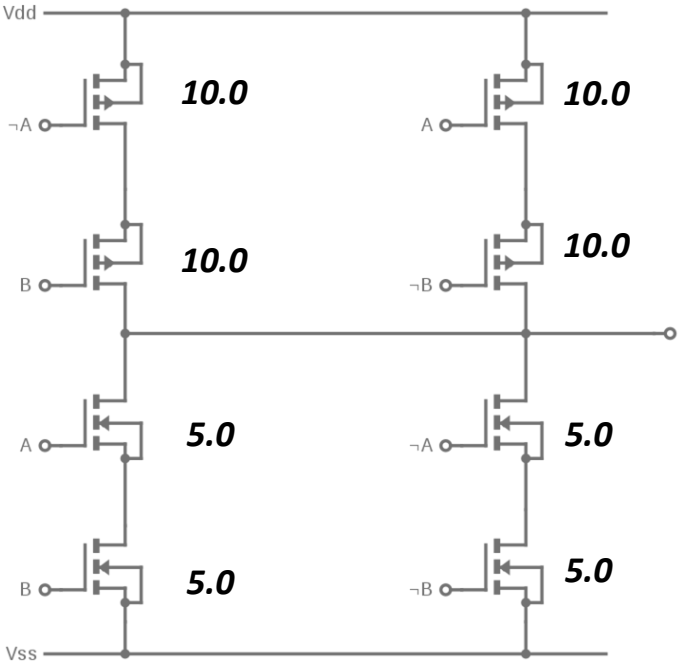
I. INVERTER



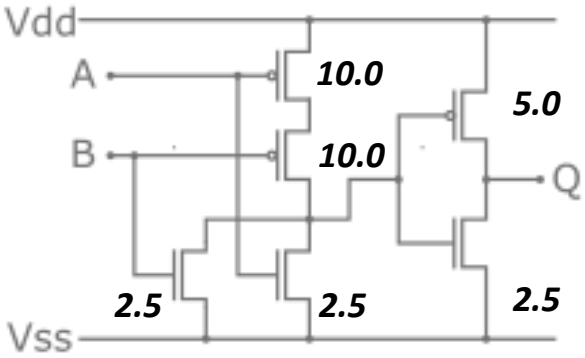
II. AND



III. XOR



IV. OR



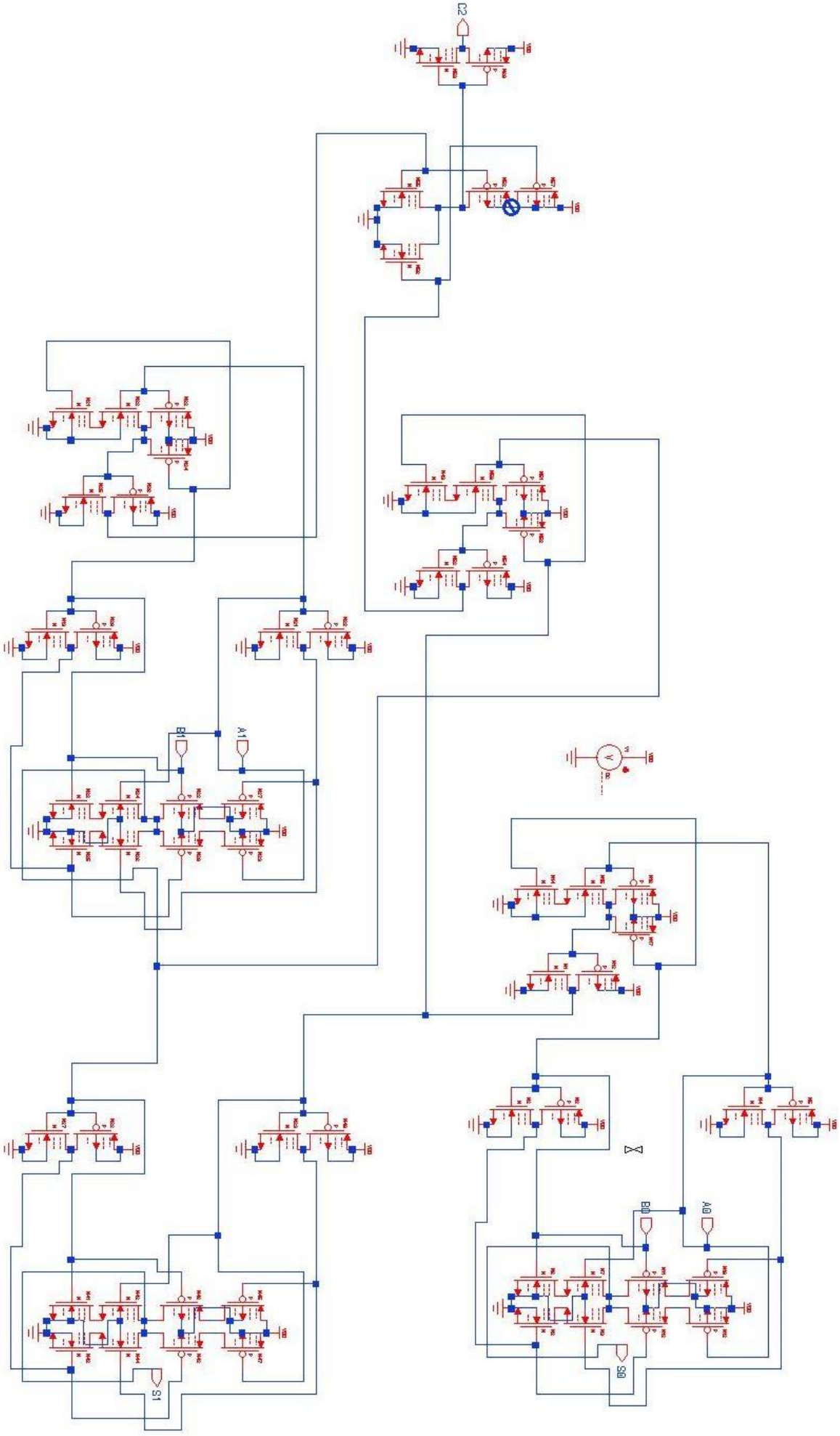


Figure 4. Circuit schematic

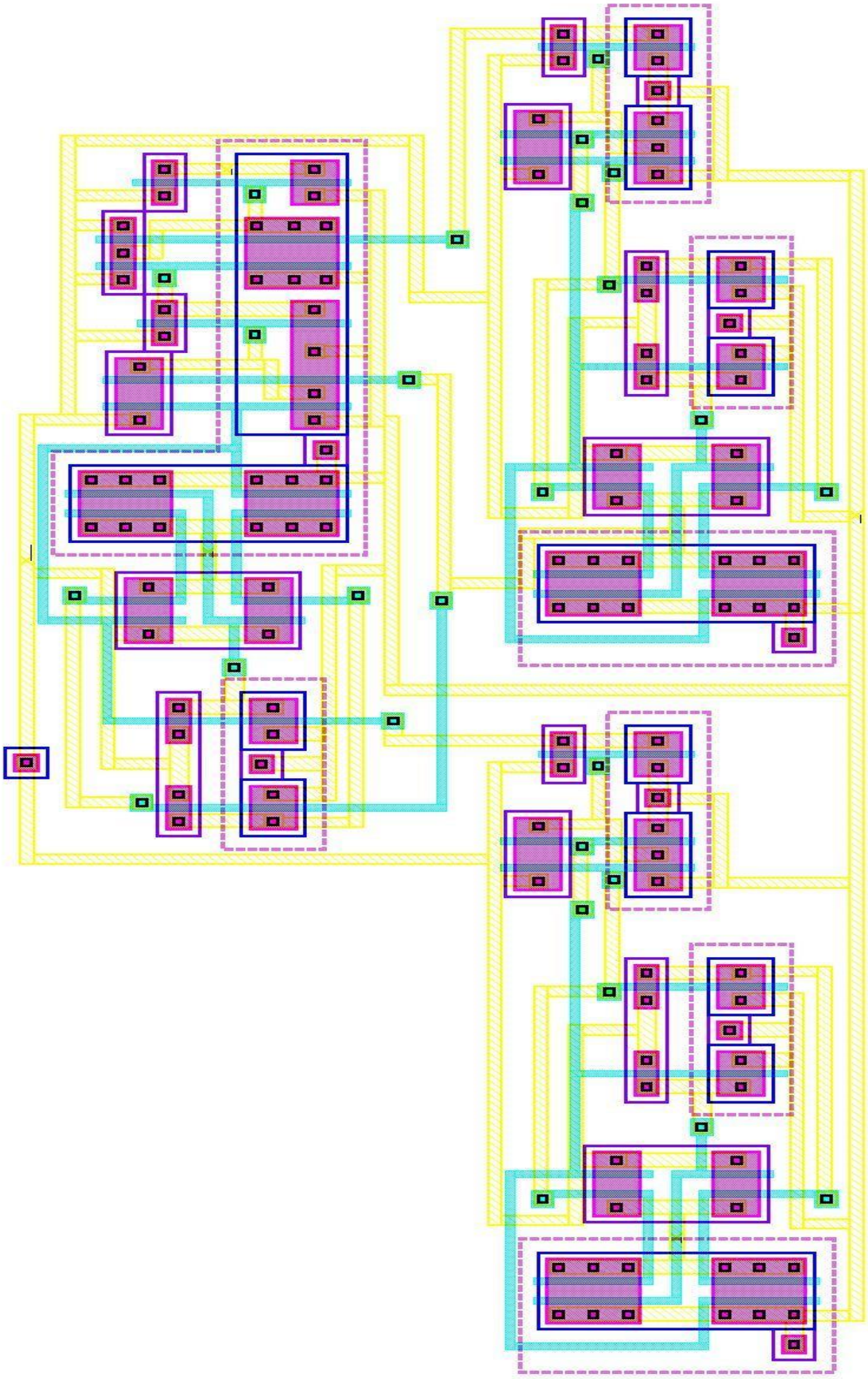


Figure 5. Circuit layout

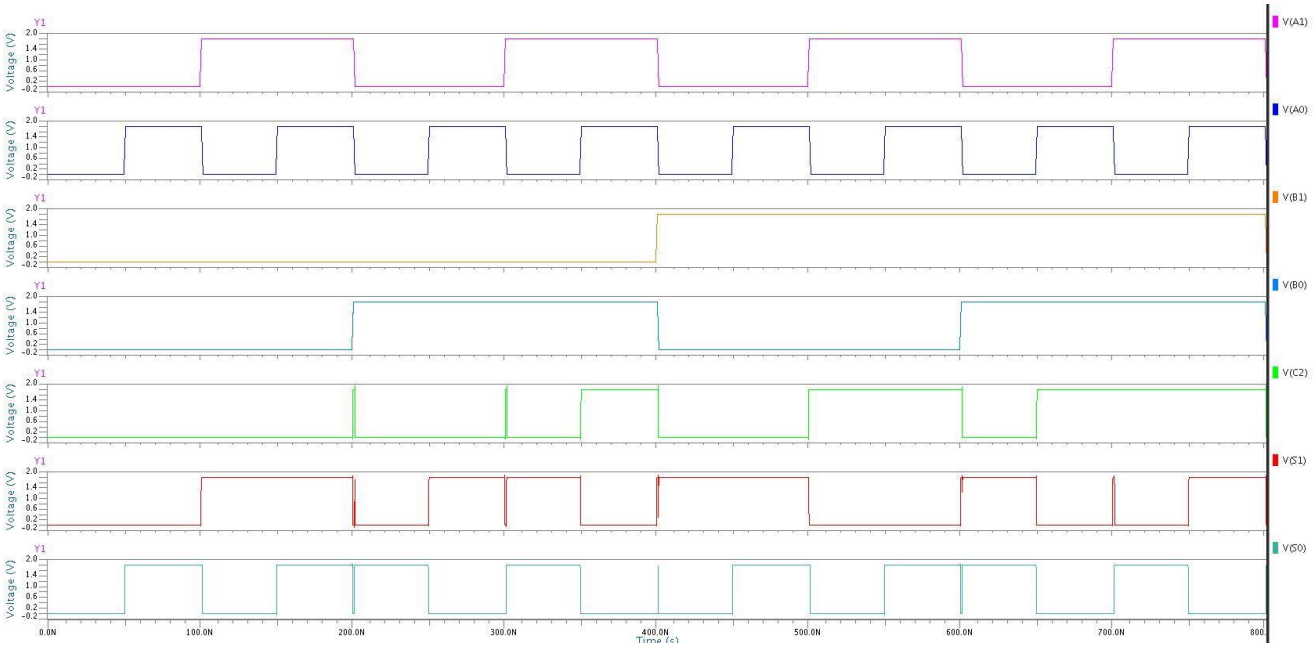


Figure 6. Simulation results for the schematic

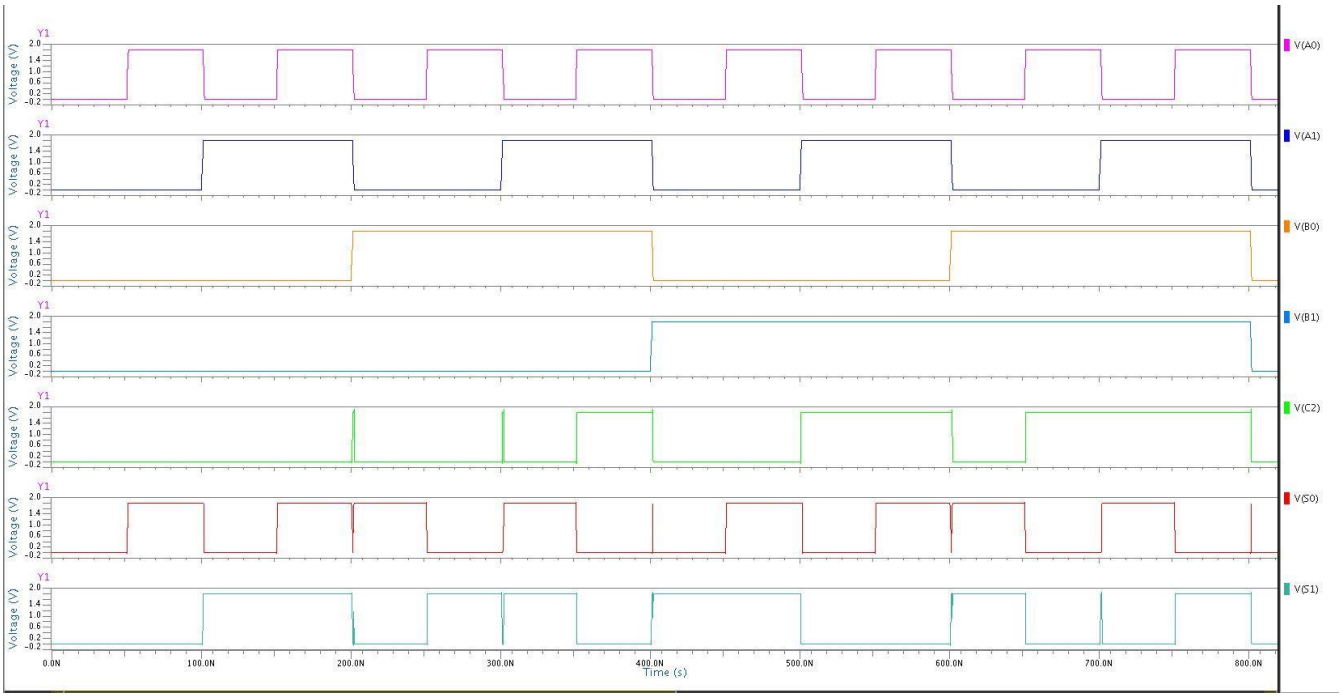


Figure 7. Post simulation layout results

RESULTS

I. Layout area = **616µm²**
II. Worst case propagation delay = **119.23ps**
III. Maximum operable frequency = **4.19GHz**

REFERENCES

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II. http://www.ijarcce.com/upload/2014/october/IJARCCE4M%20a%20sri%20-latha-Implementation%20of%20Ripple%20Carry%20and%20Carry%20Skip%20Adders%20with%20Speed%20and%20Area%20Efficient.pdf