FPGA Synthesis and Prototyping Lab: 7

Memories

Introduction

The purpose of this experiment is to Synthesis and Check the behavior of the Memories mentioned below.

Software tools Requirement

Xilinx Vivado

Synthesis the circuits given in Lab 27 on ARTY A7 FPGA Kit associated with your Login.

Results should have

Synthesis Report
RTL Schematic
Pin Mapping Report
Screenshot of the Remote Lab-Showing outputs (if any)

Note: You can use Virtual Input /Output to give inputs and View outputs or you may use Chipscope (ILA) for viewing the outputs.

Use: 100 MHz System Clock of the Board as reference clock

Design of memories

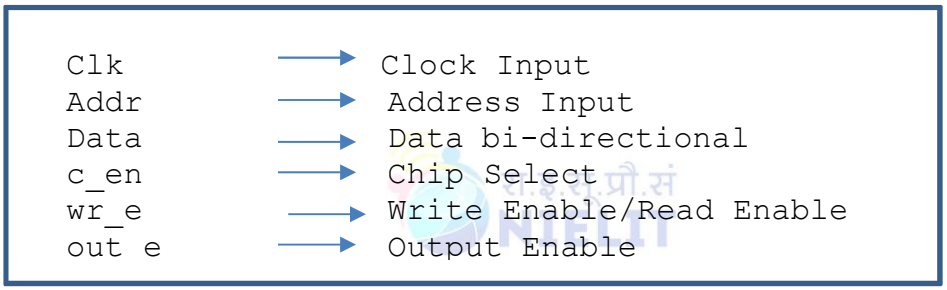
Introduction

The purpose of this experiment is to design a single Port 8 bit RAM Synchronous Read/Write.

Software tools Requirement

Modelsim (Siemens)

Xilinx Vivado



Design the above Circuit in Verilog HDL and write its test bench and capture theWaveforms,

Use Behavior modeling (use parameter to make it generic)