FPGA Synthesis and Prototyping Lab: 1

Basic Gates

Introduction

The purpose of this experiment is to Synthesis and Check the behavior of several of the basic logic gates mentioned below.

Software tools Requirement

Xilinx Vivado

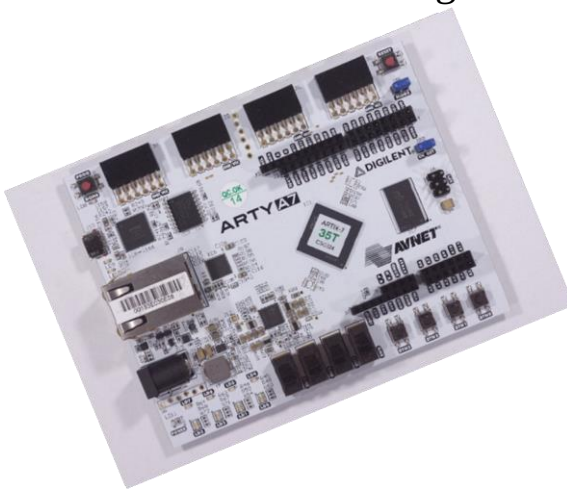
Synthesis the Basic Gates given below on ARTY A7 FPGA Kit associated with your Login.

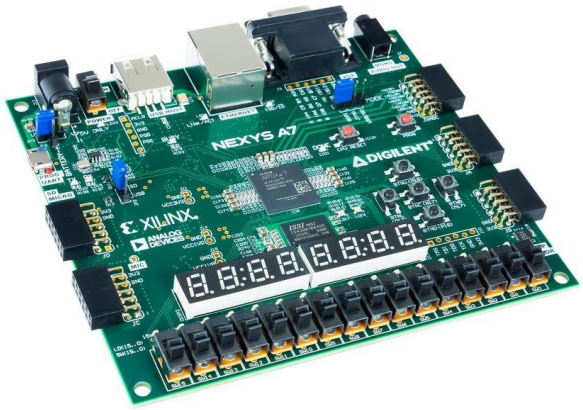
Results should have

- Synthesis Report
- RTL Schematic
- Pin Mapping Report
- Screenshot of the Remote Lab-Showing outputs (if any)

Note: Details of the Kit –ARTY A7is available in our Learning Management Portal (LMS)

You can login to our LMS with Login ID and Password Provided





Logic gates

Introduction

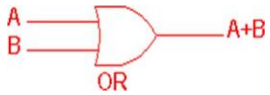
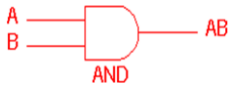
The purpose of this experiment is to connect several logic gates together to create a simple digital model.

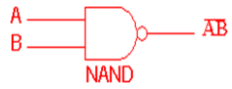
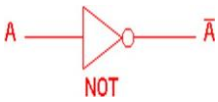
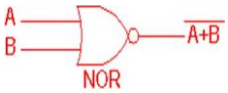
Software tools Requirement

Modelsim (Siemens)

Xilinx Vivado

Logic Gates and their Properties

Gate	Description	Truth Table			Logic Symbol
OR	The output is active high if any one of the input is in active high state, Mathematically, Q = A+B	A 0 0 1 1	B 0 1 0 1	Output Q 0 1 1	
	The output is active	A	B	Output	
AND	high only if both the inputs are in active high state, Mathematically,	0 0 1	0 1 0	Q 0 0	
	Q = A.B	1	1	0	

NAND	The output is active high only if any one of the input is in active low state, Mathematically, Q = (A.B)’	A 0 0 1 1	B 0 1 0 1	Output Q 1 1 1 0	
XOR	The output is active high only if any one of the input is in active high state, Mathematically, Q = A.B’ + B.A’	A 0 0 1 1	B 0 1 0 1	Output Q 0 1 1 0	
NOT	In this gate the output is opposite to the input state, Mathematically, Q = A^1	A 0 1		Output Q 1 0	
NOR	The output is active high only if both the inputs are in active low state, Mathematically, Q = (A+B)’	A 0 0 1 1	B 0 1 0 1	Output Q 1 0 0	

Describe the basic logic gates in Verilog HDL and capture the Waveforms

Questions to answered after this lab

1. *What is meant by ports?*
2. *Write the different types of port modes.*
3. *What are different types of operators?*
4. *What is difference b/w <= and: = operators?*
5. *What is meant by simulation?*