NATIONAL INSTITUTE OF ELECTRONICS AND INFORMATION

TECHNOLOGY, CALICUT

Lab Workshop Manual

Lab Workshop on FPGA Architecture and Programming using Verilog HDL

Contact Point for the Lab

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FPGA Synthesis and Prototyping Lab: 35

Binary Adders/Subtractors

Introduction

The purpose of this experiment is to Synthesis and Check the behavior of several of the basic adder/subtractor circuits mentioned in Lab 2,3.

Software tools Requirement

Xilinx Vivado

Synthesis the circuits given in Lab-2,3 on ARTY A7 FPGA or NEXYS A7 FPGA Kit associated with your Login.

Results should have

Synthesis Report
RTL Schematic
Pin Mapping Report
Screenshot of the Remote Lab-Showing outputs (if any)