FPGA Synthesis and Prototyping Lab: 3

Encoders/Decoders

Introduction

The purpose of this experiment is to Synthesis and Check the behavior of Encoders/Decoders circuits mentioned below.

Software tools Requirement

Xilinx Vivado

Synthesis the circuits given below on ARTY A7 FPGA or NEXYSA7 FPGA Kit associated with your Login.

Results should have

- Synthesis Report
- RTL Schematic
- Pin Mapping Report
- Screenshot of the Remote Lab-Showing outputs (if any)

Note: You can use Virtual Input /Output to give inputs and View outputs or you may use Chipscope (ILA) for viewing the outputs.

Refer to demo Videos in LMS for usage of ILA

Encoders

Introduction

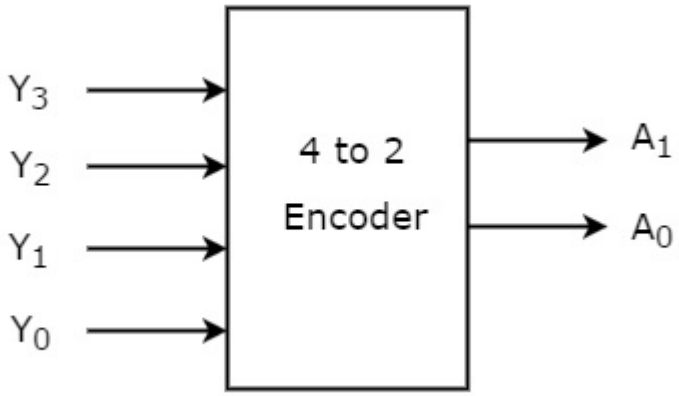
The purpose of this experiment is to introduce the design of simple combinational circuits, in this case Encoders. An Encoder is a combinational circuit that performs the reverse operation of Decoder. It has maximum of 2n input lines and ‘n’ output lines. It will produce a binary code equivalent to the input, which is active High. Therefore, the encoder encodes 2n input lines with ‘n’ bits. It is optional to represent the enable signal in encoders.

Software tools Requirement

Modelsim (Siemens)

Xilinx Vivado

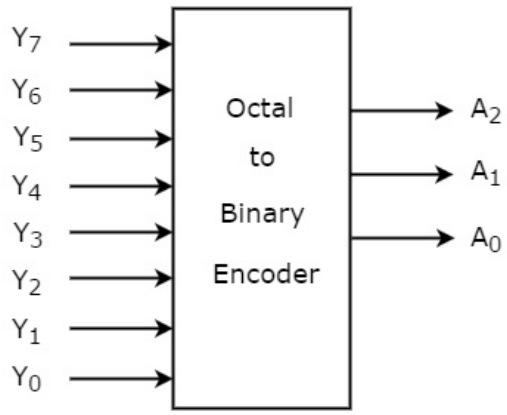
Logic Diagram



4 to 2 Encoder

Inputs				Outputs	
Y_3	Y_2	Y_1	Y_0	A_1	A_0
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1

Truth Table



Octal to Binary Encoder

Describe the above circuits in Verilog HDL and capture the Waveforms

1. ***Dataflow modeling***
2. ***Behavior modeling***
3. ***Structural modeling***

Questions to answered after this lab

1. *Implement full adder by using suitable decoder.*
2. *Write short notes on "test bench" with examples.*

Priority Encoders

Introduction

The purpose of this experiment is to introduce the design of simple combinational circuits, in this case Priority Encoder. A 4 to 2 priority encoder has four inputs Y3, Y2, Y1 & Y0 and two outputs A1 & A0. Here, the input, Y3 has the highest priority, whereas the input, Y0 has the lowest priority. In this case, even if more than one input is '1' at the same time, the output will be the binary code corresponding to the input, which is having higher priority. We considered one more output, V in order to know, whether the code available at outputs is valid or not. If at least one input of the encoder is '1', then the code available at outputs is a valid one. In this case, the output, V will be equal to 1.

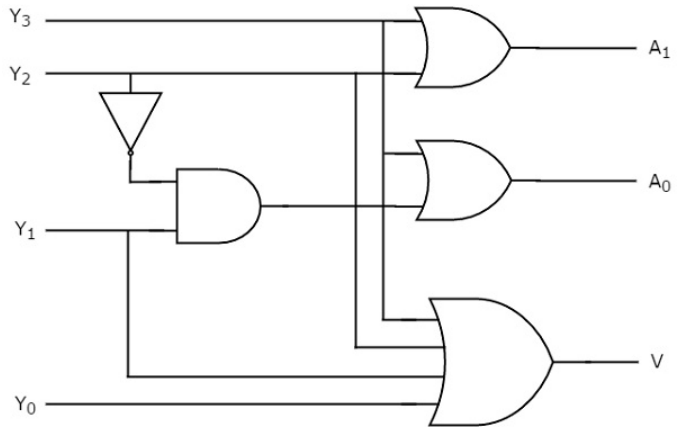
If all the inputs of encoder are '0', then the code available at outputs is not a valid one. In this case, the output, V will be equal to 0.

Software tools Requirement

Modelsim (Siemens)

Xilinx Vivado

Logic Diagram



4 to 2 Priority Encoder

Inputs				Outputs		
Y_3	Y_2	Y_1	Y_0	A_1	A_0	V
0	0	0	0	0	0	0
0	0	0	1	0	0	1
0	0	1	x	0	1	1
0	1	x	x	1	0	1
1	x	x	x	1	1	1

Truth Table

Describe the above in Verilog HDL and capture the Waveforms

1. ***Dataflow modeling***
2. ***Behavior modeling***
3. ***Structural modeling***

Questions to answered after this lab

1. Why is priority encoder preferred over conventional ones?

Decoders

Introduction

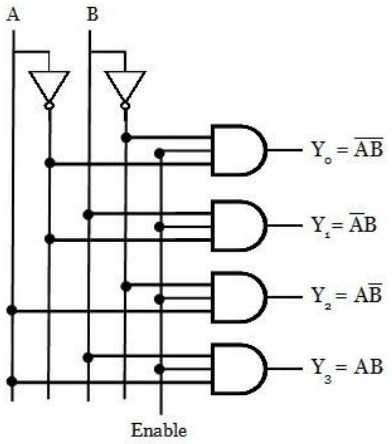
The purpose of this experiment is to introduce the design of simple combinational circuits, in this case Decoders. A decoder is a multiple-input, multiple-output combinational logic circuit. It converts the n bit data inputs into the coded 2n outputs. It decodes the information hidden by the encoder.

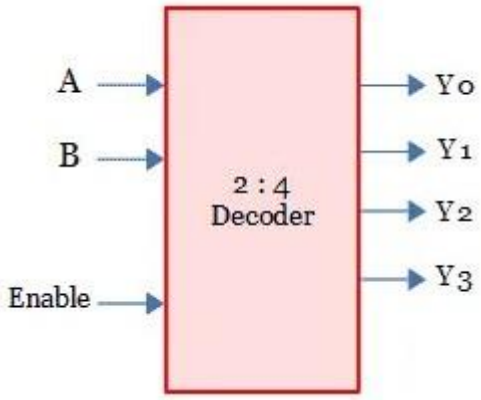
Software tools Requirement

Modelsim (Siemens)

Xilinx Vivado

Logic Diagram





2:4 Decoder

Inputs			Outputs			
EN	A	B	Y3	Y2	Y1	Yo
0	x	x	0	0	0	0
1	0	0	0	0	0	1
1	0	1	0	0	1	0
1	1	0	0	1	0	0
1	1	1	1	0	0	0

Truth Table

Describe the above in Verilog HDL and capture the Waveforms

1. **Dataflow modeling**
2. **Behavior modeling**
3. **Structural modeling (Design a 4 to 16 decoder by using two 3 to 8 decoders)**
4. **Design a 4 to 16 decoder using case statements in Verilog**