FPGA Synthesis and Prototyping Lab: 6

Counters

Introduction

The purpose of this experiment is to Synthesis and Check the behavior of the Johnson Counters mentioned below.

Software tools Requirement

Xilinx Vivado

Synthesis the circuits given below on ARTY A7 FPGA Kit associated with your Login.

Results should have

- Synthesis Report
- RTL Schematic
- Pin Mapping Report
- Screenshot of the Remote Lab-Showing outputs (if any)

Note: You can use Virtual Input /Output to give inputs and View outputs or you may use Chipscope (ILA) for viewing the outputs.

Design of Counters

Introduction

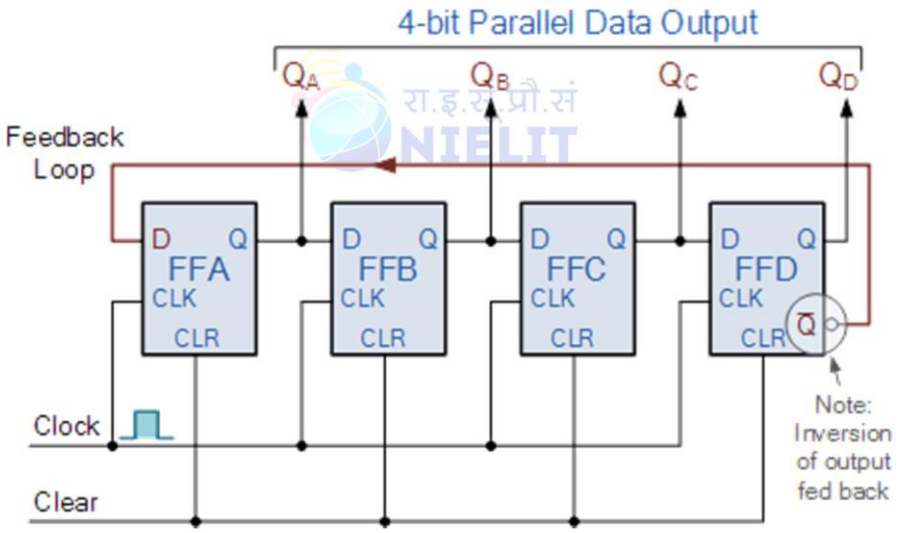
The purpose of this experiment is to introduce the design of Johnson Counter.

In Johnson counter, the complemented output of last flip flop is connected to input of first flip flop and to implement n-bit Johnson counter we require n flip-flop

Software tools Requirement

Modelsim (Siemens)

Xilinx Vivado



4 bit Johnson Counter

Design the above behavior in Verilog HDL and write its test bench and capture theWaveforms,

Use Behavior modeling or Structural Modeling