FPGA Synthesis and Prototyping Lab: 5

Counters

Introduction

The purpose of this experiment is to Synthesis and Check the behavior of the Counters mentioned in below.

Software tools Requirement

Xilinx Vivado

Synthesis the circuits given belowon ARTY A7 FPGA Kit associated with your Login.

Results should have

- Synthesis Report
- RTL Schematic
- Pin Mapping Report
- Screenshot of the Remote Lab-Showing outputs (if any)

Note: You can use Virtual Input /Output to give inputs and View outputs or you may use Chipscope (ILA) for viewing the outputs.

Design of Counters

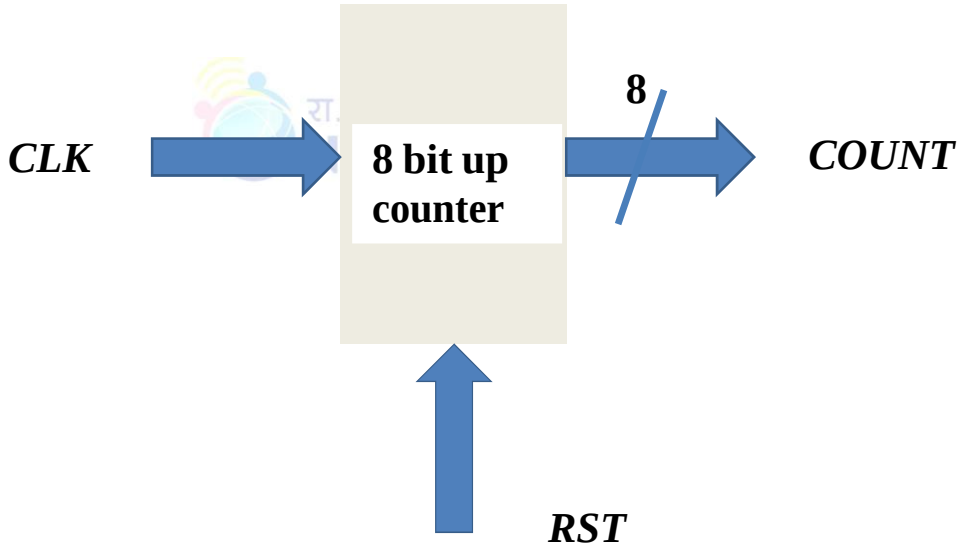
Introduction

The purpose of this experiment is to introduce the design of Synchronous sequential circuits, in this case we are taking an 8 bit up counter.

Software tools Requirement

Modelsim (Siemens)

Xilinx Vivado



Synchronous 8 bit up Counter

Design the above behavior in Verilog HDL and write its test bench and capture theWaveforms

Behavior modeling

Design of Counters

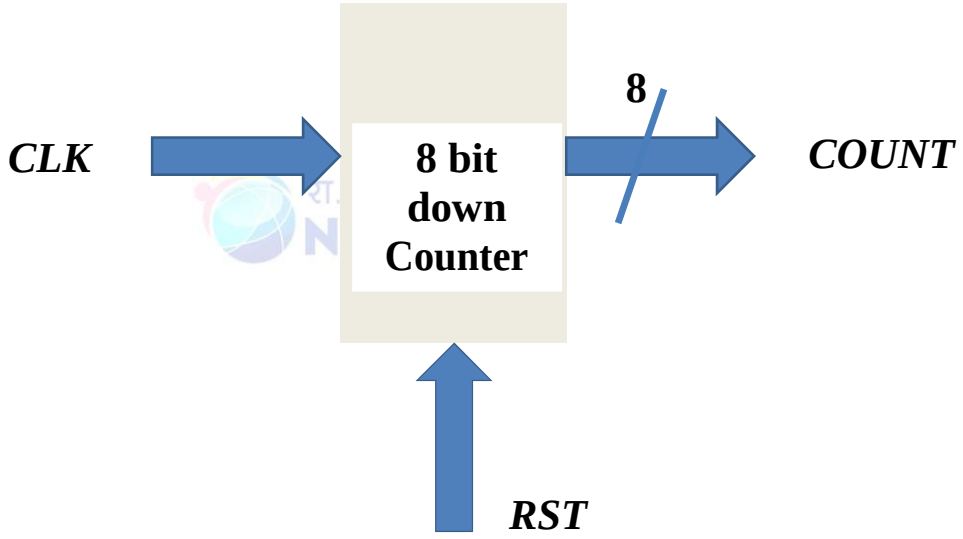
Introduction

The purpose of this experiment is to introduce the design of Synchronous sequential circuits, in this case we are taking an 8 bit down counter.

Software tools Requirement

Modelsim (Siemens)

Xilinx Vivado



Synchronous 8 bit down Counter

Design the above behavior in Verilog HDL and write its test bench and capture theWaveforms

Behavior modeling

Design of Counters

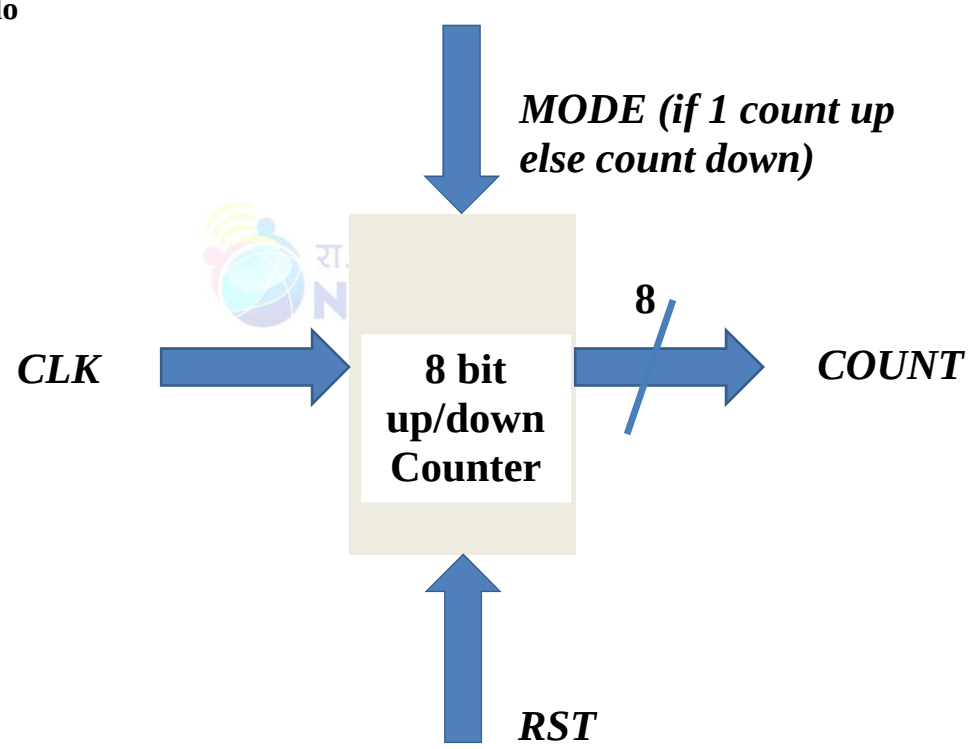
Introduction

The purpose of this experiment is to introduce the design of Synchronous sequential circuits, in this case we are taking an 8 bit up/down counter.

Software tools Requirement

Modelsim (Siemens)

Xilinx Vivado



Synchronous 8 bit up/down Counter

Design the above behavior in Verilog HDL and write its testbench and capture the Waveforms

Behavior modeling

Design of Counters

Introduction

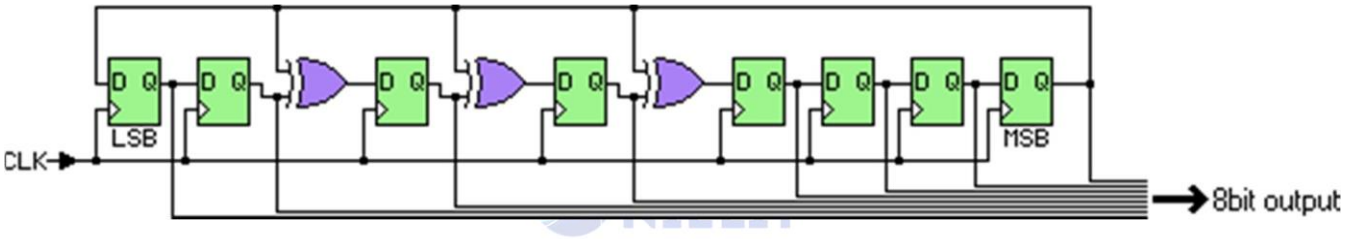
The purpose of this experiment is to introduce the design of LFSR Counters.

An LFSR is a shift-register with some XOR gates

Software tools Requirement

Modelsim (Siemens)

Xilinx Vivado



LFSR Counter

Design the above behavior in Verilog HDL and write its testbench and capture the Waveforms (Assume all D Flip flop has initial value '1')

Use Behavior modeling or Structural Modeling