FPGA Synthesis and Prototyping Lab: 4

Multiplexers/De Multiplexers

Introduction

The purpose of this experiment is to Synthesis and Check the behavior of the Multiplexers/De Multiplexers circuits mentioned below.

Software tools Requirement

Xilinx Vivado

Synthesis the circuits given below on ARTY A7 FPGA Kit associated with your Login.

Results should have

- Synthesis Report
- RTL Schematic
- Pin Mapping Report
- Screenshot of the Remote Lab-Showing outputs (if any)

Note: You can use Xilinx Vivado IP Core and Virtual Input /Output to give inputs and View outputs or you may use Chipscope (ILA) for viewing the outputs.

Refer to demo Videos in LMS for usage of IP Core, VIO, and Chipscope (ILA)

Multiplexers

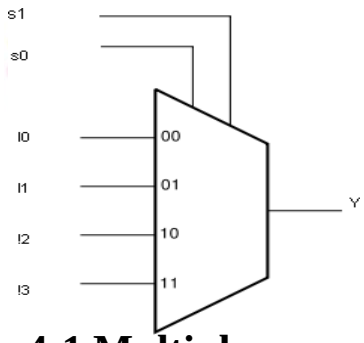
Introduction

The purpose of this experiment is to introduce the design of simple combinational circuits, in this case, multiplexers. A multiplexer is a digital circuit, which is used to select a single input from the multiple input lines.

Software tools Requirement

Modelsim (Siemens)
Xilinx Vivado

Logic Diagram



4:1 Multiplexer

s1	s0	Y
0	0	I0
0	1	I1
1	0	I2
1	1	I3

Truth Table

➡ Implement the boolean expression F(A, B, C) = ∑ m(2, 3, 6, 7) using a

multiplexer.

➡ Implement the boolean expression F(A, B, C) = ∑ m(0, 1, 3, 5, 7) using a multiplexer.

Describe the above in Verilog HDL and capture the Waveforms

1. ***Dataflow modeling***
2. ***Behavior modeling***
3. ***Structural modeling (Use the gates for designing the Mux)***
4. ***Design the above two problems using structural modeling – use Muxes as components***

Demultiplexers

Introduction

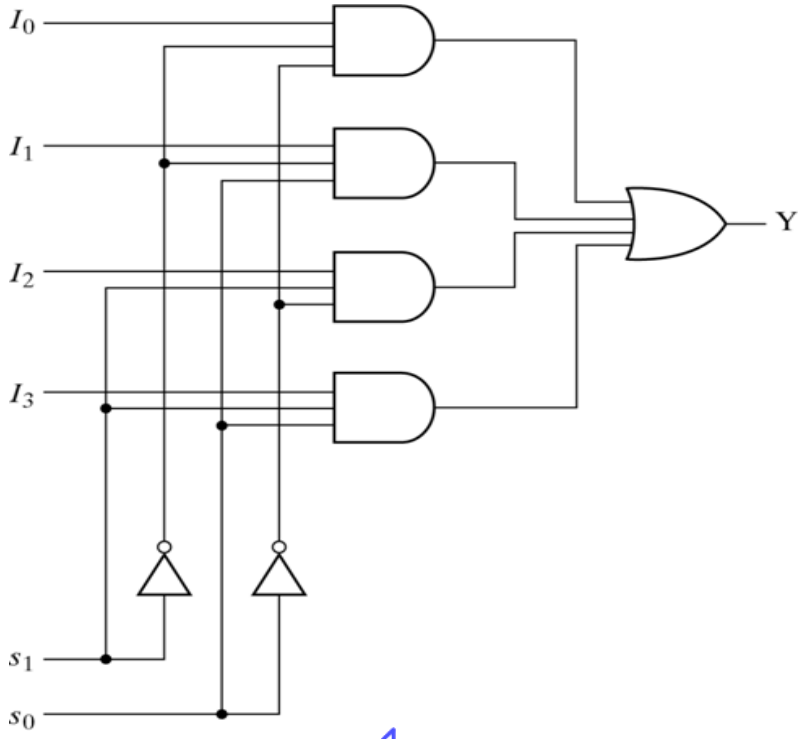
The purpose of this experiment is to introduce the design of simple combinational circuits, in this case Demultiplexer. Demultiplexer or Demux is a combinational circuit that distributes the single input data to a specific output line. The control inputs or selection lines are used to select a specific output line from the possible output lines.

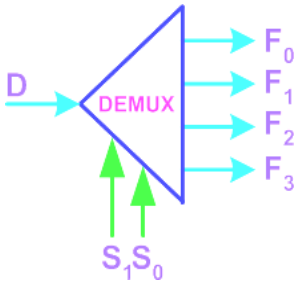
Software tools Requirement

Modelsim (Siemens)

Xilinx Vivado

Logic Diagram





1:4 Demultiplexer

S1	S0	F0	F1	F2	F3
0	0	D	0	0	0
0	1	0	D	0	0
1	0	0	0	D	0
1	1	0	0	0	D

Truth Table

Describe the above in Verilog HDL and capture the Waveforms

1. ***Dataflow modeling***
2. ***Behavior modeling***
3. ***Structural modeling (Use the gates for designing the Mux)***
4. ***Design a 1:8 Demux using two 1:4 Demux(Structural Modeling)***