Jithendra Kantharaju

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Research Interests

Aspiring to pursue a PhD in Computer Engineering with a concentration in **CMOS VLSI Design** and **Hardware Verification**. My research focus lies in developing high-performance **ASIC architectures** and optimizing **VLSI Testing** methodologies. I am particularly interested in leveraging automation and scripting to enhance **Electronic Design Automation (EDA)** workflows and exploring the intersection of **Hardware Security** and scalable design verification for next-generation computing systems.

Education

University of South Florida, Tampa — **Jan 2025 – Present**

Master of Science in Computer Engineering — *Tampa, FL*

- **Current Focus:** Computer Architecture, VLSI Systems.

Siddaganga Institute of Technology — **2020 – 2023**

Bachelor of Engineering in Electronics & Communication Engineering — *Tumakuru, India*

- **Relevant Coursework:** CMOS VLSI Design, ASIC Design, VLSI Testing & Verification, Analog & Mixed Mode VLSI Design, Digital System Design, Embedded Systems, Rapid Prototyping & MEMS, DSP, Machine Learning, ARM Controller, Microcontrollers, Industrial Automation, PCB Design.

Technical Skills

VLSI & Hardware Design: Verilog, VHDL, System Verilog, CMOS Layout, Digital Logic Design, FPGA, ASIC Design
Embedded Systems: ARM Controllers (Cortex), Microcontrollers (8051), PCB Design, IoT Network Technology
EDA & Simulation: Cadence Virtuoso, Xilinx Vivado, ModelSim, LTSpice, MATLAB
Programming: C, C++ (OOPs), Python, Embedded C, Bash
Signal Processing: Digital Signal Processing (DSP), Control Systems, Machine Learning Algorithms
DevOps & Tools: CI/CD (Jenkins, GitHub Actions), Terraform, AWS, Kubernetes, Git/Version Control, Automated Testing Frameworks

Academic Projects

ASIC Design of 8x8 Array Multiplier | *Cadence Virtuoso, 0.5μm Technology*

- Designed a layout of a 8x8 array multiplier to calculate the product of two 16-bit numbers using **0.5μm technology** within a 960μm x 960μm pad frame area using **Cadence Virtuoso**.
- Optimized layout compactness while strictly adhering to design rules; implemented Design Rule Checks (**DRC**), Layout vs. Schematic (**LVS**), and Parasitic Extraction (**PEX**) to validate circuit functionality.

Design Of Integrated Low-cost Electrospinning Device For Nanofibers

- Designed and prototyped a cost-effective electrospinning apparatus for fabricating nanofibers, focusing on **high-voltage power supply regulation** and **collector drum control**.
- Utilized knowledge of **Smart Materials** and **Rapid Prototyping** from undergraduate coursework to engineer the control mechanism.

Detecting Voice Clones in Voice Assistants | *Python, Scikit-learn, Librosa*

- Built an **ML pipeline** using **Python** to extract **MFCC features** and detect **AI-cloned voices**, achieving **96% accuracy** with an **SVM classifier**.
- **Relevance:** Demonstrates strong Python scripting and signal processing skills applicable to **UVM/Verification testbenches**.

Professional Experience

Associate DevOps Engineer — **Aug 2023 – Dec 2024**

Corezeal Technologies — *Bengaluru, India*

- Built a **GitOps CI/CD pipeline** using **GitHub Actions** to automate **Terraform** infrastructure provisioning and secure **AWS EKS** deployments.
- Integrated **Docker**, **Helm Charts**, and **SonarCloud** to enforce code quality standards and automate containerized releases via **Amazon ECR**.
- Implemented robust **Git branching strategies** and automated testing workflows to ensure auditable, zero-downtime cloud-native delivery.

Intern (IoT & Embedded Systems) — **Sep 2021 – Oct 2021**

Agimus Technologies Pvt Ltd. — *Bengaluru, India*

- Developed firmware for an **ESP32**-based **IoT** device for remote patient monitoring (Pulse, O_2, Temperature).
- Programmed **Wi-Fi** connectivity and sensor data logging, integrating real-time alerts via **Twilio APIs**.

Certifications

Microsoft Certified: Azure Fundamentals (AZ-900) (Verify Credential)
Oracle Cloud Infrastructure 2025 Certified DevOps Professional (Verify Credential)