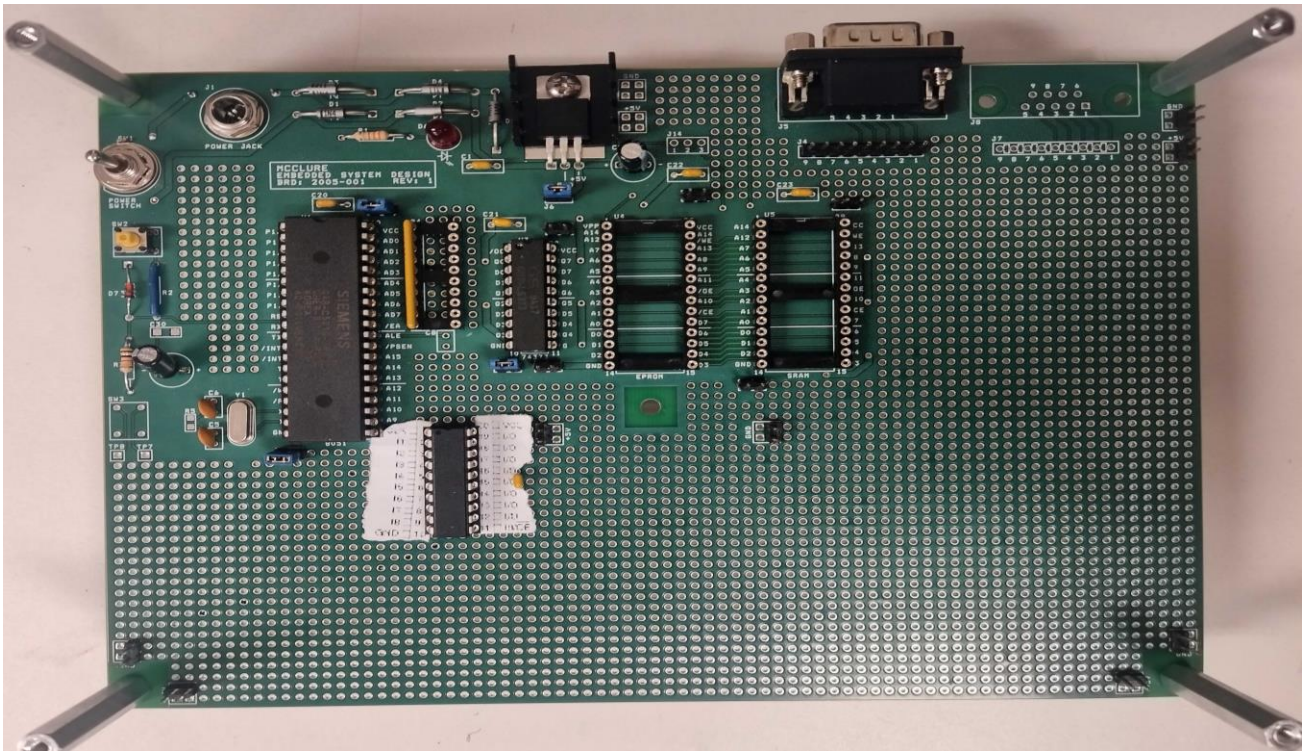
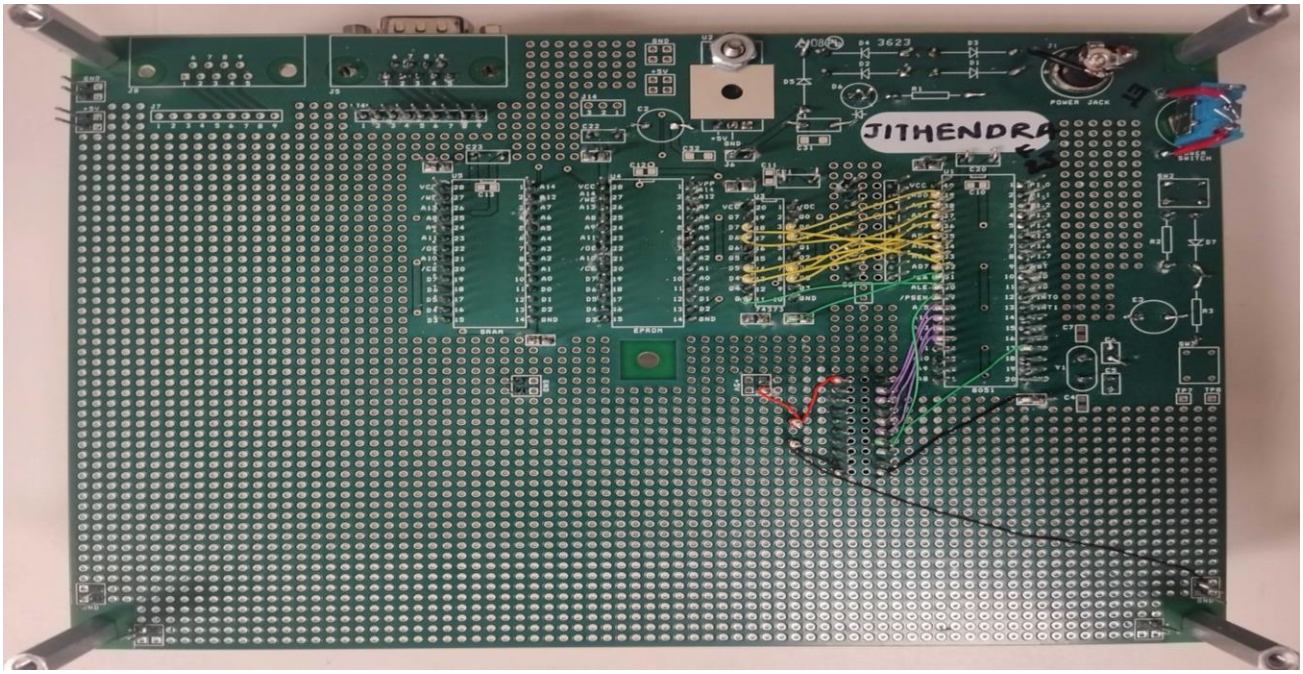
LAB 1 Submission

Board Top:

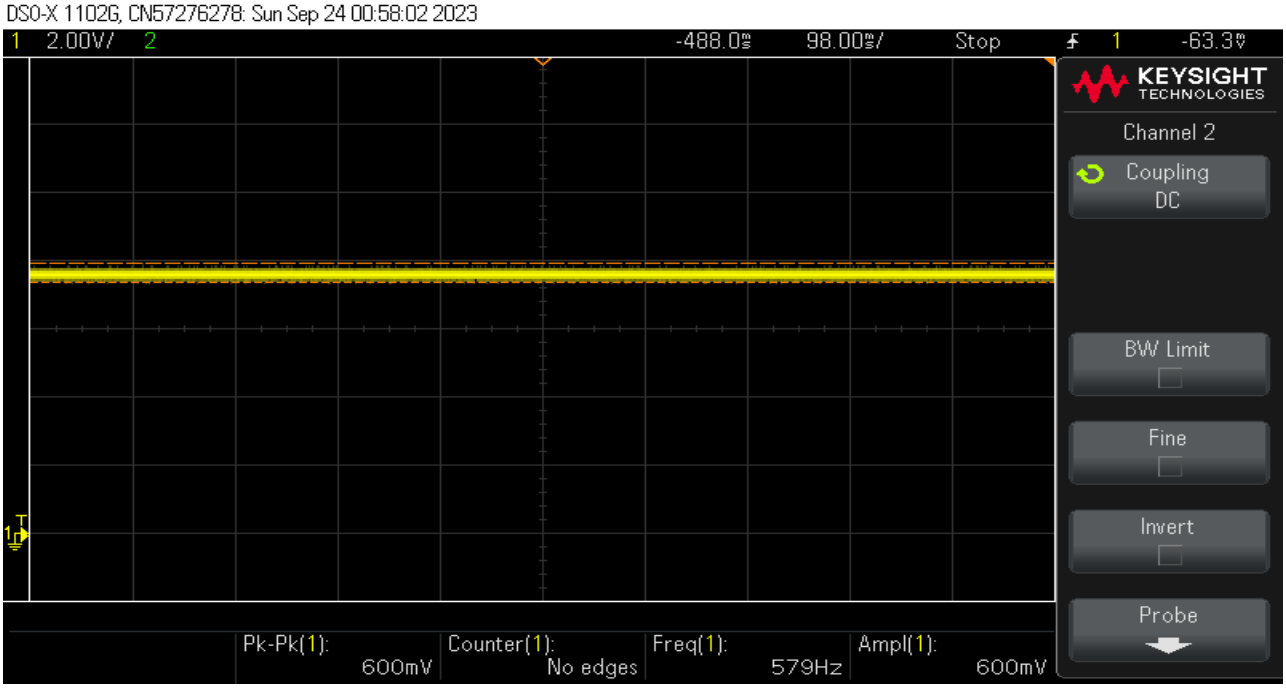


Board Bottom:

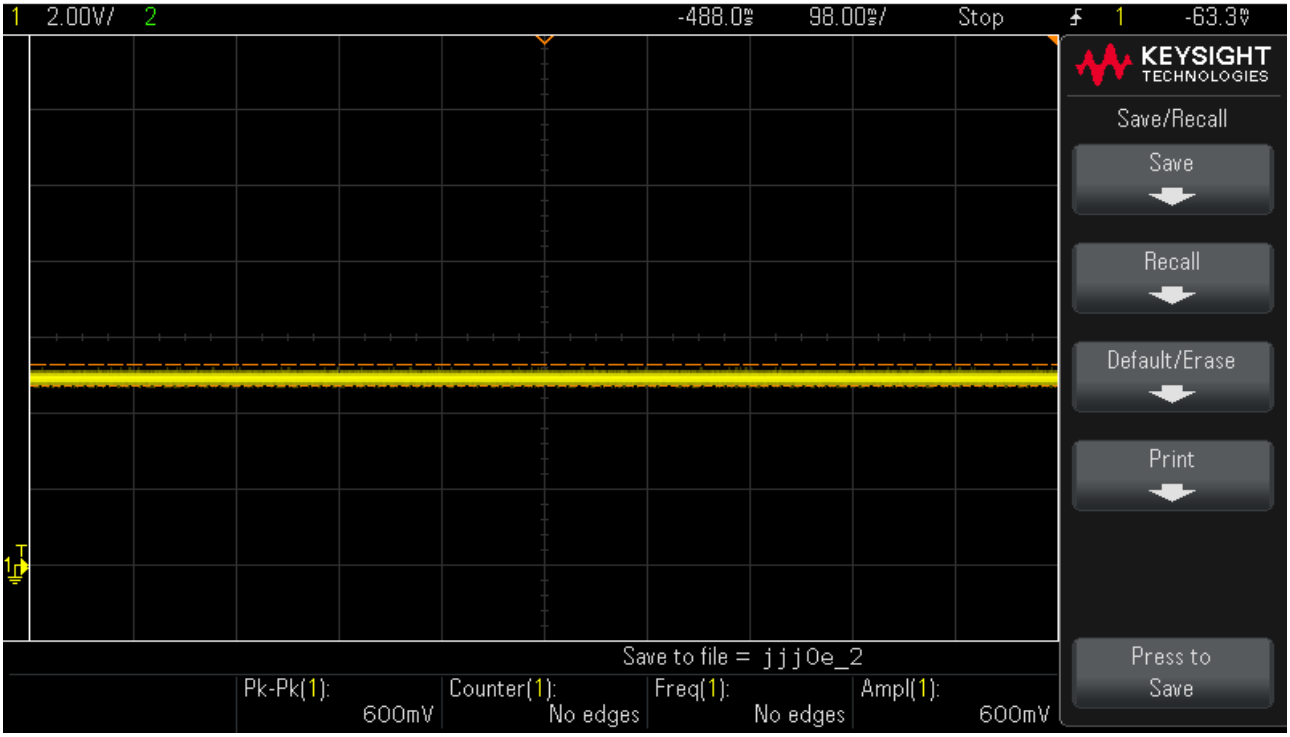


Voltage values at regulator input and output:

DSO-X 1102G, CN57276278: Sun Sep 24 00:58:02 2023

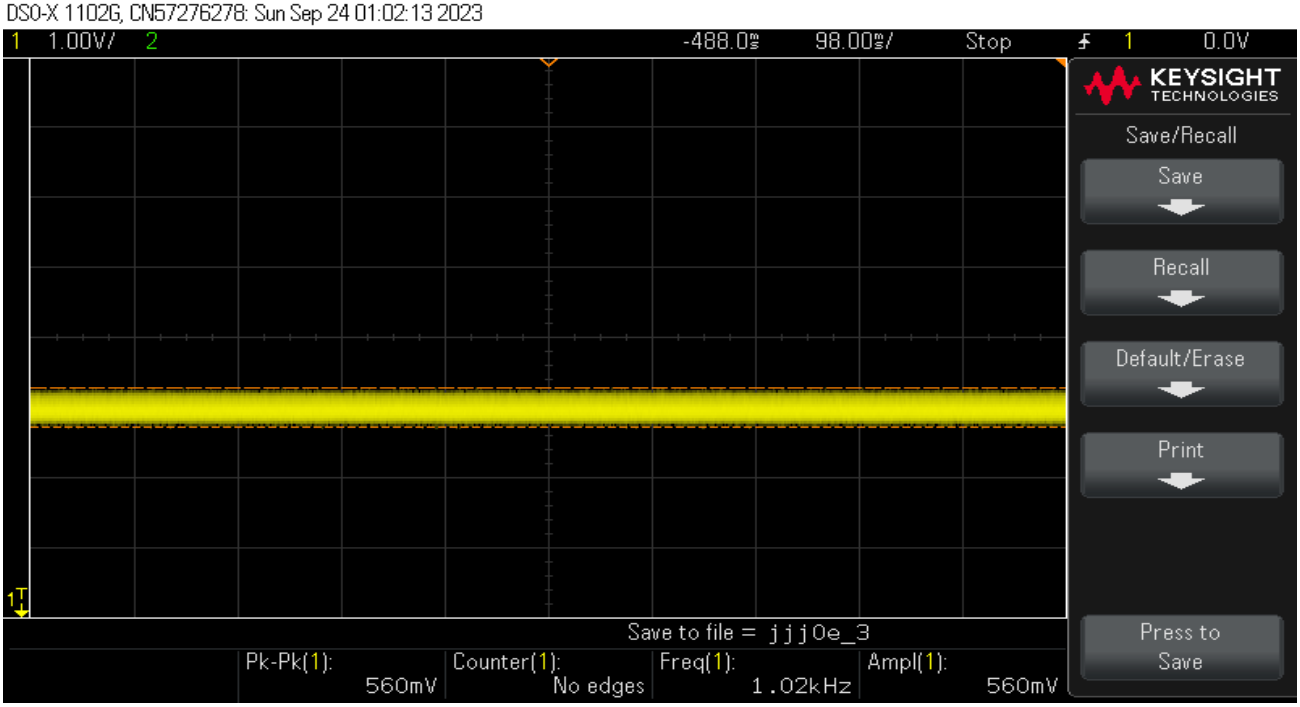


DSO-X 1102G, CN57276278: Sun Sep 24 01:00:30 2023

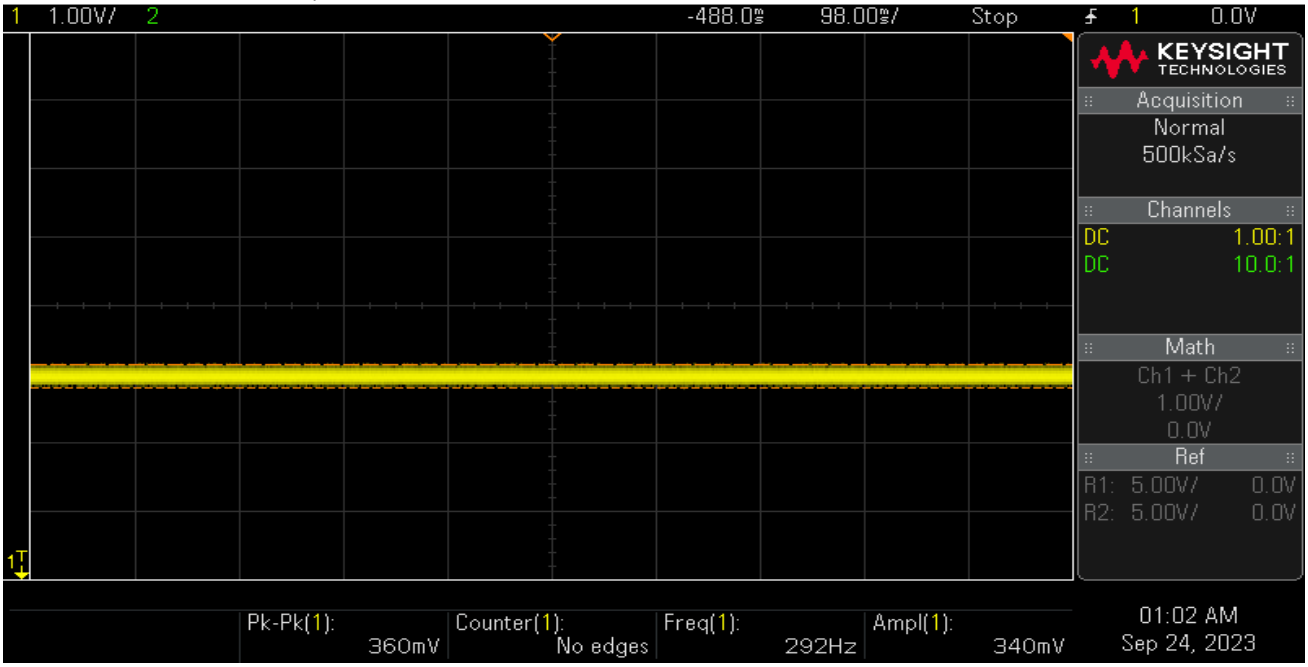


Voltage between VCC and GND at top and bottom of MCU:

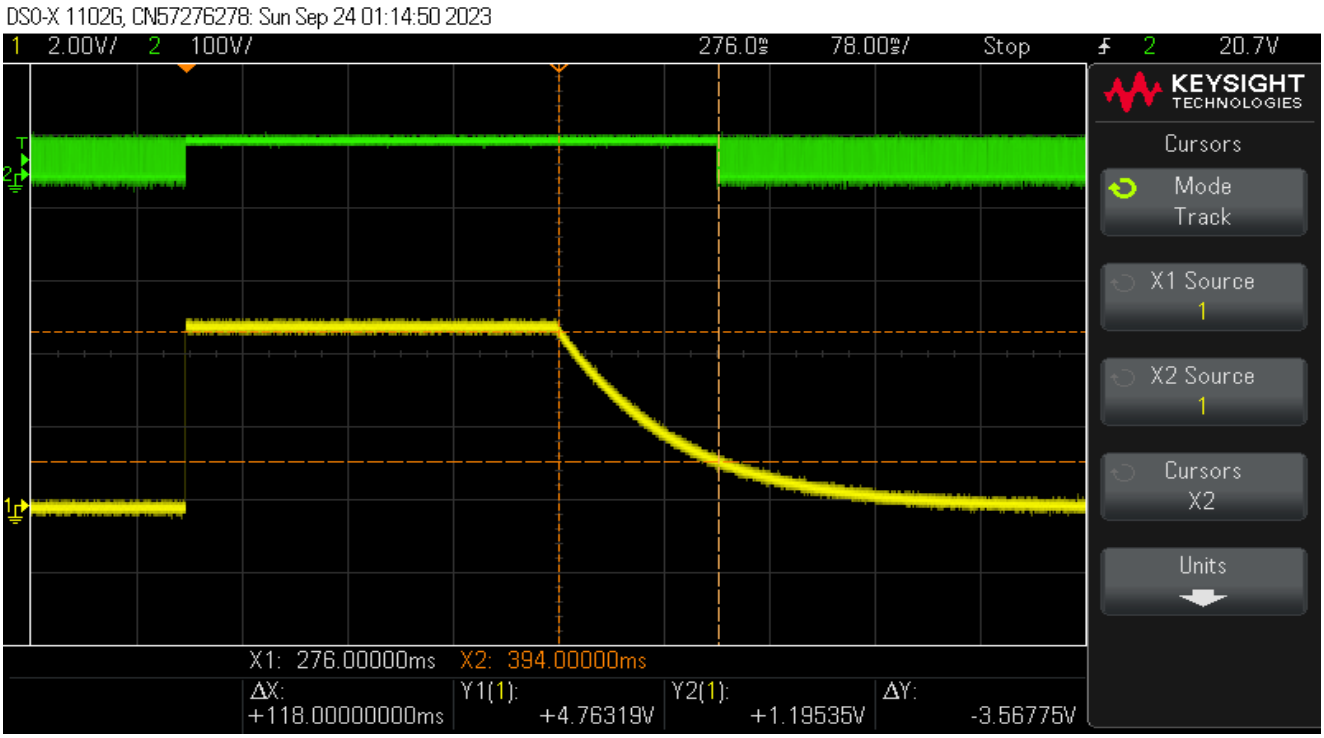
DSO-X 1102G, CN57276278: Sun Sep 24 01:02:13 2023



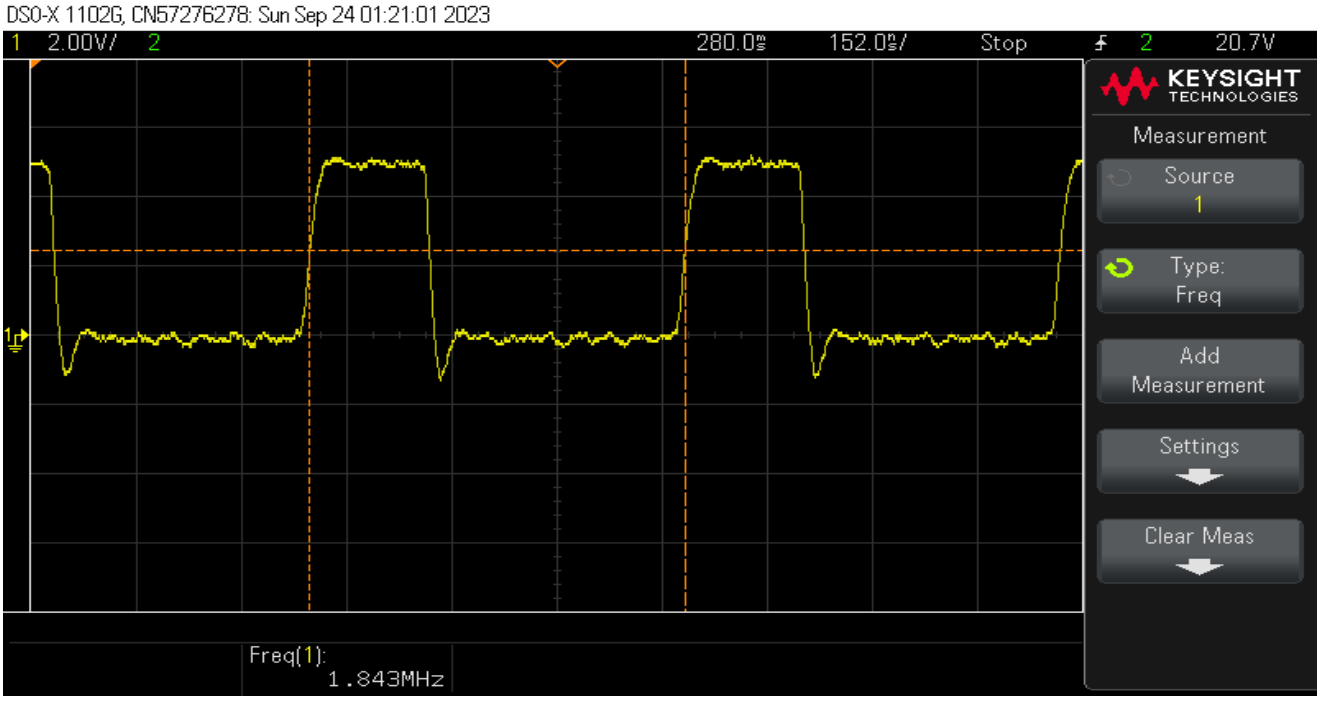
DSO-X 1102G, CN57276278: Sun Sep 24 01:03:36 2023



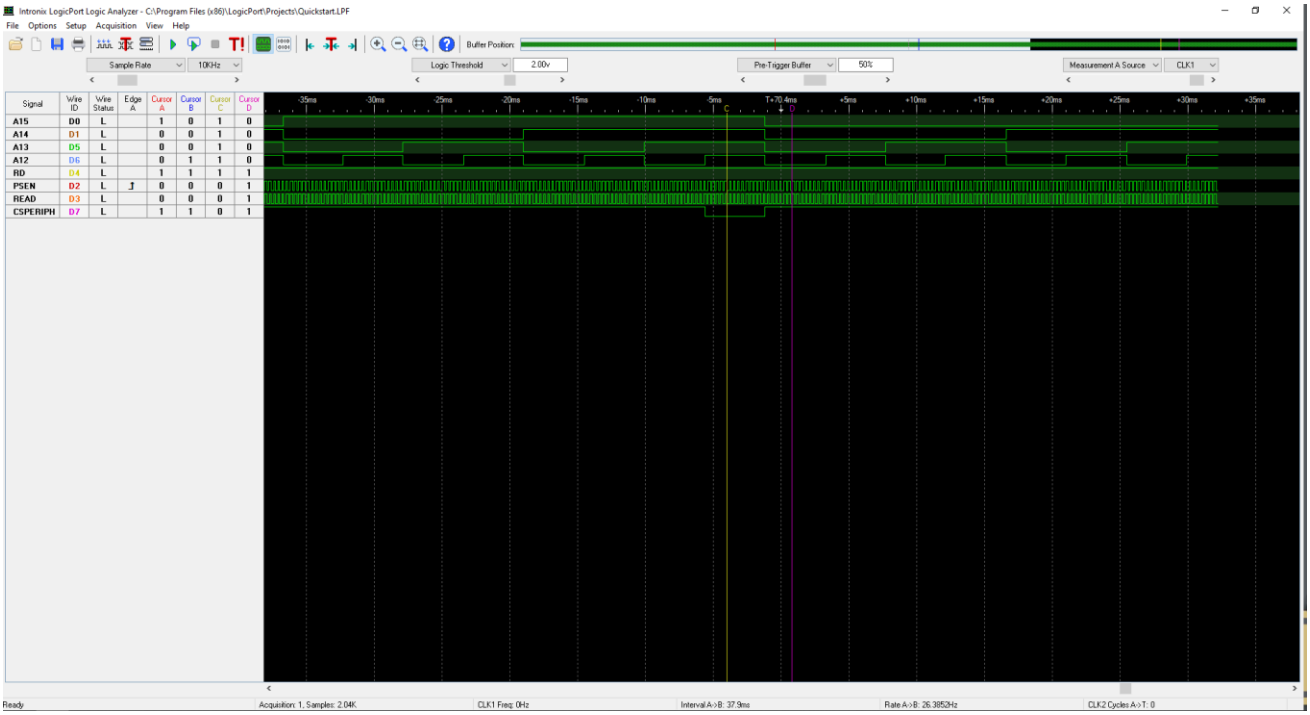
Voltage at Reset and ALE pin at the time of reset:



Clock frequency measured at ALE:



SPLD output measured at logic port application:


Intronix LogicPort Logic Analyzer - C:\Program Files (x86)\LogicPort\Projects\Quickstart.LPF
File Options Setup Acquisition View Help
Buffer Position
Sample Rate
10KHz
Logic Threshold
2.00v
Pre-Trigger Buffer
50%
Measurement A Source
CLK1
Signal
Wire ID
Wire Status
Edge A
Cursor A
Cursor B
Cursor C
Cursor D
A15 D0 L 1 0 1 0
A14 D1 L 0 0 1 0
A13 D5 L 0 0 1 0
A12 D6 L 0 1 1 0
RD D4 L 1 1 1 1
PSEN D2 L 0 0 0 1
READ D3 L 0 0 0 1
CSPERIPH D7 L 1 1 0 1
-35ms -30ms -25ms -20ms -15ms -10ms -5ms T+70.4ms +5ms +10ms +15ms +20ms +25ms +30ms +35ms
Ready
Acquisition: 1, Samples: 2.04K
CLK1 Freq: 0Hz
Interval A->B: 37.9ms
Rate A->B: 26.385Hz
CLK2 Cycles A->T: 0