PCB Report – LAB 15

Professor Version of Board 2

Objective:

The purpose of this lab is to test Professor version of board 2 which is designed with good practice and bad practice like adding decoupling capacitor and its placement, return plane and return path.

Board:

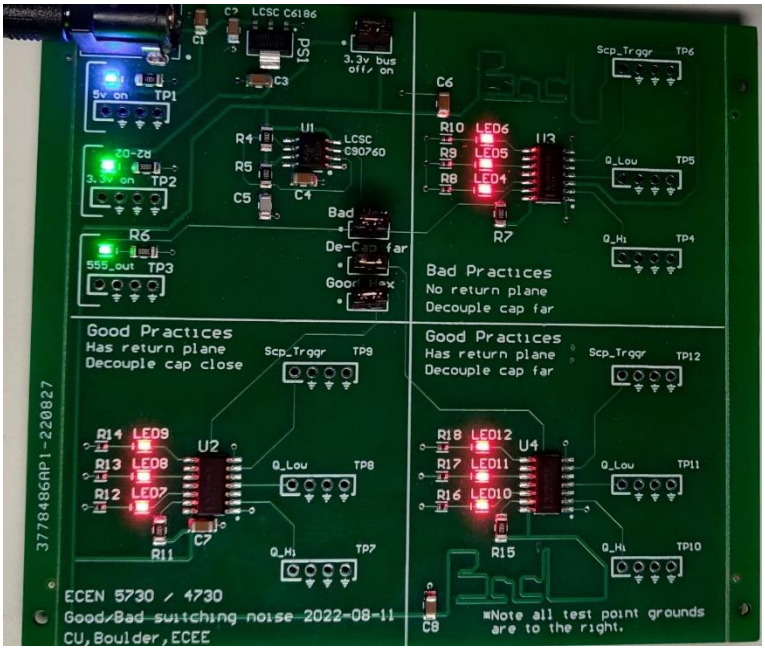


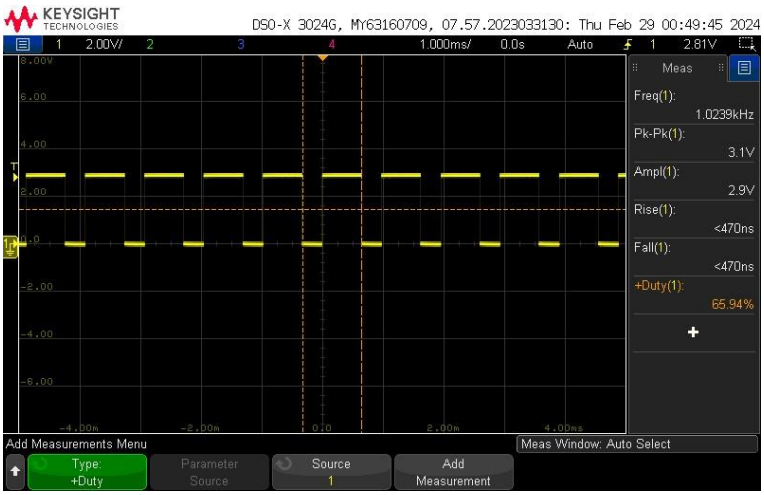
Figure 1.1 Professor version of board 2.

Scope Outputs:

1. Power supply:

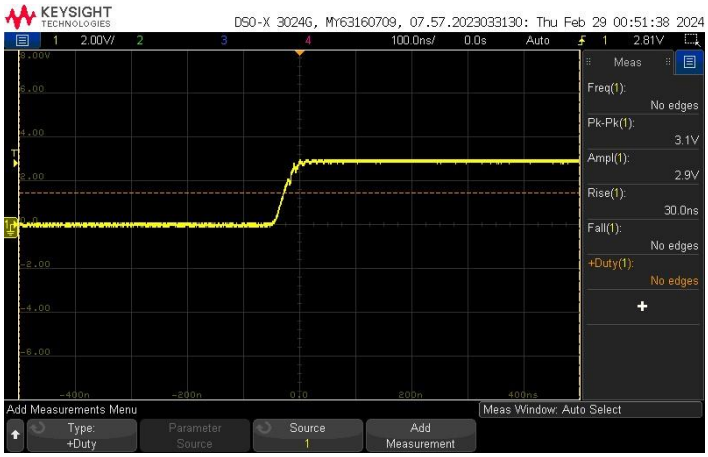
Captured and verified 5V coming from power jack and converted to 3.3V from LDO.

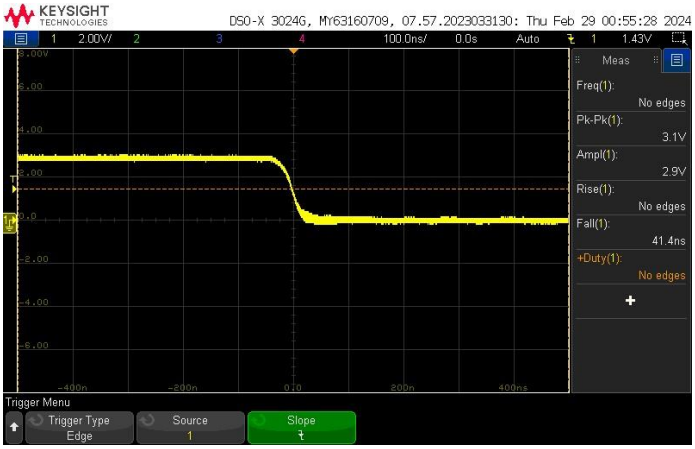
2. LMC 555 timer output:



Noted the figure of metrics such as frequency nearly 1KHz and positive duty cycle of nearly 66%.

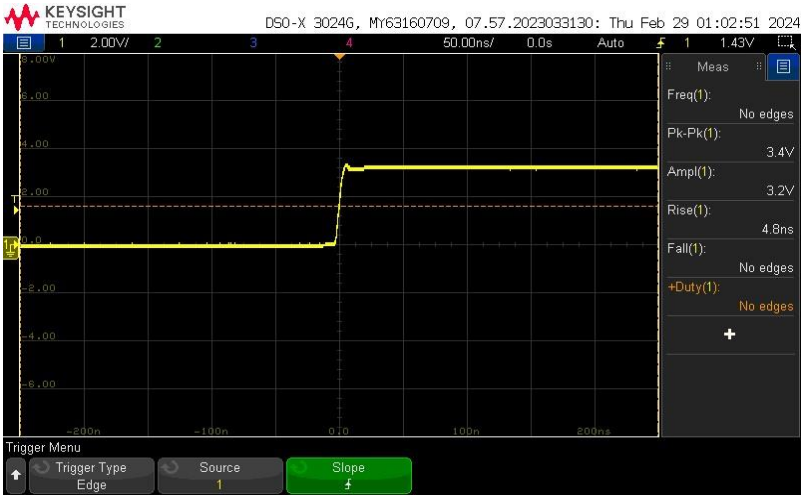
3. Rise time and fall time:



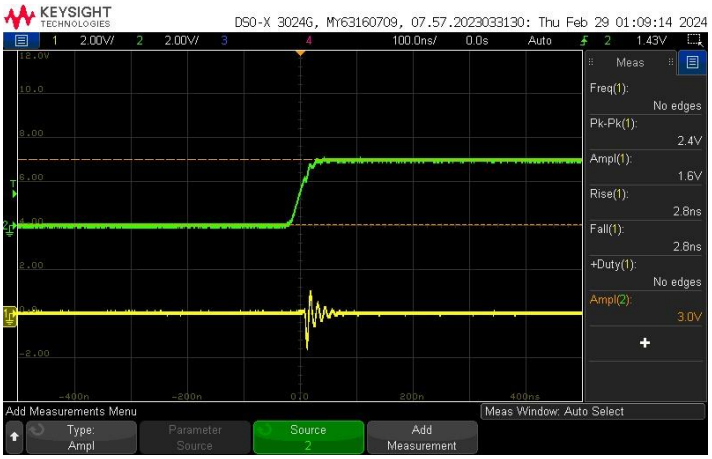


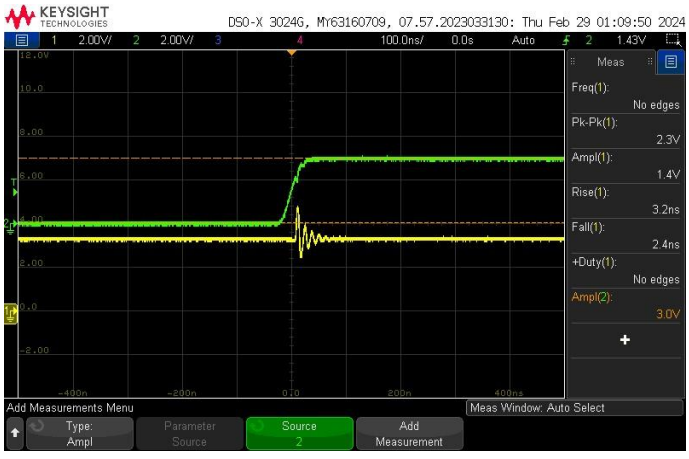
As per datasheet rise and fall time is estimated as 15ns for this LMC 555 timer. But rise time of 30ns and fall time of 41ns observed due to load at the output.

4. Output from bad practice hex inverter part of layout:



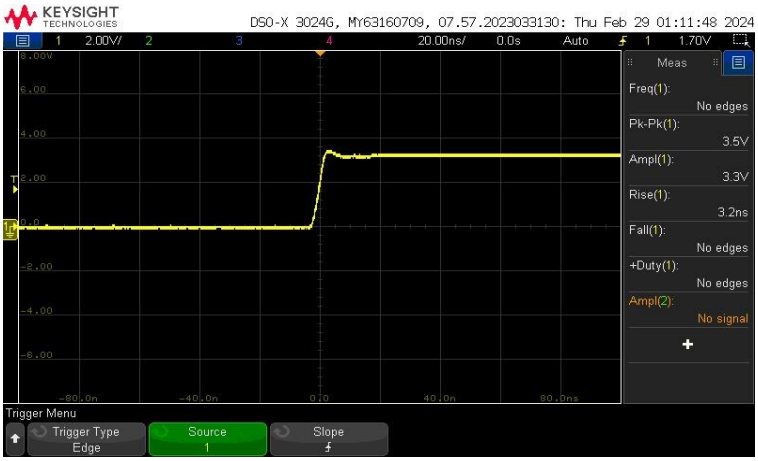
Measured rise time of 4.8ns from the triggered-out pin of inverter. In datasheet it mentioned that the transition time will be typically 8ns.



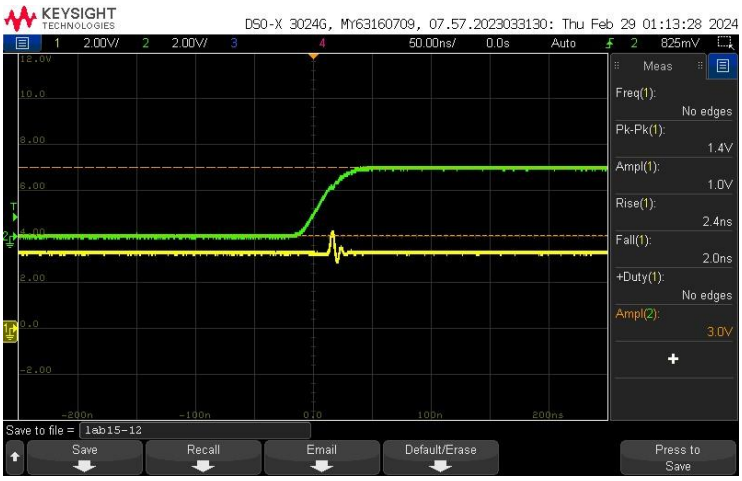


The output on the left is from quiet low and amplitude of 1.5V noise is seen because of ground debounce, which is due to common return path and lack of return plane. The right-side output is from quiet high and the amplitude of 1.4V noise observed at the switching point because of power rail noise, which in turn due to placement of decoupling capacitor for away from the IC package VCC pin.

5. Output from Good practice part with decoupling capacitor placed far:



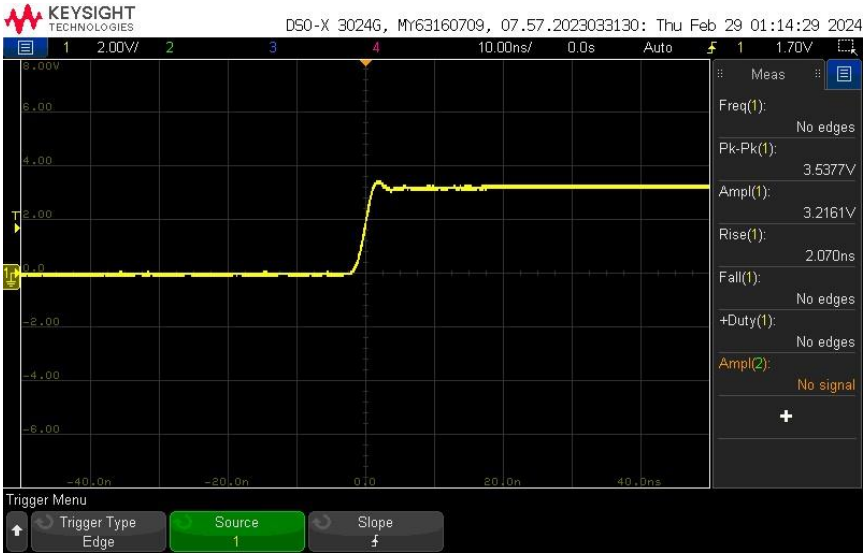
As corelation mentioned in the datasheet, the transition time depends on the Vcc applied to the inverter. As we know that the inductive noise results in the voltage variation in the power rail result in 3.2ns rise time which is lesser than what we measured in the bad practice.



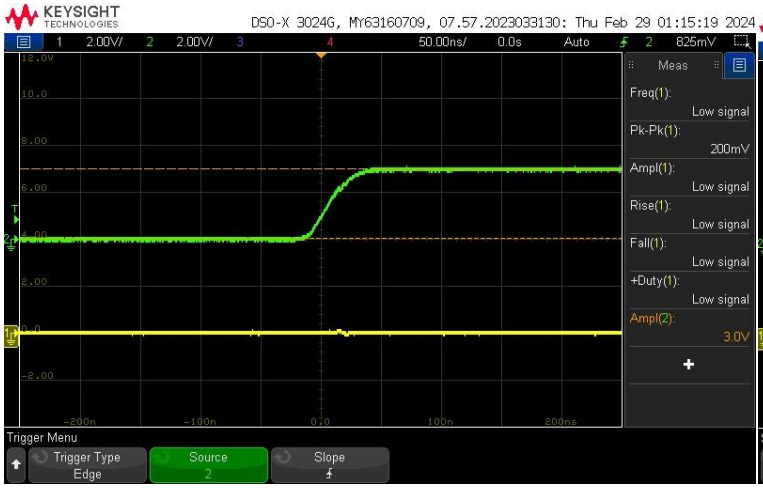
The image on the left (quiet low) shows that there is not noise seen in Volts range due to ground bounce, because of separate path and return plane is implementation. The Image on

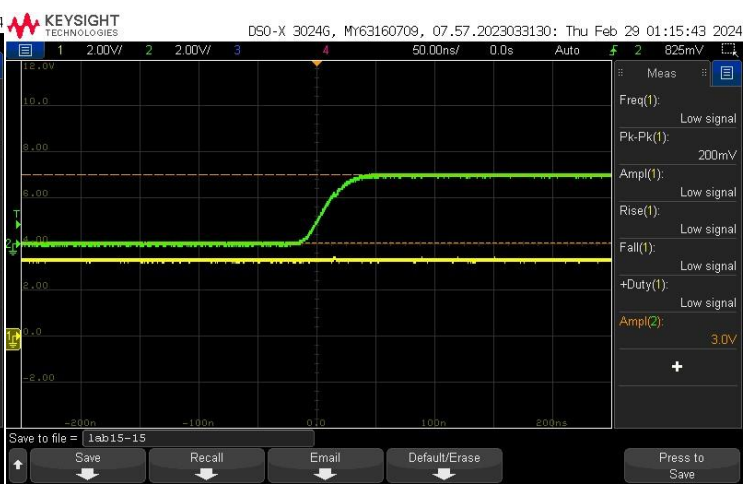
the right (quiet low) shows that there is still 1V noise to power rail, where decoupling capacitor is placed far and induced more noise from the inductance of the rail.

6. Output from good practice:



Here we can see that the rise time is further reduced to 2ns, which is because of further reduce in the induced noise in power rail.

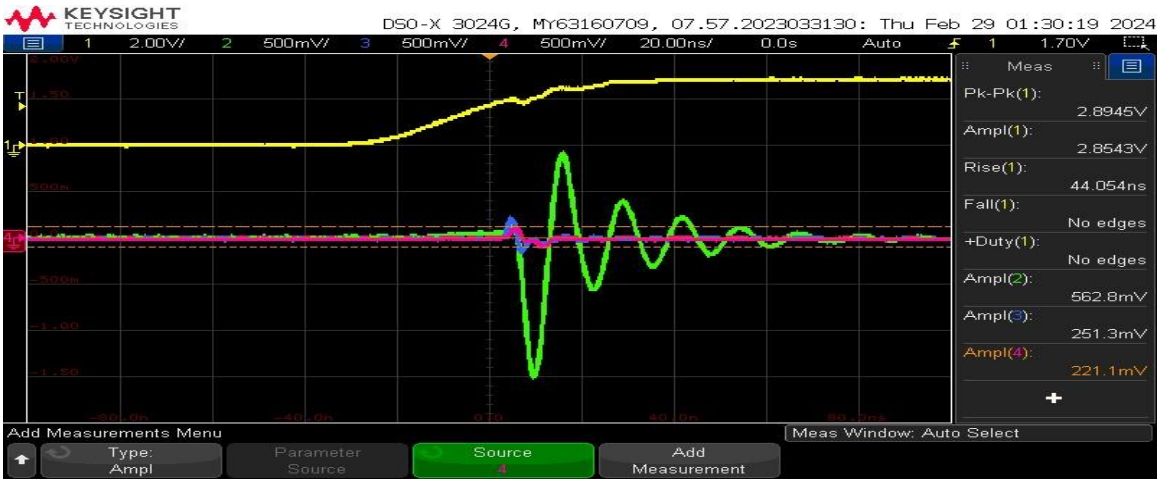




Here we can see that there is no noise seen in Volts range from both quiet low and quiet high pins, because we took every measure to reduce noise by placing decoupling capacitor close, separate return path and return plane.

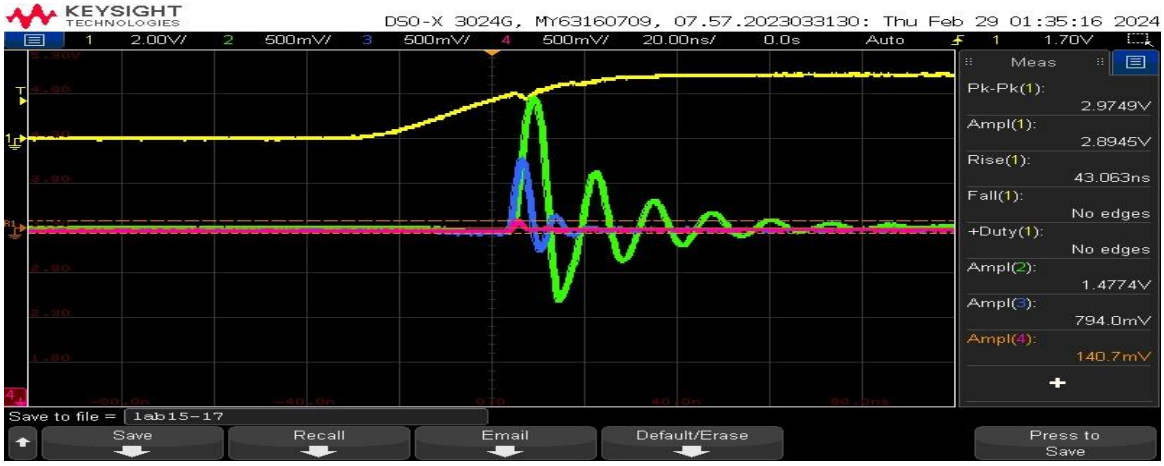
But still there will be noise in terms of millivolts. That can be seen from this next reference outputs.

7. Quiet Low output from all bad and good parts of the layout:



Green (bad part), Blue (good but far decoupling capacitor) and pink (good part) signals clearly shows that how the noise reduced in the ground plane with good practices.

8. Quiet High output from all bad and good parts of the layout:



Green (bad part), Blue (good but far decoupling capacitor) and pink (good part) signals clearly shows that how the noise reduced in the power rail with good practices.

Key learnings:

- How to test the board module wise, compare the outputs and come to conclusion by analysing the outputs such as reference voltages collected from quiet high and quiet low.
- Importance of good practice in board design like adding appropriate decoupling capacitor closer to Vcc pin of the IC package, implementation of separate ground path for every component and return plane to minimize the loop inductance and cross talk between the traces by allowing current as mentioned in skin effect.

References:

https://www.ti.com/lit/gpn/LMC555
https://www.ti.com/lit/gpn/SN74HC14