High Speed and Time Efficient Wavelet Transform on Xilinx Vertex E using Vedic Multiplier

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**ABSTRACT: With the emergence of technology in the field of communication and VLSI, also growing demand of high speed processing and low area design. Multiplier is a key factor in arithmetic operation and digital signal processing algorithm. Multiplier forms an integral part of processor design. Multiplier takes long time for execution so that there is a need of fast multiplier save the execution. For image and digital signal processing require wavelet transform so need to design a multiplier for wavelet transform which contain low area and provide high speed. This paper delineates the multiplication using Vedic multiplication technique. These design reduced hard complexity, throughput rate and different input/output data format to match different application needs. These techniques have been designed implementation on Virtex-4 FPGA. We have synthesized the proposed designs and the existing design using Synopsys tools.**

**Keywords: - Vedic Multiplier, Wavelet Transform, Xilinx Simulation**

# **Introduction**

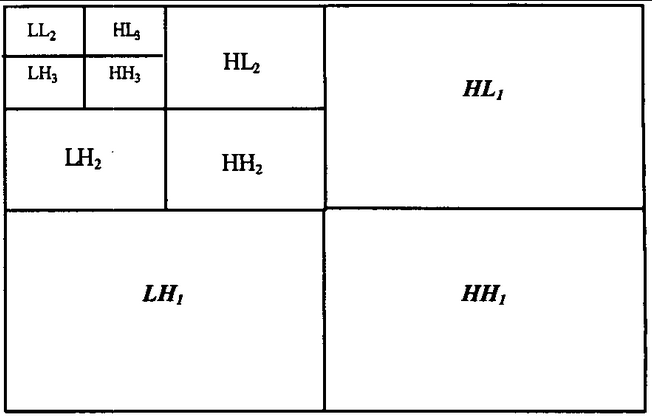
With the growth in scale of integration circuits, more and more sophisticated digital signal processing circuits are being implemented in (field programmable gate array) FPGA based circuit. Indeed, FPGA have become an attractive fabric for the implementation of computationally intensive application such as digital signal processing, image, graphics card and network processing tasks used in wireless communication. These complex signal processing circuits not only demand large computational capacity but also have high energy and area requirements. Though area and speed of operation remain the major design concerns, power consumption is also emerging as a critical factor for present VLSI system designers [1-4].

As a student in India, Vedic Mathematics is a name which is heard many times with reference to the techniques for solving mathematics problem mentally. One of the main purposes of Vedic mathematics is to transform the tedious calculations into simpler, orally manageable operation without much help of pen and paper. Any ordinary human can perform mental operations for very small magnitude of numbers and hence Vedic mathematics provides techniques to solve operations with large magnitude of numbers easily. Vedic mathematics provides more than one method for basic operations like multiplication and division. For each operation there is at least one generic method provided along with some methods which are directed towards specific cases simplifying the calculations further. Today’s CPUs are increasingly working on higher frequencies with reduction in size of transistor. Arithmetic and Logic Unit - ALU is one of the most important and critical blocks in CPU. Hence it is imperative to have fast and efficient ALU [5]. Division is the most time consuming amongst the basic mathematical calculation. In today’s computing technology functions like Sine and Cosine are also frequently required and are implemented in hardware. With these considerations, it is always important to have fast and efficient mechanism to implement mathematical functions. Vedic mathematics provides algorithms to simplify the mathematics and hence is perfect solution for the problem stated.

The entire paper has been partitioned into four parts. In II, Theoretical Background for matrix multiplication has been discussed. In III, hardware complexity and performance comparison of the proposed architecture is discussed. In IV, simulation result has been discussed. In V, conclusions and future scope of the paper work has been presented.

# **Theoretical Background**

DWT analyzes the signal by subband coding and multiresolution at different frequency band with different resolution by decomposing the signal. The resolution of a signal is changed by filtering operation scale is changed by up sampling and down sampling. DWT employs two set of function one is scaling function and another one if wavelet function which are associated with Low-Pass and High-Pass filter respectively [6]. Subband coding is a procedure when the filtering and subsampling will result in half the number of sample or half the time resolution and double the frequency resolution by Low-pass and High-pass filter. This procedure can be further repeated in three times as shown figure 2.



**Figure 1: DWT Decomposition**

# **Vedic Multiplier**

The word “Vedas” which literarily means knowledge has derivational meaning as principle and limitless store-house of all knowledge. The word Veda also refers to the sacred ancient Hindu literature which is divided into four volumes. Vedas are considered to be one of the oldest forms of written records by man. Vedas initially were passed from previous generations to next orally. Later they were transcribed in Sanskrit. A survey of all scripts available of Vedas across different part of India showed no slightest difference in them. Vedas include information from many subjects from religion, medicine, architecture, astronomy, mathematics etc. The system of Vedic mathematics is based on 16 sutras–formulas and 13 Up-sutras.

Mathematics is a root of all sciences and It is full of magic & mysteries. The ancient Indians were able to develop simple keys to solve these mysteries and this system of calculations is called Vedic Mathematics. The Vedic Mathematics approach is totally different and considered very close to the way a human mind works.

A multiplier is one of the key blocks in most of application such as cryptography, Digital Signal Processing and in other logical computations. Vedic multiplication is a logical concept and it is based on the Vedic multiplication formula (sutras), these sutras have been traditionally used for the multiplication of two numbers in the decimal number system and we use same concept on binary multiplication. This is more efficient in the multiplication of large numbers with respect to speed and area.

The proposed design evidently reduces a given 4 bit multiplication shown in below figure to a 2-bit multiplication (in fig 7) by making use of basic shifting and addition operations shown in figure 2. Similarly, for an 8 bit multiplication, the multiplier and multiplicand are grouped into 4-bit number so that it decomposes into 4×4 multiplication modules.

ca1

Ca3 S(7-4) S(2-3) S(1-0)

0 0

N(1-0) M(1-0)

Vedic Multiplier

N(3-2) M(1-0)

Vedic Multiplier

N(1-0) M(3-2)

Vedic Multiplier

N(3-2) M(3-2)

Vedic Multiplier

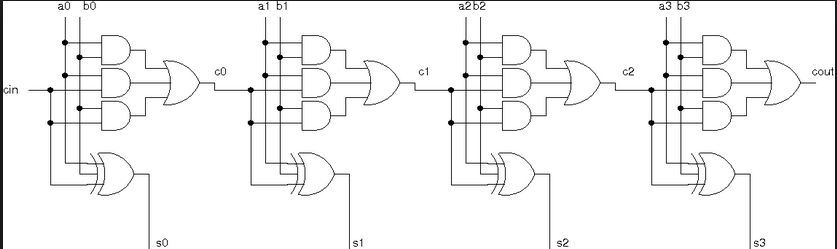
Adder

Adder

Adder

**Figure 2: Block Diagram of 4-bit Vedic Multiplier**

The 4×4 multiplier can be used for building 8×8 multiplier and 8×8 multiplier for 16×16 multiplier and so on [7].



**Figure 3: 4-bit adder**

Block diagram of Vedic multiplier is showing below figure 4 initially designed a 2×2 multiplier by Xilinx 14.1i .

B (1-0)

A (1-0)

C (3-0)

Vedic Multiplier

**Figure 4: Block Diagram of Vedic**

Which is shown in figure 5, and it would be work as input of 4×4 multiplier. Therefore efficient multiplication architecture implementation with small number such as 4-bit can be easily extended and embedded for implementing efficient 16×16 multiplication operation.

C3

C2

C1

C0

B0

A1

B1

A1

B0

A0

B1

A0

H.A

H.A

**Figure 5: 2×2 Vedic Multiplier**

The structural feature of the 16×16 multiplier is inherited from 4×4 structure. Blocks of 8 bits are worked as the input and each input-pair is handled by a separate 8×8 block which is designed using 4×4 multiplier block. These separate 8×8 block produce four partial products. These partial products are then added to generate final product of 16×16 multiplication as shown below figure 6.

# **SIMULATION RESULTS**

All the designing and experiment regarding algorithm that we have mentioned in this paper is being developed on Xilinx 14.1i Vertex 7 updated version. Xilinx 14.1i has couple of the striking features such as low memory requirement, fast debugging, and low cost. The latest release of ISETM (Integrated Software Environment) design tool provides the low memory requirement approximate 27 percentage low. ISE 14.1i that provides advanced tools like smart compile technology with better usage of their computing hardware provides faster timing closure and higher quality of results for a better time to designing solution.

7-0

7-0

Ca2

Z(15-8)

Z(7-4)

7-4

Ca1

0

Y(3-0)

X(3-0)

ca2

Y(3-0)

X(3-0)

Y(3-0)

X(3-0)

Y(3-0)

X(3-0)

8-Bit Adder

8-Bit Adder

8-Bit Adder

0

0

0

0

0

0

Ca3

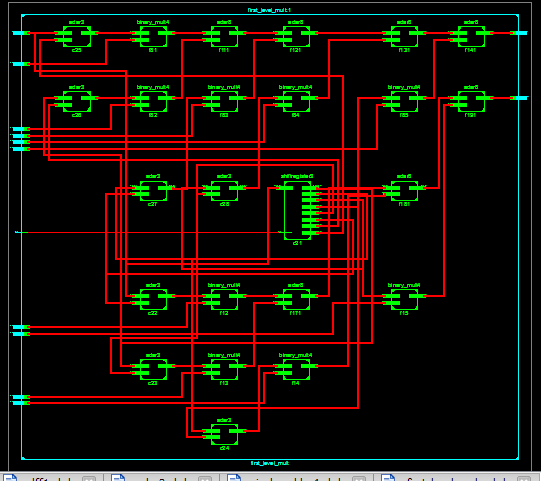
Z(3-0)

7-0

7-0

**Figure 6: 16×16 Vedic Multiplier**

All the designing and experiment regarding algorithms have been captured by VHDL and the functionality is verified by RTL and gate level simulation. Comparison result for proposed design in Vertex 7 device family in has shown the table 1 and shows the resistor transistor logic (RTL) for DWT using 4-bit Vedic multiplier figure 6 respectively.



**Figure 7: Resistor Transistor Logic (RTL) for DWT using 4-bit Vedic Multiplier**

**Table 1: Comparisons Result for DWT Architecture using 4-bit Vedic Multiplier and Existing Architecture**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | Number of Slice | Number of Slice Flip flop | 4-input LUTS | Maximum Combinational Path Delay (nsec) |
| Existing Architecture | 232 | 24 | 395 | 30.376 |
| Proposed Architecture 1 | 225 | 24 | 383 | 29.759 |
| Proposed Architecture 2 | 225 | 24 | 383 | 29.106 |

**Figure 8: Chart Diagram of different types of Device Family Using Xilinx 14.1i**

# **CONCLUSION and FUTURE SCOPE**

Multiplication or inner-product computation is usually large for various practical applications. On the other hand, most of these algorithms are currently implemented in hardware to meet the temporal requirement of real-time application [9]. We have compared the proposed designs with the existing similar design and found that, the proposed designs are used in 67 number of slice and 61 4-input LUTs respectively. Other possible improvements can also be obtained by applying different design strategies such as low-complexity Vedic multiplier less approach for optimizing the area efficient of the proposed designs.

# **REFERENCE**

1. MassoudPedram, “Design Technologies for Low Power VLSI,” Encyclopedia of Computer Science and Technology, pp. 1 – 32, 1995.
2. Pramod Kumar Meher, “Hardware-Efficient Systemization of DA-Based Calculation of Finite Digital Convolution,” IEEE Transaction on Circuits and Systems, vol. 53, no. 8, pp. 707 - 711, 2006
3. Azadeh Safari and Niras C V, “VLSI Architecture of Multiplier-less DWT Image Processor”, 978-1-4673-6349-5/13/$31.00 ©2013 IEEE.
4. Gaurav Tewari, Santu Sardar, K. A. Babu, “High-Speed & Memory Efficient 2-D DWT on Xilinx Spartan3A DSP using scalable Polyphase Structure with DA for JPEG2000 Standard”, IEEE 2011.
5. Milad Ghantous and Magdy Bayoumi, “P2E-DWT: A Parallel and Pipelined Efficient VLSI Architecture of 2-D Discrete Wavelet Transform”, 978-1-4244-9474-3/11/$26.00  
   ©2011 IEEE.
6. B. K. Mohanty and P. K. Meher, “Memory-Efficient High-Speed Convolution-based Generic Structure for Multilevel 2-D DWT”, IEEE Transactions on Circuits Systems for Video Technology. vol. 60, no. 5. Sep.2011.
7. J. Lloyd, “Parallel Formulations of Matrix-Vector Multiplication for Matrices with Large Aspect Ratios, ”in IEEE Proceedings of the Fourth Euro micro Workshop on Parallel and Distributed Processing, pp. 102-108, 1996
8. K. K. Parhi, VLSI Digital Signal Processing Systems. John Wiley & Sons, Inc. 1999.
9. Sushma R. Huddar and Sudhir Rao, Kalpana M., “Novel High Speed Vedic Mathematics Multiplier using Compressors”, 978-1-4673-5090-7/13/$31.00 ©2013 IEEE.
10. S. S. Kerur, Prakash Narchi, Jayashree C N, Harish M Kittur and Girish V A, “Implementation of Vedic multiplier for Digital Signal Processing”, International Conference on VLSI, Communication & Instrumentation (ICVCI) 2011, Proceedings published by International Joural of Computer Applications® (IJCA), pp.1-6.
11. Himanshu Thapaliyal and M.B Srinivas, “VLSI Implementation of RSA Encryption System Using Ancient Indian Vedic Mathematics”, Center for VLSI and Embedded System Technologies, International Institute of Information Technology Hyderabad, India.
12. Jagadguru Swami Sri Bharati Krishna Tirthaji Maharaja, “Vedic Mathematics: Sixteen simple Mathematical Formulae from the Veda”, Delhi(2011).