Lab Report: Lab 0

Translatch & MasterSlave

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Abstract

***Abstract*—This is the first lab of the semester titled lab-0 for two reasons: firstly, in computer science it is important to the understanding bases that 0 is seen as the first number of any number system. Secondly, this lab is in regards to two components which are not a part of the main lab goal of this course: *building a working 32 bit computer*, but rather an introduction to working with VHDL and the software tools used in the course.**

***Index Terms*—VHDL, Computer, Architecture, Boolean, Logic.**

I. Introduction

TransLatch & MasterSlave

DESCRIBE: TransLatch & MasterSlave.

A translatch is a fundamental and atomic component in computers and ICs. The purpose of a translatch is either to enable a conductor to carry a tri-state value called hi-Z using a control signal or to time the sending of bits to a strobe/clock. A masterslave is a combination of two translatches and allows a flip-flop to be edge triggered, which is beneficial to timing a certain control signal to run between cycles.

II. Materials and Methods.

In order to produce these components a description was written in Virtual Hardware Description Language (VHDL). This description would begin with the translatch and then a masterslave which is the combination of two translatches. After the description was determined to be valid by the compiler (Quartus) then a practical yet comprehensive test was written in Model-Sim. This allows virtual representations of hardware to be tested without physical production necessary. Note: in the case of production new tests should be written to test ever component as Model-Sim tests the best case.

Model-Sim Wave-Forms

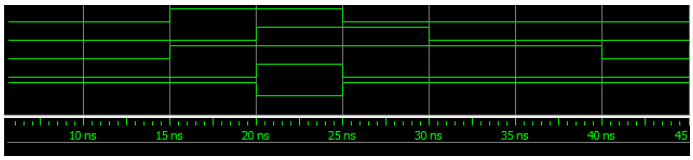

Fig. 1. The Wave-form generates by testtranslatch in Model-Sim.

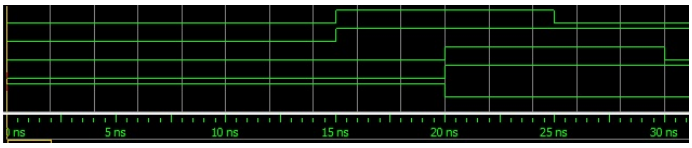

Fig. 2. The Wave-form generates by testmasterslave in Model-Sim.