Results

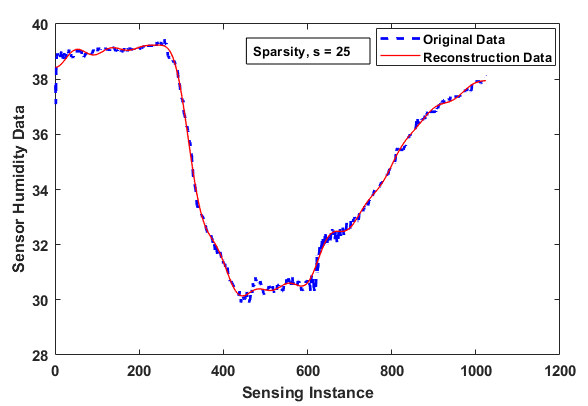


Fig 1: Original vs. reconstructed data for sparsity, *s* = 25

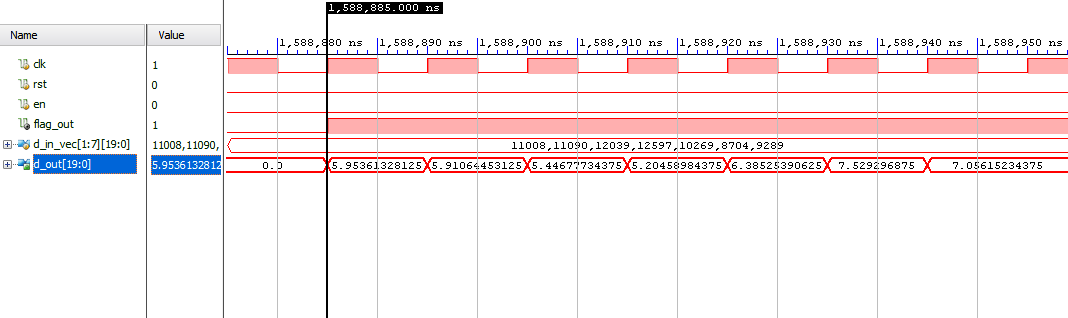


Fig 2: Diagonal matrix inverse Verilog-HDL result

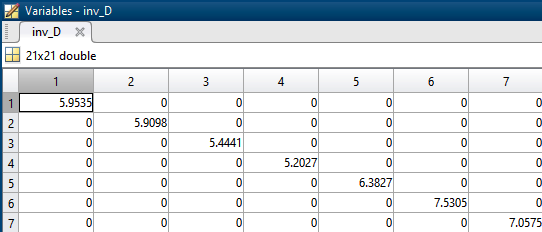


Fig 3: Diagonal matrix inverse MATLAB result

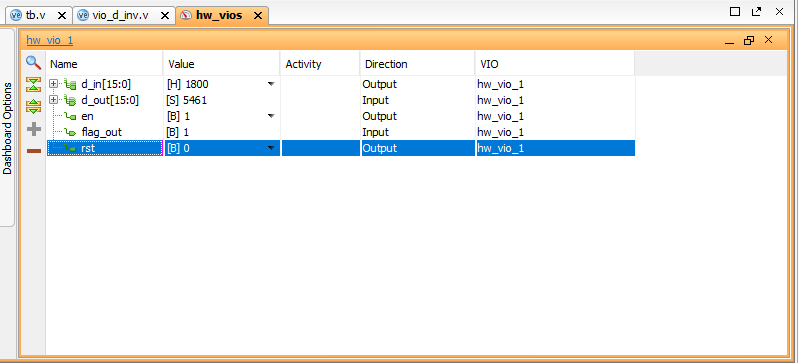


Fig 4: Diagonal matrix inverse FPGA result