Analog Multiplexers/ Demultiplexers

High-Performance Silicon-Gate CMOS

The MC74HC4051A, MC74HC4052A and MC74HC4053A utilize silicon—gate CMOS technology to achieve fast propagation delays, low ON resistances, and low OFF leakage currents. These analog multiplexers/demultiplexers control analog voltages that may vary across the complete power supply range (from $V_{\rm CC}$ to $V_{\rm EE}$).

The HC4051A, HC4052A and HC4053A are identical in pinout to the metal—gate MC14051AB, MC14052AB and MC14053AB. The Channel—Select inputs determine which one of the Analog Inputs/Outputs is to be connected, by means of an analog switch, to the Common Output/Input. When the Enable pin is HIGH, all analog switches are turned off.

The Channel-Select and Enable inputs are compatible with standard CMOS outputs; with pullup resistors they are compatible with LSTTL outputs.

These devices have been designed so that the ON resistance (R_{on}) is more linear over input voltage than R_{on} of metal-gate CMOS analog switches.

For a multiplexer/demultiplexer with injection current protection, see HC4851A and HC4852A.

Features

- Fast Switching and Propagation Speeds
- Low Crosstalk Between Switches
- Diode Protection on All Inputs/Outputs
- Analog Power Supply Range $(V_{CC} V_{EE}) = 2.0$ to 12.0 V
- Digital (Control) Power Supply Range $(V_{CC} GND) = 2.0$ to 6.0 V
- Improved Linearity and Lower ON Resistance Than Metal–Gate Counterparts
- Low Noise
- In Compliance with the Requirements of JEDEC Standard No. 7A
- Chip Complexity: HC4051A 184 FETs or 46 Equivalent Gates
 HC4052A 168 FETs or 42 Equivalent Gates
 HC4053A 156 FETs or 39 Equivalent Gates
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb–Free, Halogen Free/BFR–Free and are RoHS Compliant

This document contains information on some products that are still under development. ON Semiconductor reserves the right to change or discontinue these products without notice.



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TSSOP-16 DT SUFFIX CASE 948F



SOIC-16 D SUFFIX CASE 751B



QFN16 MN SUFFIX CASE 485AW

MARKING DIAGRAMS





SOIC-16 WIDE

TSSOP-16

= 1, 2 or 3

A = Assembly Location

WL, L = Wafer Lot YY, Y = Year

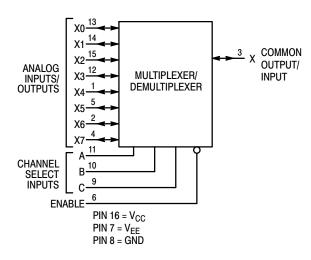
WW, W = Work Week
G or ■ = Pb–Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 13 of this data sheet.

LOGIC DIAGRAM MC74HC4051A Single-Pole, 8-Position Plus Common Off

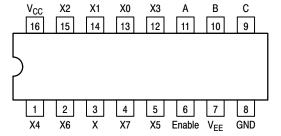


FUNCTION TABLE - MC74HC4051A

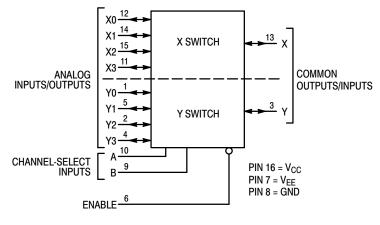
Conti	rol In			
	,	Selec	t	
Enable	С	В	Α	ON Channels
L	L	L	L	X0
L	L	L	Н	X1
L	L	Н	L	X2
L	L	Н	Н	X3
L	Н	L	L	X4
L	н	L	Н	X5
L	н	Н	L	X6
L	н	Н	Н	X7
н	X	Χ	X	NONE

X = Don't Care

Pinout: MC74HC4051A (Top View)



LOGIC DIAGRAM MC74HC4052A Double-Pole, 4-Position Plus Common Off

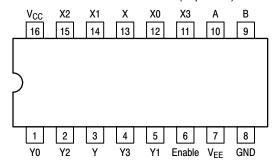


FUNCTION TABLE - MC74HC4052A

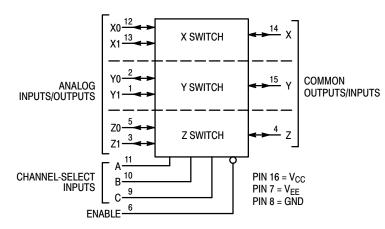
1 0110	11011 17	TDLL -	11107 7110-	10327
Cont	rol Input	s		
	Sel	lect		
Enable	В	Α	ON Ch	annels
L	L	L	Y0	X0
L	L	Н	Y1	X1
L	Н	L	Y2	X2
L	Н	Н	Y3	Х3
Н	X	Χ	NO	NE

X = Don't Care

Pinout: MC74HC4052A (Top View)



LOGIC DIAGRAM MC74HC4053A Triple Single-Pole, Double-Position Plus Common Off



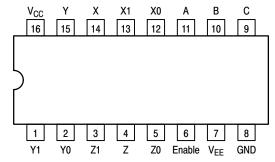
NOTE: This device allows independent control of each switch. Channel–Select Input A controls the X–Switch, Input B controls the Y–Switch and Input C controls the Z–Switch

FUNCTION TABLE - MC74HC4053A

Conti	Control Inputs					
Enable	C	Selec B	t A	01	N Chann	els
L	L	L	L	Z0	Y0	X0
L	L	L	Н	Z0	Y0	X1
L	L	Н	L	Z0	Y1	X0
L	L	Н	Н	Z0	Y1	X1
L	Н	L	L	Z1	Y0	X0
L	Н	L	Н	Z1	Y0	X1
L	Н	Н	L	Z1	Y1	X0
L	Н	Н	Н	Z1	Y1	X1
Н	X	Χ	Χ		NONE	

X = Don't Care

Pinout: MC74HC4053A (Top View)



MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	Positive DC Supply Voltage (Referenced to GND) (Referenced to V _{EE})	-0.5 to +7.0 -0.5 to +14.0	V
V _{EE}	Negative DC Supply Voltage (Referenced to GND)	-7.0 to +5.0	V
V _{IS}	Analog Input Voltage	V _{EE} – 0.5 to V _{CC} + 0.5	V
V _{in}	Digital Input Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
- 1	DC Current, Into or Out of Any Pin	±25	mA
P _D	Power Dissipation in Still Air, SOIC Package† TSSOP Package†	500 450	mW
T _{stg}	Storage Temperature Range	-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds SOIC or TSSOP Package	260	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND \leq (V_{in} or V_{out}) \leq V_{CC} .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or $V_{\rm CC}$). Unused outputs must be left open.

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

†Derating: SOIC Package: -7 mW/°C from 65° to 125°C TSSOP Package: -6.1 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V _{CC}	Positive DC Supply Voltage	(Referenced to GND) (Referenced to V _{EE})	2.0 2.0	6.0 12.0	V
V _{EE}	Negative DC Supply Voltage, Output (Referenced to GND)		-6.0	GND	V
V _{IS}	Analog Input Voltage		V _{EE}	V _{CC}	V
V _{in}	Digital Input Voltage (Referenced to GND)		GND	V _{CC}	V
V _{IO} *	Static or Dynamic Voltage Across Switch			1.2	V
T _A	Operating Temperature Range, All Package Types		- 55	+125	°C
t _r , t _f	Input Rise/Fall Time (Channel Select or Enable Inputs)	$V_{CC} = 2.0 \text{ V}$ $V_{CC} = 3.0 \text{ V}$ $V_{CC} = 4.5 \text{ V}$ $V_{CC} = 6.0 \text{ V}$	0 0 0	1000 600 500 400	ns

DC CHARACTERISTICS — Digital Section (Voltages Referenced to GND) VEE = GND, Except Where Noted

				V _{CC}	Guara	nteed Lim	nit	
Symbol	Parameter	Conditio	n	V	–55 to 25°C	≤85°C	≤125°C	Unit
V _{IH}	Minimum High-Level Input Voltage, Channel-Select or Enable Inputs	R _{on} = Per Spec		2.0 3.0 4.5 6.0	1.50 2.10 3.15 4.20	1.50 2.10 3.15 4.20	1.50 2.10 3.15 4.20	V
V _{IL}	Maximum Low-Level Input Voltage, Channel-Select or Enable Inputs	R _{on} = Per Spec		2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	V
I _{in}	Maximum Input Leakage Current, Channel–Select or Enable Inputs	$V_{in} = V_{CC}$ or GND, $V_{EE} = -6.0 \text{ V}$		6.0	± 0.1	± 1.0	± 1.0	μΑ
I _{CC}	Maximum Quiescent Supply Current (per Package)	Channel Select, Enab $V_{IS} = V_{CC}$ or GND; $V_{IO} = 0 \text{ V}$		6.0 6.0	1 4	10 40	20 80	μΑ

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

*For voltage drops across switch greater than 1.2 V (switch on), excessive V_{CC} current may be drawn; i.e., the current out of the switch may contain both V_{CC} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

DC CHARACTERISTICS — Analog Section

					Guara	nteed Lim	nit	
Symbol	Parameter	Condition	V _{CC}	V _{EE}	−55 to 25°C	≤85°C	≤125°C	Unit
R _{on}	Maximum "ON" Resistance	$V_{in} = V_{IL}$ or V_{IH} ; $V_{IS} = V_{CC}$ to V_{EE} ; $I_S \le 2.0$ mA (Figures 1, 2)	4.5 4.5 6.0	0.0 - 4.5 - 6.0	190 120 100	240 150 125	280 170 140	Ω
		$V_{in} = V_{IL} \text{ or } V_{IH}; V_{IS} = V_{CC} \text{ or } V_{EE} \text{ (Endpoints); } I_S \leq 2.0 \text{ mA} $ (Figures 1, 2)	4.5 4.5 6.0	0.0 - 4.5 - 6.0	150 100 80	190 125 100	230 140 115	
ΔR_{on}	Maximum Difference in "ON" Resistance Between Any Two Channels in the Same Package	$\begin{split} &V_{in} = V_{IL} \text{ or } V_{IH}; \\ &V_{IS} = 1/2 (V_{CC} - V_{EE}); \\ &I_{S} \leq 2.0 \text{ mA} \end{split}$	4.5 4.5 6.0	0.0 - 4.5 - 6.0	30 12 10	35 15 12	40 18 14	Ω
l _{off}	Maximum Off-Channel Leakage Current, Any One Channel	$V_{\text{in}} = V_{\text{IL}} \text{ or } V_{\text{IH}};$ $V_{\text{IO}} = V_{\text{CC}} - V_{\text{EE}};$ Switch Off (Figure 3)	6.0	- 6.0	0.1	0.5	1.0	μΑ
	Maximum Off–ChannelHC4051A Leakage Current, HC4052A Common Channel HC4053A	$V_{IO} = V_{CC} - V_{EE};$	6.0 6.0 6.0	- 6.0 - 6.0 - 6.0	0.2 0.1 0.1	2.0 1.0 1.0	4.0 2.0 2.0	
I _{on}	Maximum On–ChannelHC4051A Leakage Current, HC4052A Channel–to–Channel HC4053A	Switch-to-Switch =	6.0 6.0 6.0	- 6.0 - 6.0 - 6.0	0.2 0.1 0.1	2.0 1.0 1.0	4.0 2.0 2.0	μΑ

AC CHARACTERISTICS ($C_L = 50 \text{ pF}$, Input $t_r = t_f = 6 \text{ ns}$)

			V _{CC}	Guara	nteed Lin	nit	
Symbol	Parameter		V	–55 to 25°C	≤85°C	≤125°C	Unit
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Channel–Select to Analog (Figure 9)	g Output	2.0 3.0 4.5 6.0	270 90 59 45	320 110 79 65	350 125 85 75	ns
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Analog Input to Analog O (Figure 10)	utput	2.0 3.0 4.5 6.0	40 25 12 10	60 30 15 13	70 32 18 15	ns
t _{PLZ} , t _{PHZ}	Maximum Propagation Delay, Enable to Analog Output (Figure 11)		2.0 3.0 4.5 6.0	160 70 48 39	200 95 63 55	220 110 76 63	ns
t _{PZL} , t _{PZH}	Maximum Propagation Delay, Enable to Analog Output (Figure 11)		2.0 3.0 4.5 6.0	245 115 49 39	315 145 69 58	345 155 83 67	ns
C _{in}	Maximum Input Capacitance, Channel-Select or Enable	e Inputs		10	10	10	pF
C _{I/O}	Maximum Capacitance	Analog I/O		35	35	35	pF
	(All Switches Off) Common O	/I: HC4051A HC4052A HC4053A		130 80 50	130 80 50	130 80 50	
	F	eed-through		1.0	1.0	1.0	
			Typica	I @ 25°C, V _{CC}	= 5.0 V, V	_{EE} = 0 V	
C _{PD}	Power Dissipation Capacitance (Figure 13)*	HC4051A HC4052A HC4053A		45 80 45			pF

^{*} Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

ADDITIONAL APPLICATION CHARACTERISTICS (GND = 0 V)

			v _{cc}	V _{EE}		Limit*	•	
Symbol	Parameter	Condition	V	V	25°C			Unit
BW	Maximum On–Channel Bandwidth or Minimum Frequency Response (Figure 6)	f _{in} = 1MHz Sine Wave; Adjust f _{in} Voltage to Obtain 0dBm at V _{OS} ; Increase f _{in} Frequency Until dB Meter Reads –3dB;	2.25 4.50	-2.25 -4.50	'51 80 80	'52 95 95	'53 120 120	MHz
		$R_L = 50\Omega$, $C_L = 10pF$	6.00	-6.00	80	95	120	
-	Off-Channel Feed-through Isolation (Figure 7)	f_{in} = Sine Wave; Adjust f_{in} Voltage to Obtain 0dBm at V_{IS} f_{in} = 10kHz, R_L = 600 Ω , C_L = 50pF	2.25 4.50 6.00	-2.25 -4.50 -6.00		-50 -50 -50		dB
		f_{in} = 1.0MHz, R_L = 50 Ω , C_L = 10pF	2.25 4.50 6.00	-2.25 -4.50 -6.00		-40 -40 -40		
_	Feedthrough Noise. Channel–Select Input to Common I/O (Figure 8)	$\begin{split} V_{in} & \leq \text{1MHz Square Wave } (t_r = t_f = 6\text{ns}); \\ \text{Adjust } R_L \text{ at Setup so that } I_S = 0\text{A}; \\ \text{Enable} & = \text{GND} \qquad R_L = 600\Omega, \ C_L = 50\text{pF} \end{split}$	2.25 4.50 6.00	-2.25 -4.50 -6.00		25 105 135		mV_{PP}
		R_L = 10kΩ, C_L = 10pF	2.25 4.50 6.00	-2.25 -4.50 -6.00		35 145 190		
_	Crosstalk Between Any Two Switches (Figure 12) (Test does not apply to HC4051A)	f_{in} = Sine Wave; Adjust f_{in} Voltage to Obtain 0dBm at V_{IS} f_{in} = 10kHz, R_L = 600 Ω , C_L = 50pF	2.25 4.50 6.00	-2.25 -4.50 -6.00		-50 -50 -50		dB
		$f_{in} = 1.0MHz, R_L = 50\Omega, C_L = 10pF$	2.25 4.50 6.00	-2.25 -4.50 -6.00		-60 -60 -60		
THD	Total Harmonic Distortion (Figure 14)	f_{in} = 1kHz, R _L = 10k Ω , C _L = 50pF THD = THD _{measured} - THD _{source} V _{IS} = 4.0V _{PP} sine wave V _{IS} = 8.0V _{PP} sine wave	2.25 4.50	-2.25 -4.50		0.10 0.08		%
		$V_{IS} = 11.0V_{PP}$ sine wave	6.00	-6.00		0.05		

^{*}Limits not tested. Determined by design and verified by qualification.

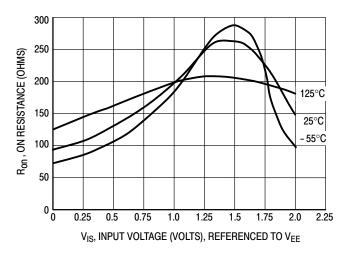


Figure 1a. Typical On Resistance, $V_{CC} - V_{EE} = 2.0 \text{ V}$

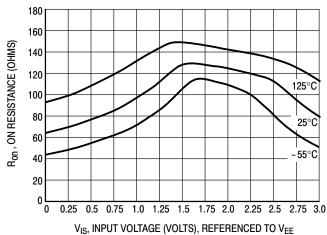


Figure 1b. Typical On Resistance, $V_{CC} - V_{EE} = 3.0 \text{ V}$

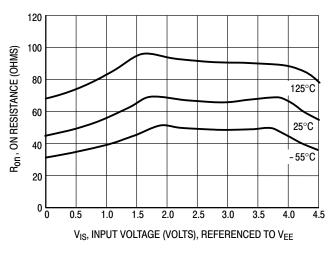
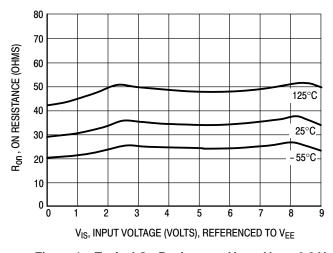


Figure 1c. Typical On Resistance, $V_{CC} - V_{EE} = 4.5 \text{ V}$

Figure 1d. Typical On Resistance, $V_{CC} - V_{EE} = 6.0 \text{ V}$



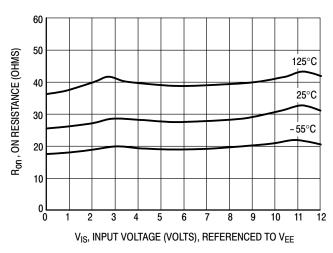


Figure 1e. Typical On Resistance, $V_{CC} - V_{EE} = 9.0 \text{ V}$

Figure 1f. Typical On Resistance, $V_{CC} - V_{EE} = 12.0 \text{ V}$

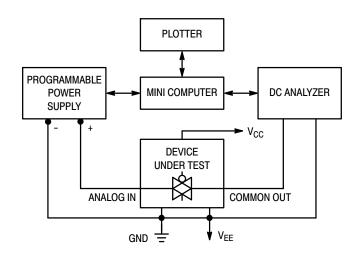


Figure 2. On Resistance Test Set-Up

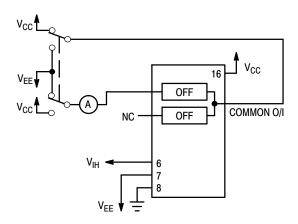


Figure 3. Maximum Off Channel Leakage Current, Any One Channel, Test Set-Up

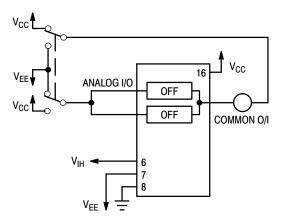


Figure 4. Maximum Off Channel Leakage Current, Common Channel, Test Set-Up

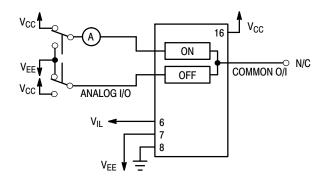


Figure 5. Maximum On Channel Leakage Current, Channel to Channel, Test Set-Up

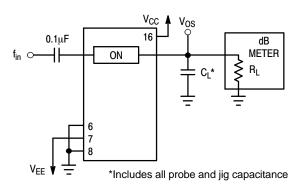


Figure 6. Maximum On Channel Bandwidth,
Test Set-Up

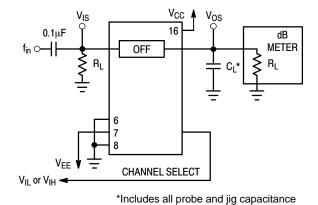
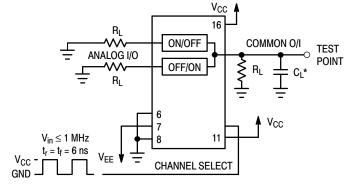
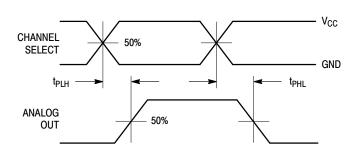


Figure 7. Off Channel Feedthrough Isolation, Test Set-Up



*Includes all probe and jig capacitance

Figure 8. Feedthrough Noise, Channel Select to Common Out, Test Set-Up



ANALOG I/O

OFF/ON

TEST
POINT

CHANNEL SELECT

*Includes all probe and jig capacitance

Figure 9a. Propagation Delays, Channel Select to Analog Out

Figure 9b. Propagation Delay, Test Set-Up Channel Select to Analog Out

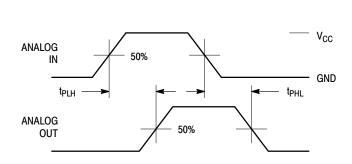
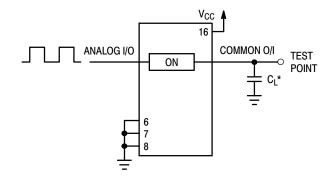


Figure 10a. Propagation Delays, Analog In to Analog Out



*Includes all probe and jig capacitance

 V_{CC} 90% **ENABLE** 50% 10% **GND** t_{PZL} t_{PLZ} HIGH **IMPEDANCE ANALOG** 50% OUT 10% V_{OL} t_{PZH} t_{PHZ} V_{OH} 90% **ANALOG** 50% OUT

Figure 11a. Propagation Delays, Enable to Analog Out

Figure 10b. Propagation Delay, Test Set-Up Analog In to Analog Out

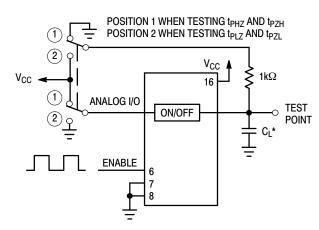
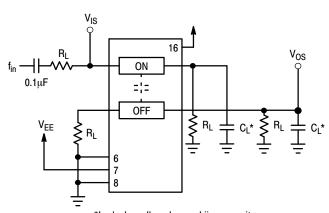


Figure 11b. Propagation Delay, Test Set-Up
Enable to Analog Out

HIGH IMPEDANCE



*Includes all probe and jig capacitance

Figure 12. Crosstalk Between Any Two Switches, Test Set-Up

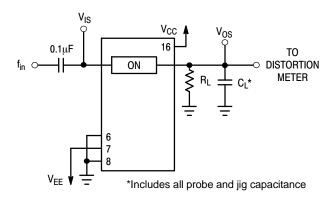


Figure 14a. Total Harmonic Distortion, Test Set-Up

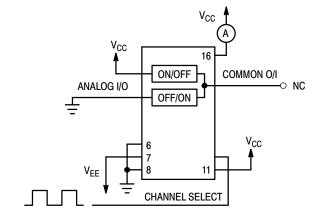


Figure 13. Power Dissipation Capacitance, Test Set-Up

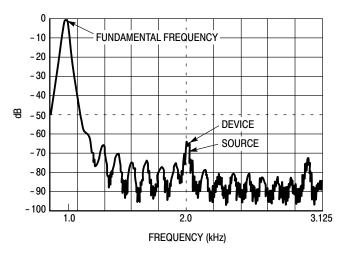


Figure 14b. Plot, Harmonic Distortion

APPLICATIONS INFORMATION

The Channel Select and Enable control pins should be at V_{CC} or GND logic levels. V_{CC} being recognized as a logic high and GND being recognized as a logic low. In this example:

$$V_{CC} = +5V = logic high$$

 $GND = 0V = logic low$

The maximum analog voltage swings are determined by the supply voltages V_{CC} and V_{EE} . The positive peak analog voltage should not exceed V_{CC} . Similarly, the negative peak analog voltage should not go below V_{EE} . In this example, the difference between V_{CC} and V_{EE} is ten volts. Therefore, using the configuration of Figure 15, a maximum analog signal of ten volts peak—to—peak can be controlled. Unused analog inputs/outputs may be left floating (i.e., not connected). However, tying unused analog inputs and

outputs to V_{CC} or GND through a low value resistor helps minimize crosstalk and feed-through noise that may be picked up by an unused switch.

Although used here, balanced supplies are not a requirement. The only constraints on the power supplies are that:

$$\begin{split} V_{CC} - GND &= 2 \text{ to 6 volts} \\ V_{EE} - GND &= 0 \text{ to -6 volts} \\ V_{CC} - V_{EE} &= 2 \text{ to 12 volts} \\ and V_{EE} &\leq GND \end{split}$$

When voltage transients above V_{CC} and/or below V_{EE} are anticipated on the analog channels, external Germanium or Schottky diodes (D_x) are recommended as shown in Figure 16. These diodes should be able to absorb the maximum anticipated current surges during clipping.

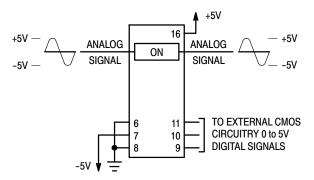


Figure 15. Application Example

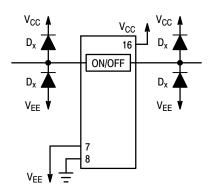
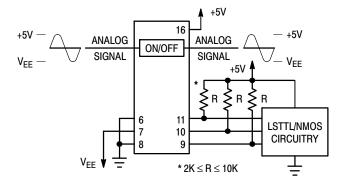
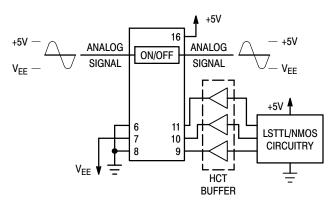


Figure 16. External Germanium or **Schottky Clipping Diodes**

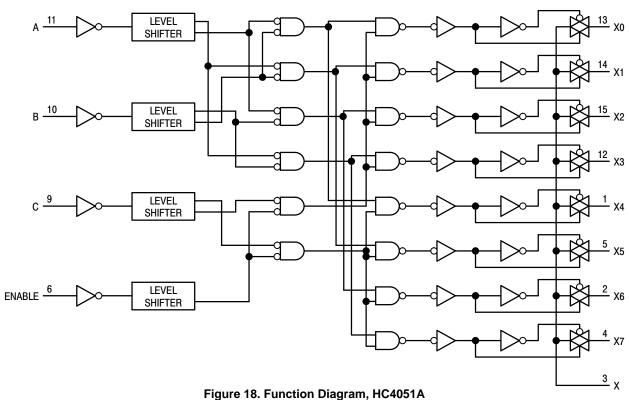


a. Using Pull-Up Resistors



b. Using HCT Interface

Figure 17. Interfacing LSTTL/NMOS to CMOS Inputs



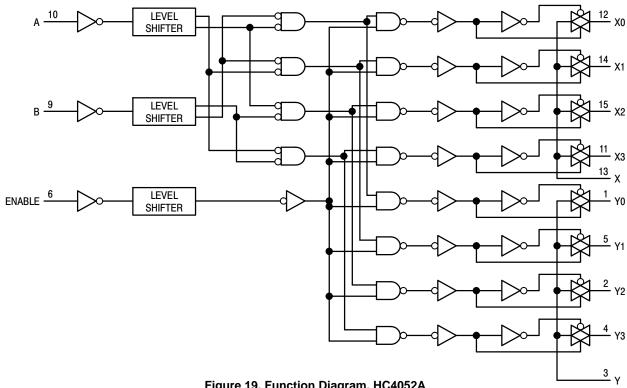


Figure 19. Function Diagram, HC4052A

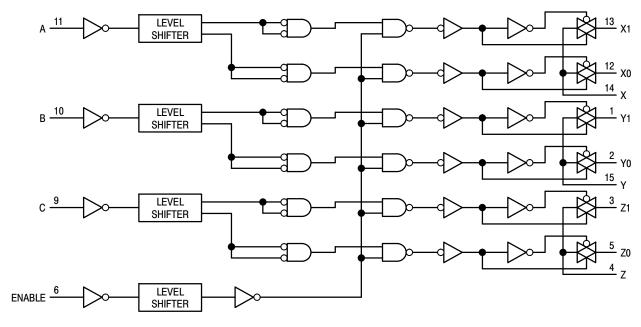


Figure 20. Function Diagram, HC4053A

ORDERING INFORMATION

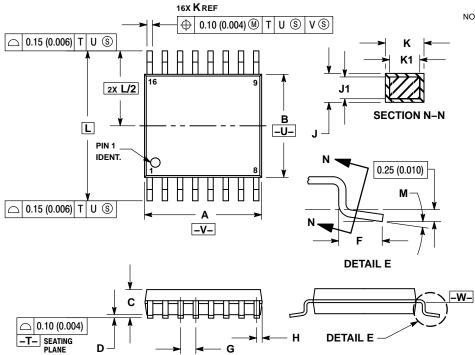
Device	Package	Shipping [†]
MC74HC4051ADG		48 Units / Rail
MC74HC4051ADR2G	SOIC-16 (Pb-Free)	2500 Units / Tape & Reel
NLV74HC4051ADR2G*	(. 2	2500 Units / Tape & Reel
MC74HC4051ADWG		48 Units / Rail
MC74HC4051ADWR2G	SOIC-16 WIDE (Pb-Free)	1000 Units / Tape & Reel
NLVHC4051ADWR2G*	(1.5.1.33)	1000 Units / Tape & Reel
MC74HC4051ADTG		96 Units / Rail
MC74HC4051ADTR2G	TSSOP-16 (Pb-Free)	2500 Units / Tape & Reel
NLVHC4051ADTR2G*	(151166)	2500 Units / Tape & Reel
MC74HC4052ADG	0010.40	48 Units / Rail
MC74HC4052ADR2G	SOIC-16 (Pb-Free)	2500 Units / Tape & Reel
NLV74HC4052ADR2G*	, ,	2500 Units / Tape & Reel
MC74HC4052ADWG	SOIC-16 WIDE	48 Units / Rail
MC74HC4052ADWR2G	(Pb-Free)	1000 Units / Tape & Reel
MC74HC4052ADTG		96 Units / Rail
MC74HC4052ADTR2G	TSSOP-16	2500 Units / Tape & Reel
NLV74HC4052ADTR2G*	(Pb-Free)	2500 Units / Tape & Reel
NLVHC4052ADTR2G*		2500 Units / Tape & Reel
NLVHC4052AMNTWG* (In Development)	QFN16 (Pb–Free)	3000 Units / Tape & Reel
	T	
MC74HC4053ADG	SOIC-16	48 Units / Rail
MC74HC4053ADR2G	(Pb-Free)	2500 Units / Tape & Reel
NLV74HC4053ADR2G*		2500 Units / Tape & Reel
MC74HC4053ADWG		48 Units / Rail
NLV74HC4053ADWRG*	SOIC-16 WIDE	1000 Units / Tape & Reel
MC74HC4053ADWR2G	(Pb-Free)	1000 Units / Tape & Reel
NLV74HC4053ADWR2G*		1000 Units / Tape & Reel
MC74HC4053ADTG		96 Units / Rail
MC74HC4053ADTR2G	TSSOP-16 (Pb-Free)	2500 Units / Tape & Reel
NLVHC4053ADTR2G*	(2500 Units / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

^{*}NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

PACKAGE DIMENSIONS

TSSOP-16 CASE 948F **ISSUE B**



NOTES:

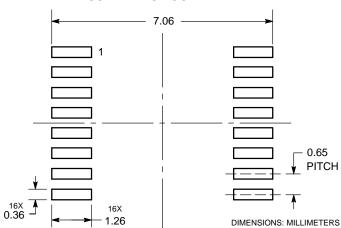
- JIES:

 1. DIMENSIONING AND TOLERANCING PER
 ANSI Y14.5M, 1982.

 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A DOES NOT INCLUDE MOLD
 FLASH. PROTRUSIONS OR GATE BURRS.
 MOLD FLASH OR GATE BURRS SHALL NOT
- EXCEED 0.15 (0.006) PER SIDE.
 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
 INTERLEAD FLASH OR PROTRUSION SHALL
- INTERLEAD FLASH OR PROTRUSION SI NOT EXCEED 0.25 (0.010) PER SIDE. 5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
- 6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY. 7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INC	HES
DIM	MIN	MAX	MIN	MAX
Α	4.90	5.10	0.193	0.200
В	4.30	4.50	0.169	0.177
С		1.20		0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65	BSC	0.026	BSC
Н	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40		0.252	
М	0°	8°	0°	8°

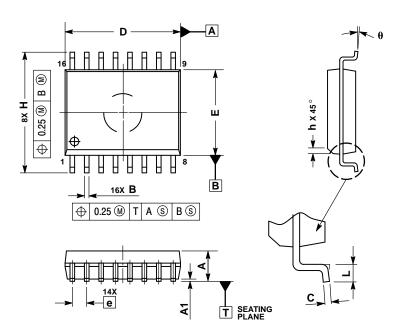
SOLDERING FOOTPRINT*



^{*}For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

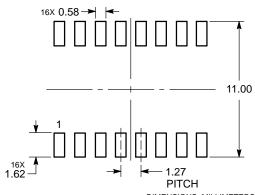
SOIC-16 WB CASE 751G-03 ISSUE D



- NOTES:
 1. DIMENSIONS ARE IN MILLIMETERS.
 2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
 3. DIMENSIONS D AND E DO NOT INLCUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
 5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIN	MILLIMETERS				
DIM	MIN	MAX				
Α	2.35	2.65				
A1	0.10	0.25				
В	0.35	0.49				
С	0.23	0.32				
D	10.15	10.45				
Е	7.40	7.60				
е	1.27	BSC				
Н	10.05	10.55				
h	0.25	0.75				
L	0.50	0.90				
а	0 °	7 °				

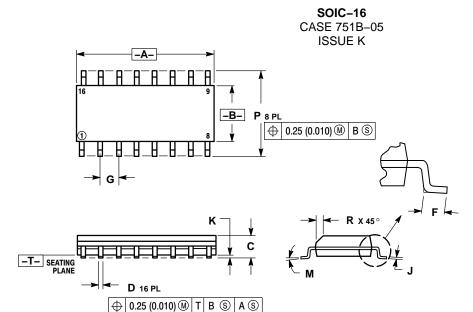
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

^{*}For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

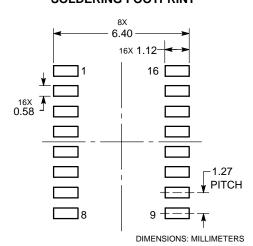


- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 CONTROLLING DIMENSION: MILLIMETER.
 DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
 MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 DIMENSION D DOES NOT INCLUDE DAMBAR
 PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D
 DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
Α	9.80	10.00	0.386	0.393
В	3.80	4.00	0.150	0.157
С	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
Р	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

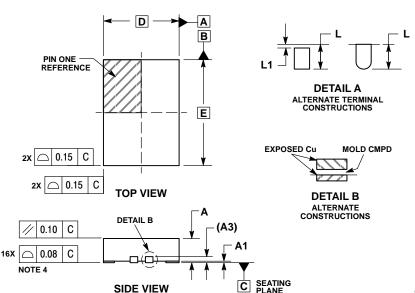
SOLDERING FOOTPRINT*



*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

QFN16, 2.5x3.5, 0.5P CASE 485AW **ISSUE O**

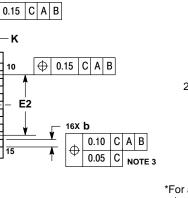


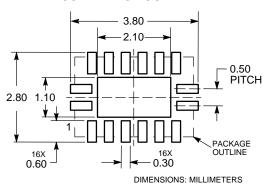
BOTTOM VIEW

- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- CONTROLLING DIMENSION: MILLIMETERS.
 DIMENSIONS b APPLIES TO PLATED
- DIMENSIONS AFFILIES TO FLATER
 TERMINAL AND IS MEASURED BETWEEN
 0.15 AND 0.30 MM FROM TERMINAL.
 COPLANARITY APPLIES TO THE EXPOSED
 PAD AS WELL AS THE TERMINALS.

	MILLIMETERS		
DIM	MIN	MAX	
Α	0.80	1.00	
A1	0.00	0.05	
А3	0.20 REF		
b	0.20	0.30	
D	2.50 BSC		
D2	0.85	1.15	
Е	3.50 BSC		
E2	1.85	2.15	
е	0.50 BSC		
K	0.20		
L	0.35	0.45	
L1		0.15	

SOLDERING FOOTPRINT*





*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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