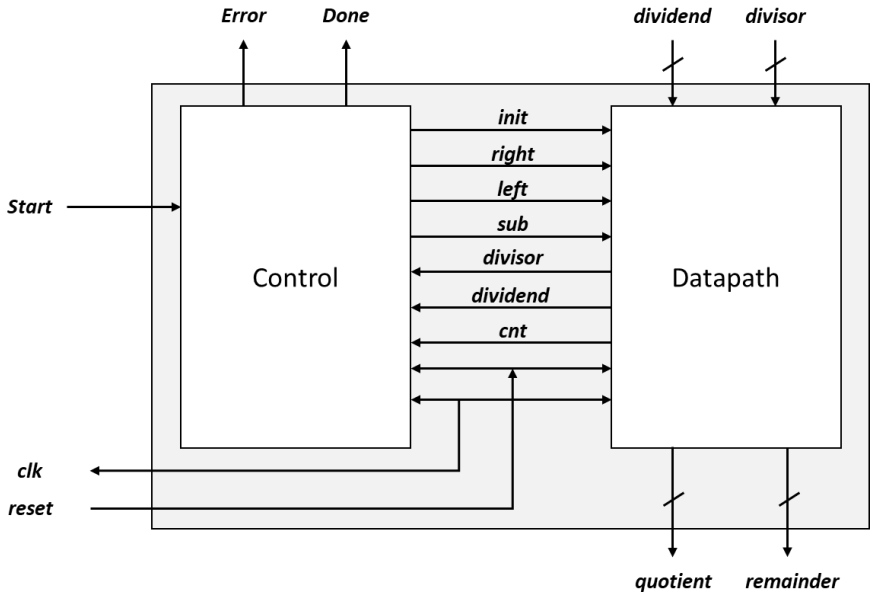
## FINAL PROJECT

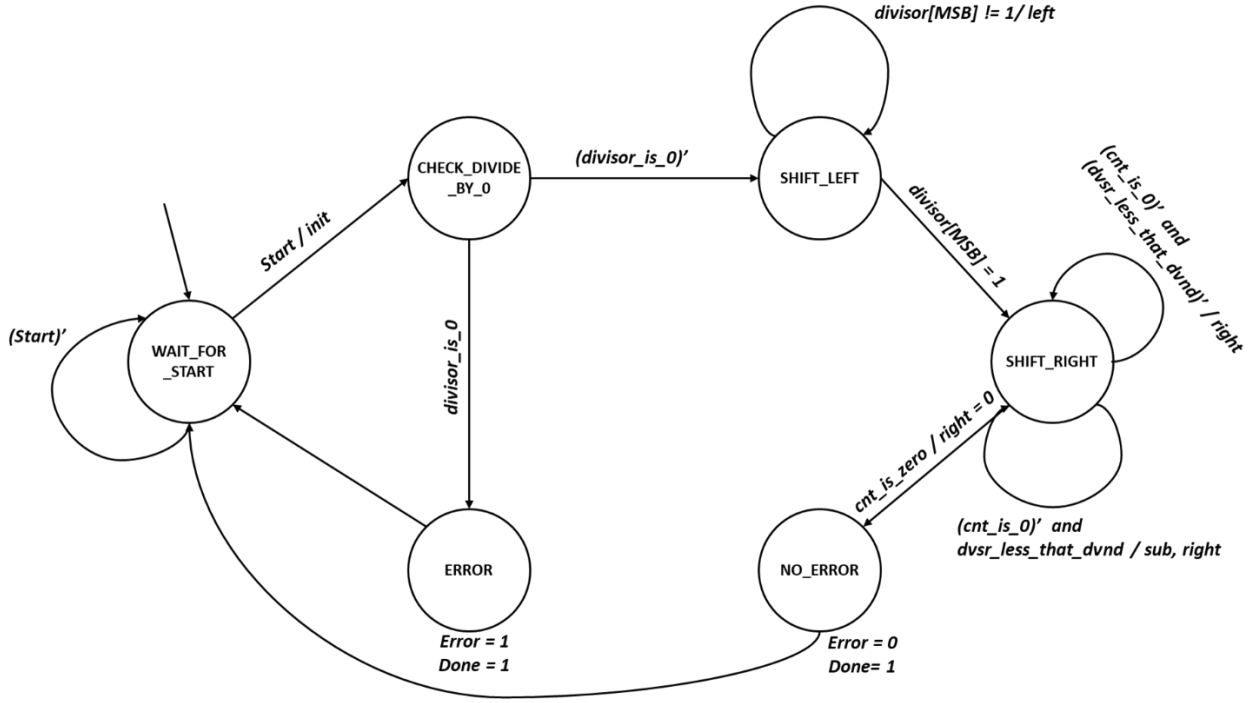
This project can be done in pairs (at most two students per group). A group with any graduate student(s) must meet all graduate requirements.

**Included below is a control and Datapath circuit of the "pen and paper" long division algorithm for two 32-bit unsigned binary numbers.**



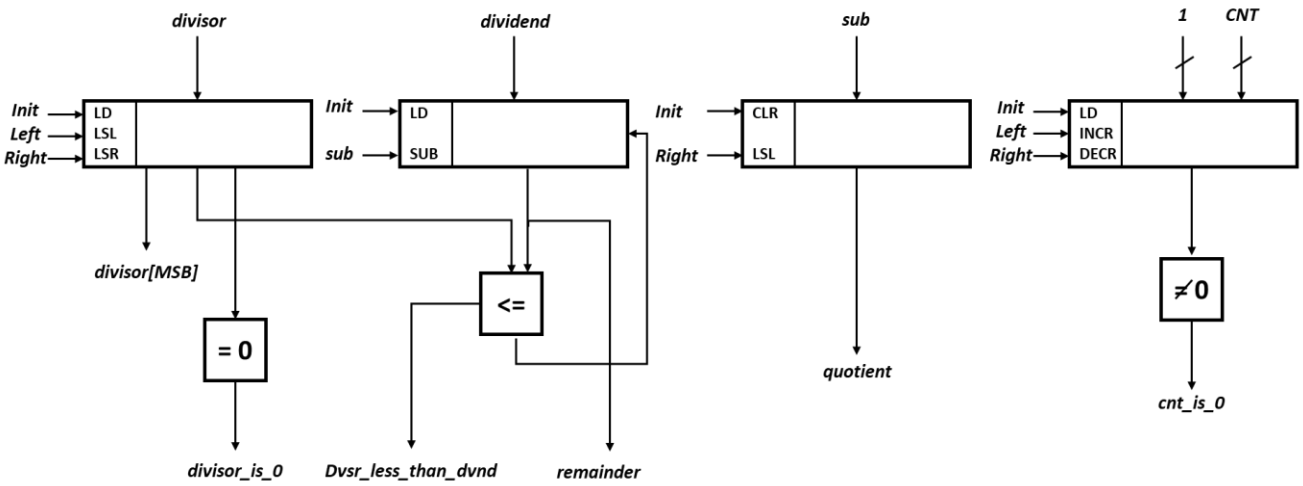

## CONTROL PATH

**Inputs:** Start, Reset, Clk
**Outputs:** Done, Error
**Control Signals:** init, left, right, sub



## Datapath

**Inputs:** divisor, dividend
**Outputs:** quotient, remainder
**Status signals:** cnt_is_0, divisor_is0, dvsr_less_than_dvnd, divisor[MSB]




- Describe the circuit in Verilog (parameterized for size = 32)
- Write a Testbench for the control path (finite state machine)
- Synthesize using TCL scripts in Vivado's Non-Project Mode

## DESIGN REQUIREMENTS

**VIVADO TCL SYNTHESIS SCRIPT:**

1. The main synth.tcl script should be executable using either batch or TCL mode
2. All constraints applied should be in a constraints.xdc file, sourced by the synthesis script
3. The synth.tcl script when executed should create a Reports folder and export all generated reports into the specified folder

**GRADUATE REQUIREMENTS:**

Your synthesized circuit must meet the following requirements:

1. The area of the synthesized circuit must be under 106 Slice LUTs
2. The frequency of the resulting circuit must be at least 350 MHz

**UNDERGRDAUATE REQUIREMENTS:**

Your synthesized circuit must meet the following requirements:

1. The area of the synthesized circuit must be under 115 Slice LUTs
2. The frequency of the resulting circuit must be at least 500 MHz

## SUBMIT

1. All your Verilog design file(s)
2. All timing and area reports showing that your design meets the requirements
3. Your compile TCL script(s)