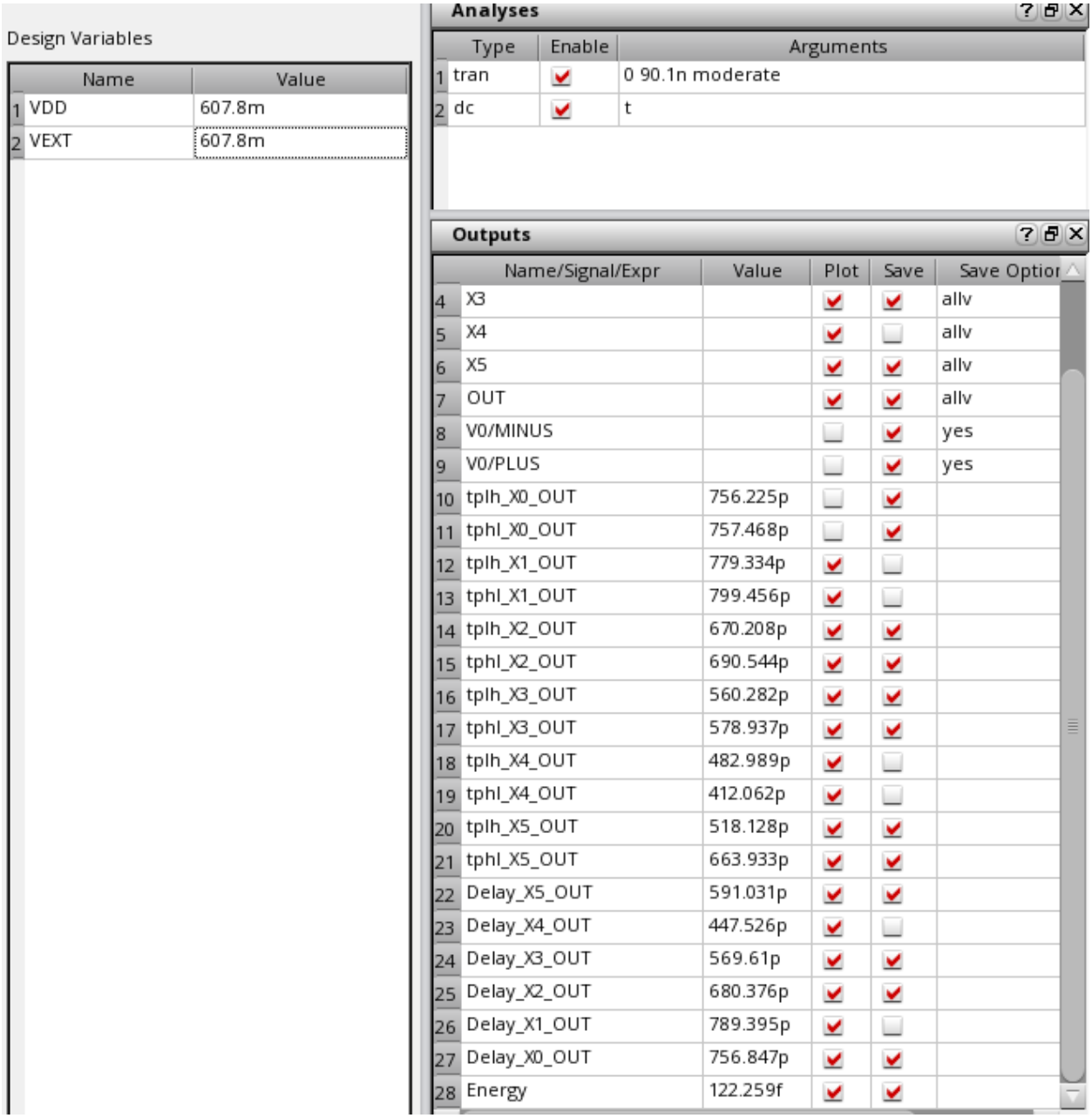
Screenshots Pre-Layout



Design Variables

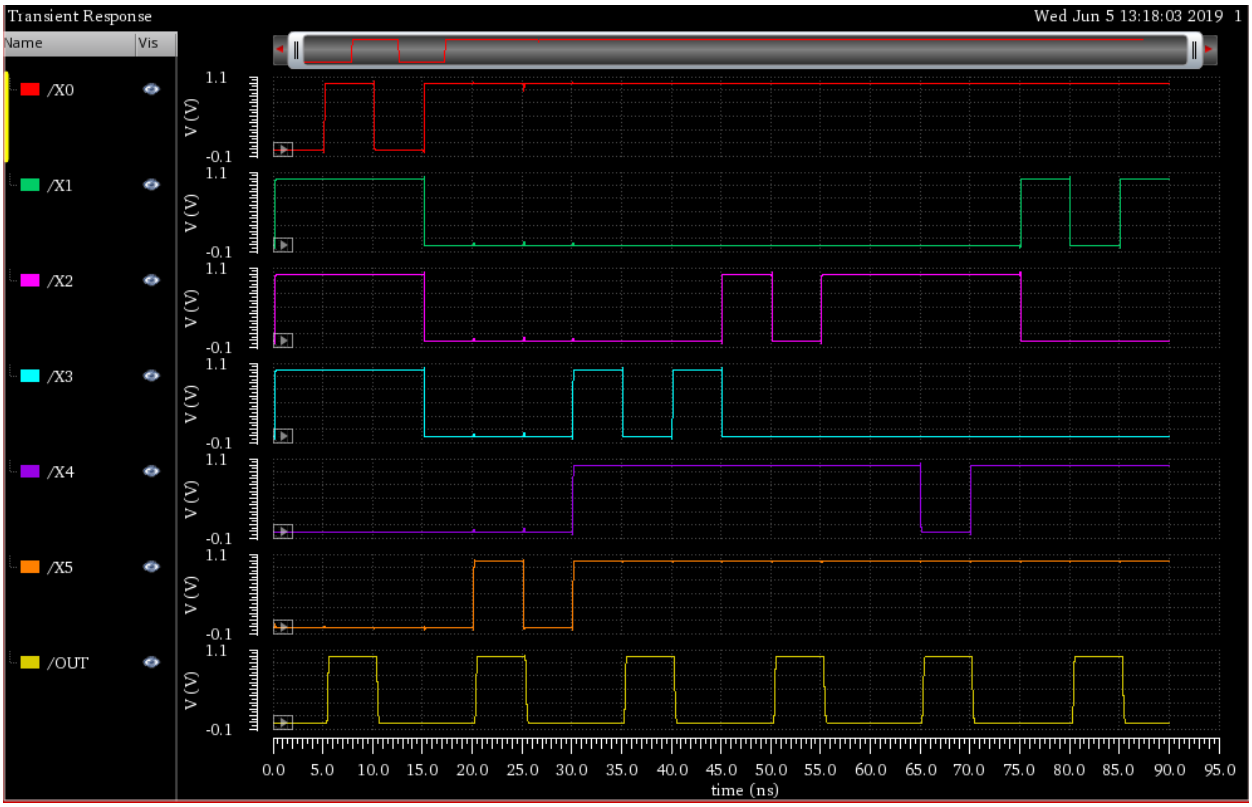
	Name	Value
1	VDD	607.8m
2	VEXT	607.8m

Analyses

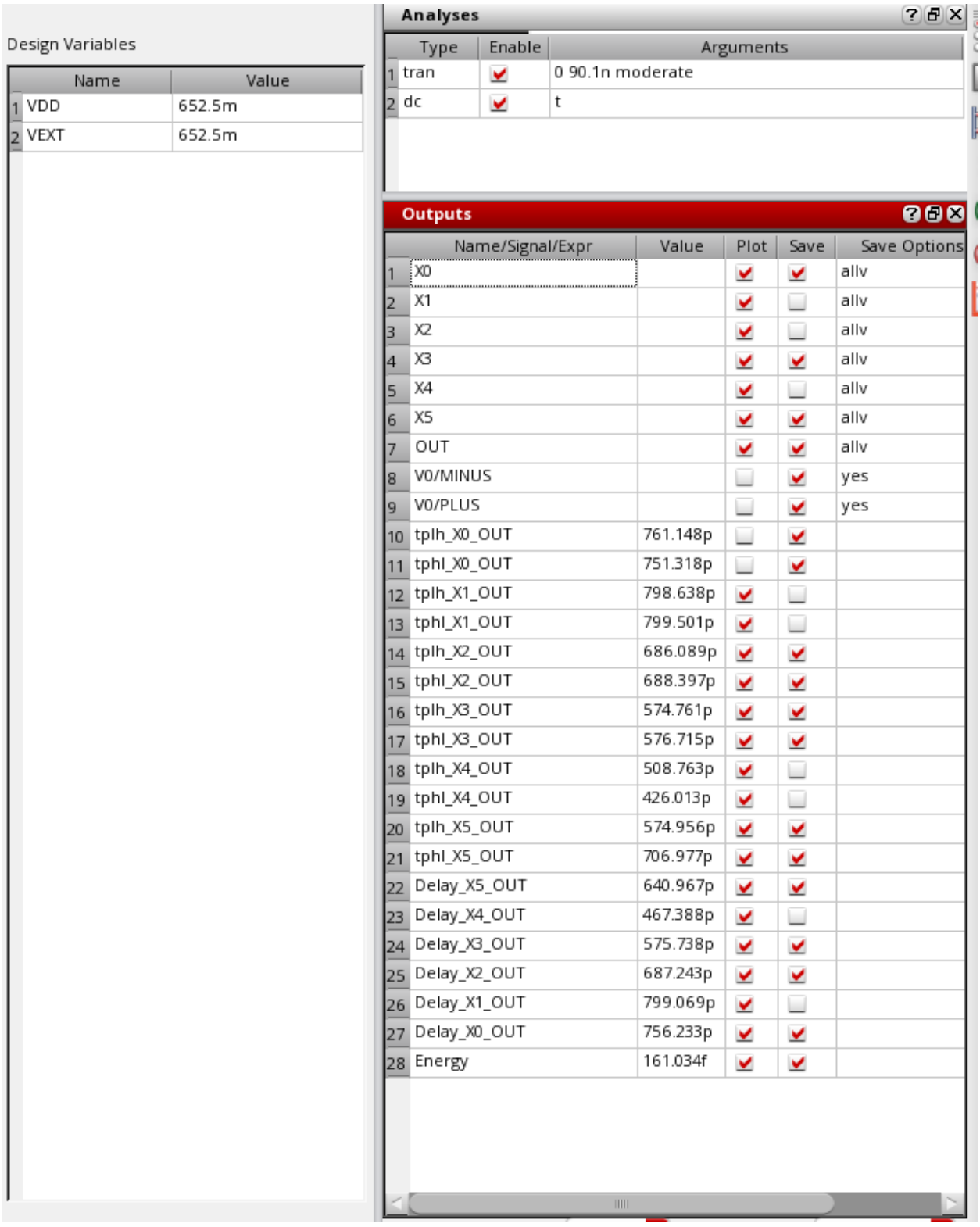
	Type	Enable	Arguments
1	tran	☑	0 90.1n moderate
2	dc	☑	t

Outputs

	Name/Signal/Expr	Value	Plot	Save	Save Optio
4	X3		☑	☑	allv
5	X4		☑	☐	allv
6	X5		☑	☑	allv
7	OUT		☑	☑	allv
8	V0/MINUS		☐	☑	yes
9	V0/PLUS		☐	☑	yes
10	tplh_X0_OUT	756.225p	☐	☑	
11	tphl_X0_OUT	757.468p	☐	☑	
12	tplh_X1_OUT	779.334p	☑	☐	
13	tphl_X1_OUT	799.456p	☑	☐	
14	tplh_X2_OUT	670.208p	☑	☑	
15	tphl_X2_OUT	690.544p	☑	☑	
16	tplh_X3_OUT	560.282p	☑	☑	
17	tphl_X3_OUT	578.937p	☑	☑	
18	tplh_X4_OUT	482.989p	☑	☐	
19	tphl_X4_OUT	412.062p	☑	☐	
20	tplh_X5_OUT	518.128p	☑	☑	
21	tphl_X5_OUT	663.933p	☑	☑	
22	Delay_X5_OUT	591.031p	☑	☑	
23	Delay_X4_OUT	447.526p	☑	☐	
24	Delay_X3_OUT	569.61p	☑	☑	
25	Delay_X2_OUT	680.376p	☑	☑	
26	Delay_X1_OUT	789.395p	☑	☐	
27	Delay_X0_OUT	756.847p	☑	☑	
28	Energy	122.259f	☑	☑	


Transient Response
Wed Jun 5 13:18:03 2019 1
Name
Vis
/X0
/X1
/X2
/X3
/X4
/X5
/OUT
1.1
-0.1
V (V)
0.0 5.0 10.0 15.0 20.0 25.0 30.0 35.0 40.0 45.0 50.0 55.0 60.0 65.0 70.0 75.0 80.0 85.0 90.0 95.0
time (ns)

Screenshots Post Layout



Design Variables

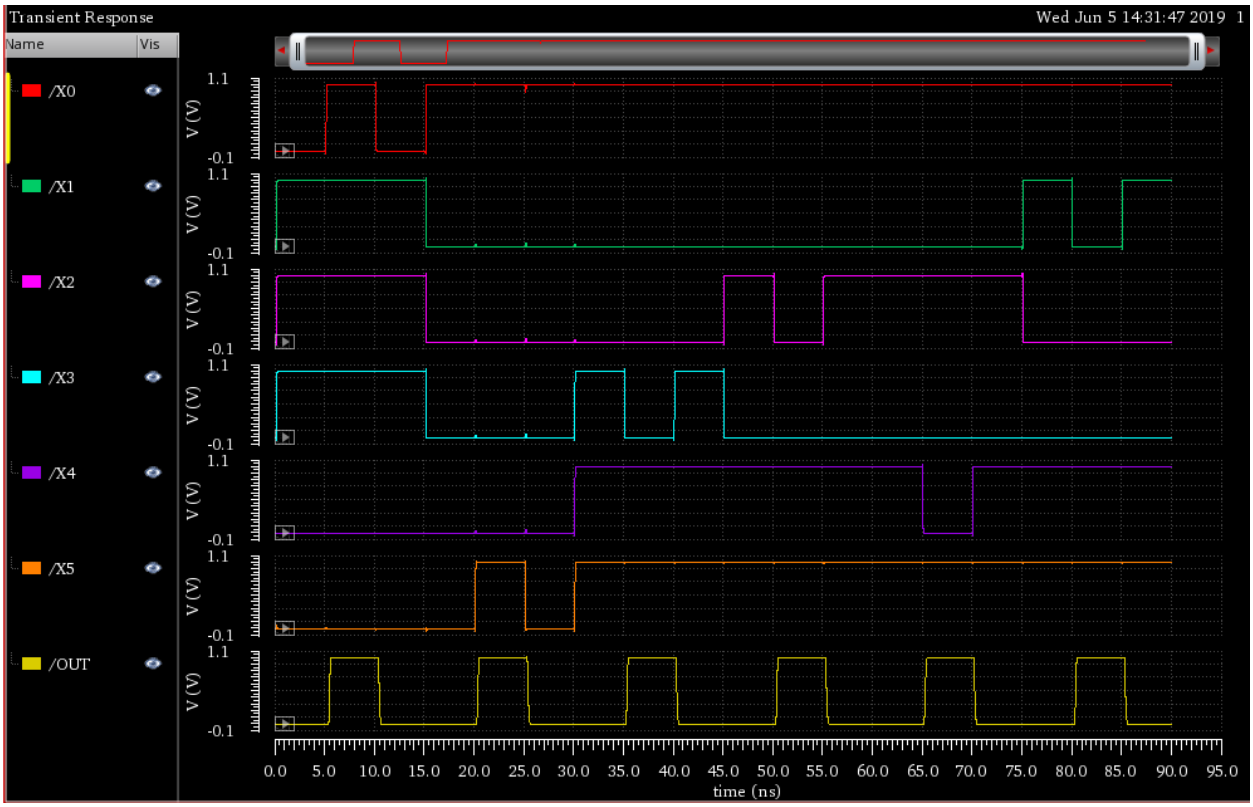
	Name	Value
1	VDD	652.5m
2	VEXT	652.5m

Analyses

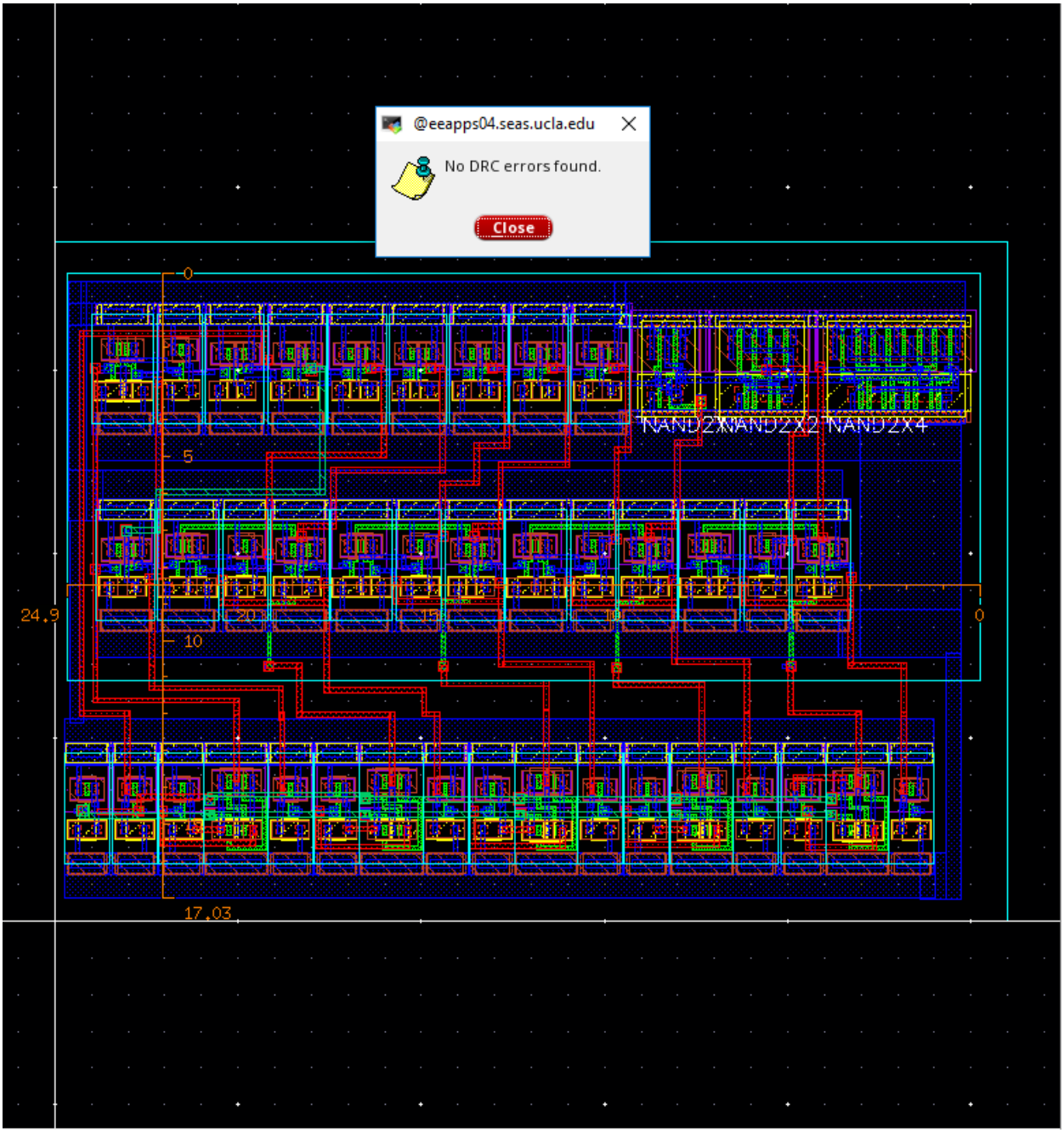
	Type	Enable	Arguments
1	tran	☑	0 90.1n moderate
2	dc	☑	t

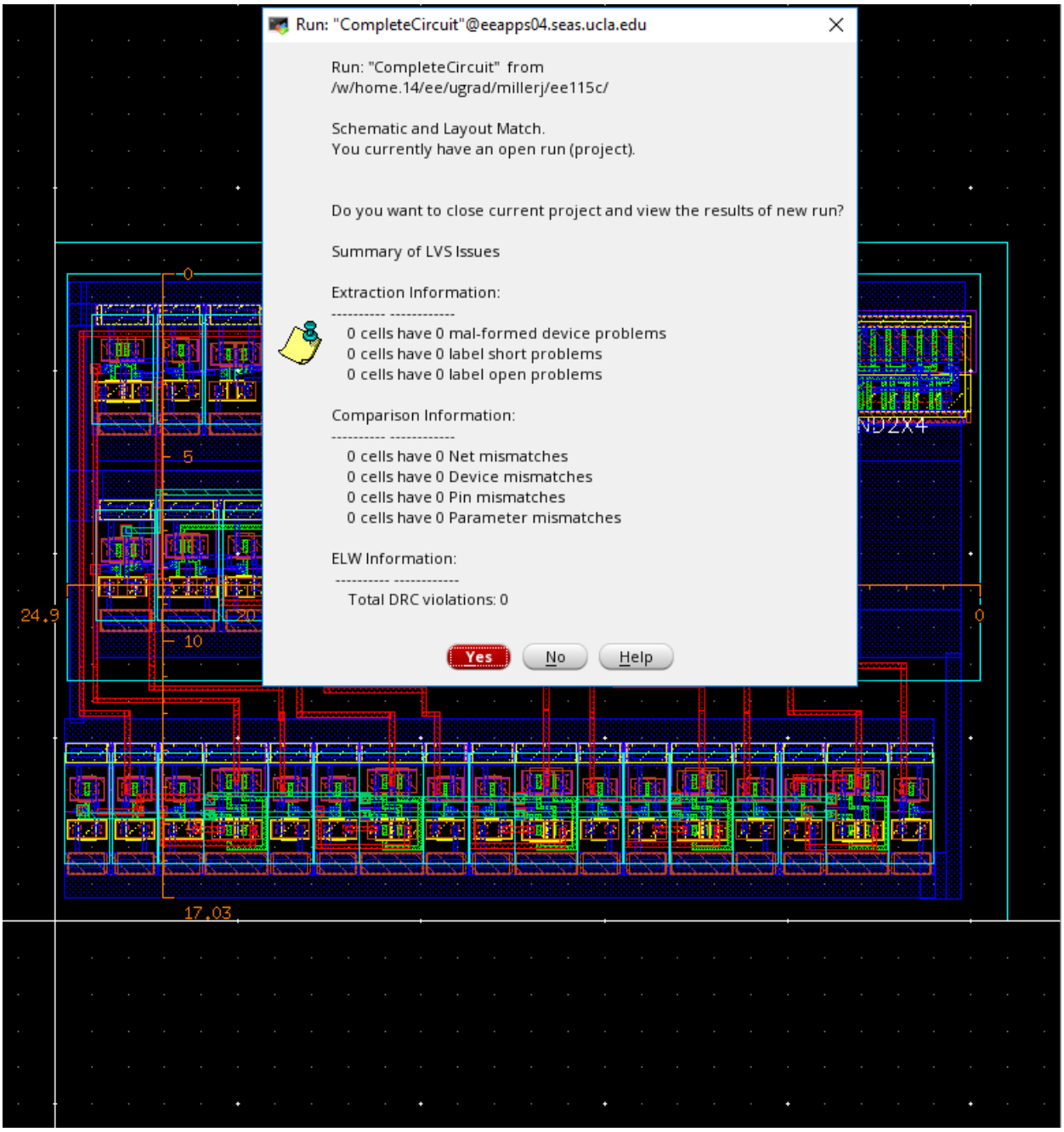
Outputs

	Name/Signal/Expr	Value	Plot	Save	Save Options
1	X0		☑	☑	allv
2	X1		☑	☐	allv
3	X2		☑	☐	allv
4	X3		☑	☑	allv
5	X4		☑	☐	allv
6	X5		☑	☑	allv
7	OUT		☑	☑	allv
8	V0/MINUS		☐	☑	yes
9	V0/PLUS		☐	☑	yes
10	tplh_X0_OUT	761.148p	☐	☑	
11	tphl_X0_OUT	751.318p	☐	☑	
12	tplh_X1_OUT	798.638p	☑	☐	
13	tphl_X1_OUT	799.501p	☑	☐	
14	tplh_X2_OUT	686.089p	☑	☑	
15	tphl_X2_OUT	688.397p	☑	☑	
16	tplh_X3_OUT	574.761p	☑	☑	
17	tphl_X3_OUT	576.715p	☑	☑	
18	tplh_X4_OUT	508.763p	☑	☐	
19	tphl_X4_OUT	426.013p	☑	☐	
20	tplh_X5_OUT	574.956p	☑	☑	
21	tphl_X5_OUT	706.977p	☑	☑	
22	Delay_X5_OUT	640.967p	☑	☑	
23	Delay_X4_OUT	467.388p	☑	☐	
24	Delay_X3_OUT	575.738p	☑	☑	
25	Delay_X2_OUT	687.243p	☑	☑	
26	Delay_X1_OUT	799.069p	☑	☐	
27	Delay_X0_OUT	756.233p	☑	☑	
28	Energy	161.034f	☑	☑	


Transient Response
Wed Jun 5 14:31:47 2019 1
Name
Vis
/X0
/X1
/X2
/X3
/X4
/X5
/OUT
V (V)
1.1
-0.1
0.0 5.0 10.0 15.0 20.0 25.0 30.0 35.0 40.0 45.0 50.0 55.0 60.0 65.0 70.0 75.0 80.0 85.0 90.0 95.0
time (ns)

Layout Verification





Work Division

Alexander:

Built schematic view for AdderModule, Built and tested carry Bypass Adder to compare with CLA, designed layout for PTL Mux half sized NAND, NOR, Inverter, as well as layout for Adder Module.

Joseph:

Designed circuit used for schematic, sized schematic, built schematic view for Inverting Stage, designed layout for Inverting Stage and Abs_Value_Detector.