Hello Shawn Furman,

This is an FPGA project from last fall that had me design a UART based transmitter that sent a simple stream of hex digits encoded with a key using XOR (XORing hexadecimal numbers). This was a long project over 3 weeks and it was completed 1 week ahead of schedule. This was designed with another student who coded the receiver and we needed to meet half way with two devices that work together. At the time Also, my idea to combine 3 states into 1 reduced the number of states from 6 to 4. I saw the fact that we were splitting the states Encrypt data, Load Shift Register, output Start BIT. So, what I did is combine those to 1 single state, this was to save time and make the design more efficient. My professors design did it in 6 which worked but needed more clock cycles to get to the same result. I have included most of the documents that should give you a look into what I did. My code here isn’t commented because at the time it wasn’t push for specific standards. However, this is extremely hit on in HDL which requires proper documentation. However, I have commented the state machine code file “FSM.vhd” to give you an idea of what everything would look like if I had done it right and plus you like finite state machines (Type: Morre).