Jordan Winkler
Computer Architecture
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hw7

1) Do Exercise B.2 on page B-80 of the textbook.

Prove that the two equations for E in the example starting on page B-7 are equivalent by using DeMorgan's theorems and the axioms shown on page B-7.

$E_1 = (AB + AC + BC)(ABC)'$
$E_2 = ABC' + ACB' + BCA'$

$$\begin{aligned}
E_1 &= (AB + AC + BC)(ABC)' \\
&= (AB + AC + BC)(A' + B' + C') \\
&= ABA' + ACA' + BCA' + ABB' + ACB' + BCB' + ABC' + ACC' + BCC' \\
&= AA'B + AA'C + BCA' + ABB' + ACB' + BB'C + ABC' + ACC' + BCC' \\
&= ACB' + ABC' + BCA' \\
&= E_2
\end{aligned}$$

2) Do Exercise B.5 on page B-80 of the textbook.

Prove that the NOR gate is universal by showing how to build the AND, OR, and NOT functions using a two-input NOR gate.

$A' = (A + A)'$

$AB = (A' + B')' = ((A + A)' + (B + B)')'$

$A + B = (A'B')' = ((A + B)')' = ((A + B)' + (A + B)')'$

3) User perfect induction to prove or disprove $(A)(A' + B) = AB$

A	B	A'+B	A(A'+B)	AB
0	0	1	0	0
0	1	1	0	0
1	0	0	0	0
1	1	1	1	1

So $(A)(A' + B) <-> AB$ is always 1, or in other words is a tautology.

4) Draw the truth table and the logic circuit for the following function $F = (A + B) \cdot (A' + C')$

(Note, for the logic circuit part, you could draw it by hand) For the truth table, have Separate columns for ALL intermediate steps.

A	B	C	A'	C'	A+B	A'+C'	(A+B)(A'+C')
0	0	0	1	1	0	1	0
0	0	1	1	0	0	1	0
0	1	0	1	1	1	1	1
0	1	1	1	0	1	1	1
1	0	0	0	1	1	1	1
1	0	1	0	0	1	0	0
1	1	0	0	1	1	1	1
1	1	1	0	0	1	0	0

In scheme

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(define (F A B C)
    (and (or A B)
         (or (not A) (not C))))
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5) Do Exercise B.11 on page B-81 of the textbook.

Assume that X consists of 3 bits, x2 x1 x0. Write four logic functions that are true if and only if
X contains only one 0

$x_1'x_2x_3 + x_1x_2'x_3 + x_1x_2x_3'$

X contains an even number of 0s

$x_1'x_2'x_3 + x_1'x_2x_3' + x_1x_2'x_3'$

X when interpreted as an unsigned binary number is less than 4

x_1'

X when interpreted as a signed (two's complement) number is negative

x_1

And to double check

x1	x2	x3	1 zero	2 zeroes	0xx	1xx
0	0	0	0	0	1	0
0	0	1	0	1	1	0
0	1	0	0	1	1	0
0	1	1	1	0	1	0
1	0	0	0	1	0	1
1	0	1	1	0	0	1
1	1	0	1	0	0	1
1	1	1	0	0	0	1

6) Do Exercise B.14 on page B-81 of the textbook.

Implement a switching network that has two data inputs (A and B), two data outputs (C and D), and a control input (S). If S equals 1, the network is in pass-through mode, and C should equal A, and D should equal B. If S equals 0, the network is in crossing mode, and C should equal B, and D should equal A.