TODO: Tidy up Ctrl Word Z register X register ◇BUS\_0 ◇BUS\_1 ◇BUS\_2 ◇BUS\_3 ◇BUS\_4 ◇BUS\_5 ◇BUS\_5 BUS\_0C BUS\_1C BUS\_3C BUS\_5C BUS\_5C BUS\_5C <u>XI</u>C ⊃ZI CLK< DCLK File: x-register.kicad\_sch File: Z register.kicad\_sch Y register ◆BUS\_0 ◆BUS\_1 ◆BUS\_2 ◆BUS\_3 ◆BUS\_3 ◆BUS\_4 ◆BUS\_5 ◆BUS\_5 ◆BUS\_7 CLKD CLKD DHLT <u>∀I</u> YO built File: clock.kicad\_sch MAR → MILb → MIhb upgrade DCLK DCLR ⊳MO - MO - ABUS - 00 - ABUS - 01 - ABUS - 02 - ABUS - 03 - ABUS - 05 - ABUS - 10 - ABUS - 12 - ABUS - 14 - ABUS - 15 -File: y-register.kicad\_sch A register - → BUS\_0 - → BUS\_1 - → BUS\_2 - → BUS\_3 - → BUS\_4 - → BUS\_6 - → BUS\_7 AIC-ALU DA\_0 DA\_1 DA\_2 DA\_3 DA\_4 DA\_5 DA\_6 DA\_7 CLKC-CLRC--DCLK -DCLR CLKC <u>FI</u>< Σ0< Σ\_0< Σ\_1< CLR File: a-register.kicad\_sch File: mar.kicad\_sch RAM Σ\_2< →<u>Rī</u> →RO upgrade B register BUS\_0 ♦
BUS\_1 ♦
BUS\_3 ♦
BUS\_5 ♦
BUS\_5 ♦
BUS\_5 ♦
BUS\_7 ♦ ◇BUS\_0 ◇BUS\_1 ◇BUS\_2 ◇BUS\_3 ◇BUS\_4 ◇BUS\_5 ◇BUS\_6 ◇BUS\_6 DCLK DCLR BIC BOC File: alu.kicad\_sch File: b-register.kicad\_sch Instruction register File: ram.kicad\_sch ◇BUS\_0 built ◇BUS\_1 ◇BUS\_2 ◇BUS\_3 ◇BUS\_4 ◇BUS\_5 ◇BUS\_5 ◇BUS\_6 ◇BUS\_7 BUS\_0 \\
BUS\_1 \\
BUS\_2 \\
BUS\_3 \\
BUS\_5 \\
BUS\_5 \\
BUS\_6 \\
BUS\_7 \\ 100 -DCLK -DCLR CLRD OVRDD File: inst-register.kicad\_ Control logic File: control.kicad\_sch CLR ♦<u>RI</u> ♦RO OVRD CLK File: IO.kicad\_sch Sheet: / File: 8bit—computer.kicad\_sch Title: Size: A3 Rev: KiCad E.D.A. kicad (6.0.8) ld: 1/13























