TODO: BOM Z register X register → BUS_0 → BUS_1 → BUS_2 → BUS_3 → BUS_4 → BUS_5 → BUS_5 BUS_0C BUS_1C BUS_3C BUS_3C BUS_5C BUS_5C <u>XI</u>C DΖΙ CLK< DCLK File: x-register.kicad_sch File: Z register.kicad_sch Y register CLKD CLKD ->BUS_0 ->BUS_1 ->BUS_2 ->BUS_3 ->BUS_4 ->BUS_5 ->BUS_6 ->BUS_7 DHLT YIC YOC built File: clock.kicad_sch MAR → MILb → MIhb upgrade DCLK ⊳MO - MO - ABUS - 00 - ABUS - 01 - ABUS - 02 - ABUS - 03 - ABUS - 05 - ABUS - 10 - ABUS - 12 - ABUS - 15 --DCLR File: y-register.kicad_sch A register - → BUS_0 - → BUS_1 - → BUS_2 - → BUS_3 - → BUS_4 - → BUS_6 - → BUS_7 AIC-ALU A 0 A 1 A 2 A 3 A 4 A 5 A 6 A 7 CLKC CLRC -DCLK -DCLR <u>FI</u>< Σ0< Σ_0< Σ_1< CLR File: mar.kicad_sch RAM File: a-register.kicad_sch Σ_2< →RO upgrade B register BUS_0 ♦
BUS_1 ♦
BUS_3 ♦
BUS_5 ♦
BUS_5 ♦
BUS_5 ♦
BUS_7 ♦ ◇BUS_0 ◇BUS_1 ◇BUS_2 ◇BUS_3 ◇BUS_4 ◇BUS_5 ◇BUS_6 ◇BUS_6 DCLK DCLR BIC BOC File: alu.kicad_sch File: b-register.kicad_sch Instruction register File: ram.kicad_sch ◇BUS_0 built ◇BUS_1 ◇BUS_2 ◇BUS_3 ◇BUS_4 ◇BUS_5 ◇BUS_5 ◇BUS_6 ◇BUS_7 BUS_0 ♦
BUS_1 ♦
BUS_2 ♦
BUS_3 ♦
BUS_5 ♦
BUS_5 ♦
BUS_6 ♦ 100 -DCLK -DCLR CLRD OVRDD File: inst-register.kicad_ Control logic File: control.kicad_sch CLR NON ♦<u>RI</u> ♦RO OVRD CLK ⇔HLT File: IO.kicad_sch Sheet: / File: 8bit—computer.kicad_sch Title: Size: A3 Rev: KiCad E.D.A. kicad (6.0.8) ld: 1/13























