Assignment 3

1. Clock Divider

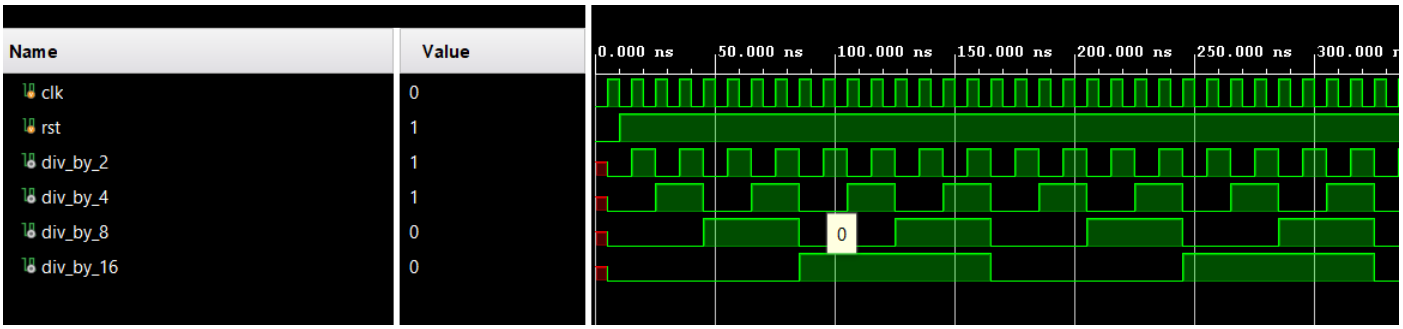
Verilog code:

```
module clock_divider(
    input rst,
    input   clk,

   output reg div_by_2,div_by_4,div_by_8,div_by_16

    );
     reg  [3:0]count;
    always @ (posedge clk)

    begin
    if(rst==0)
    count=4'b0000;

    else

    count = count + 1;

    div_by_2  = count[0];
    div_by_4  = count[1];
    div_by_8  = count[2];
    div_by_16 = count[3];


end

endmodule
```

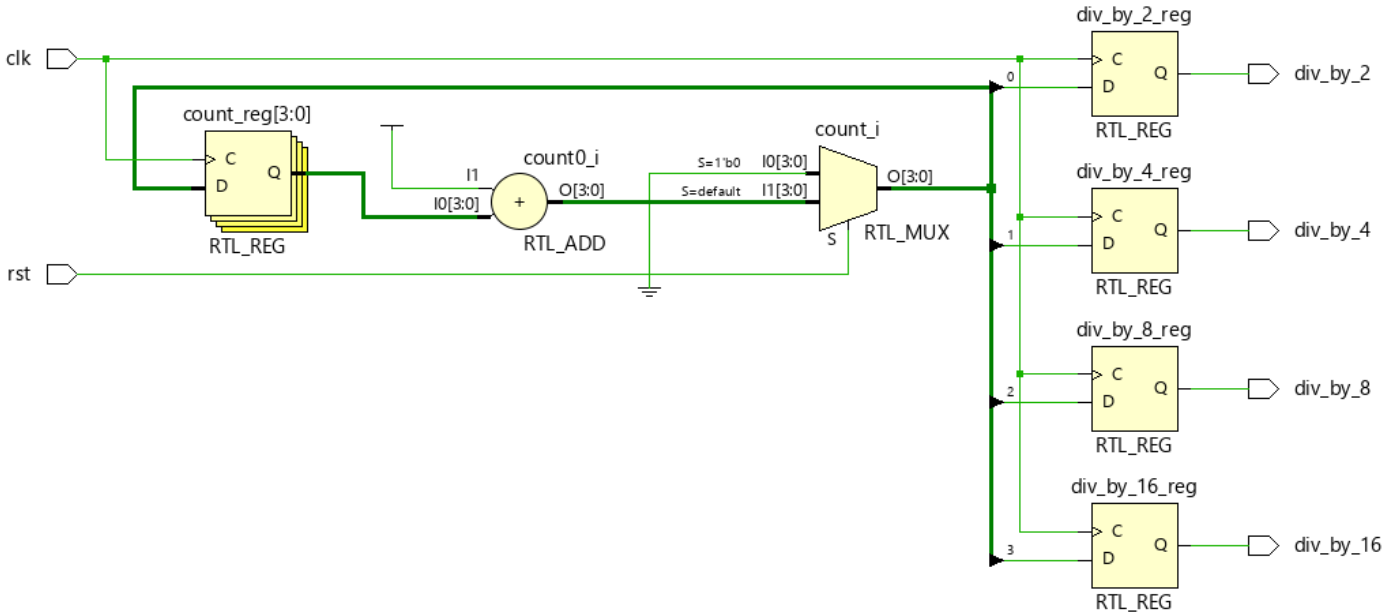
Testbench:

```
module clock_divider_tb(

    );
    reg clk;
    reg rst;
    wire div_by_2,div_by_4,div_by_8,div_by_16;


    clock_divider uut(rst,clk,div_by_2,div_by_4,div_by_8,div_by_16);
    initial     clk = 1'b0;
        always #5 clk = ~clk;

   initial begin : test

            rst = 1'b0;
            #10
            rst = 1'b1;

            #60000
            $finish;

        end


endmodule
```

Simulation:



Schematic:



Synthesis report:

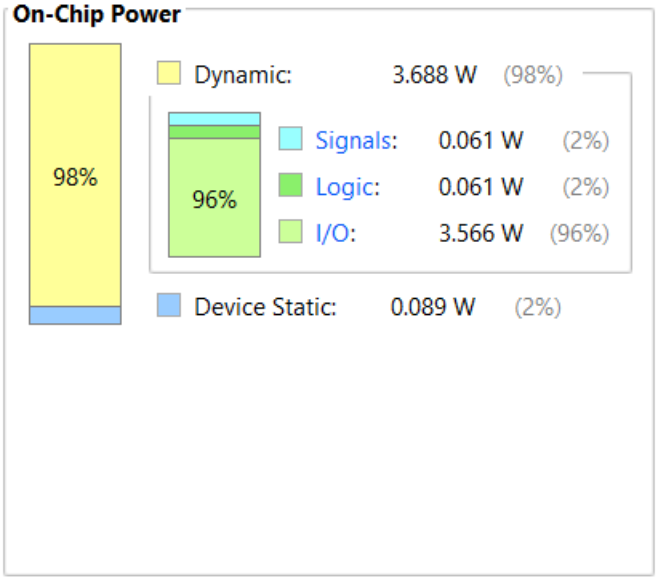
```
Start Writing Synthesis Report
-------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |BUFG |     1|
|2     |LUT1 |     2|
|3     |LUT2 |     1|
|4     |LUT3 |     1|
|5     |LUT4 |     1|
|6     |FDRE |     4|
|7     |IBUF |     2|
|8     |OBUF |     4|
+------+-----+------+

Report Instance Areas:
+------+---------+-------+------+
|      |Instance |Module |Cells |
+------+---------+-------+------+
|1     |top      |       |    16|
+------+---------+-------+------+
-------------------------------------
Finished Writing Synthesis Report : 
```

Power report:

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**3.777 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**32.1°C**
Thermal Margin:	52.9°C (27.9 W)
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



2. Johnson Counter

Verilog code:

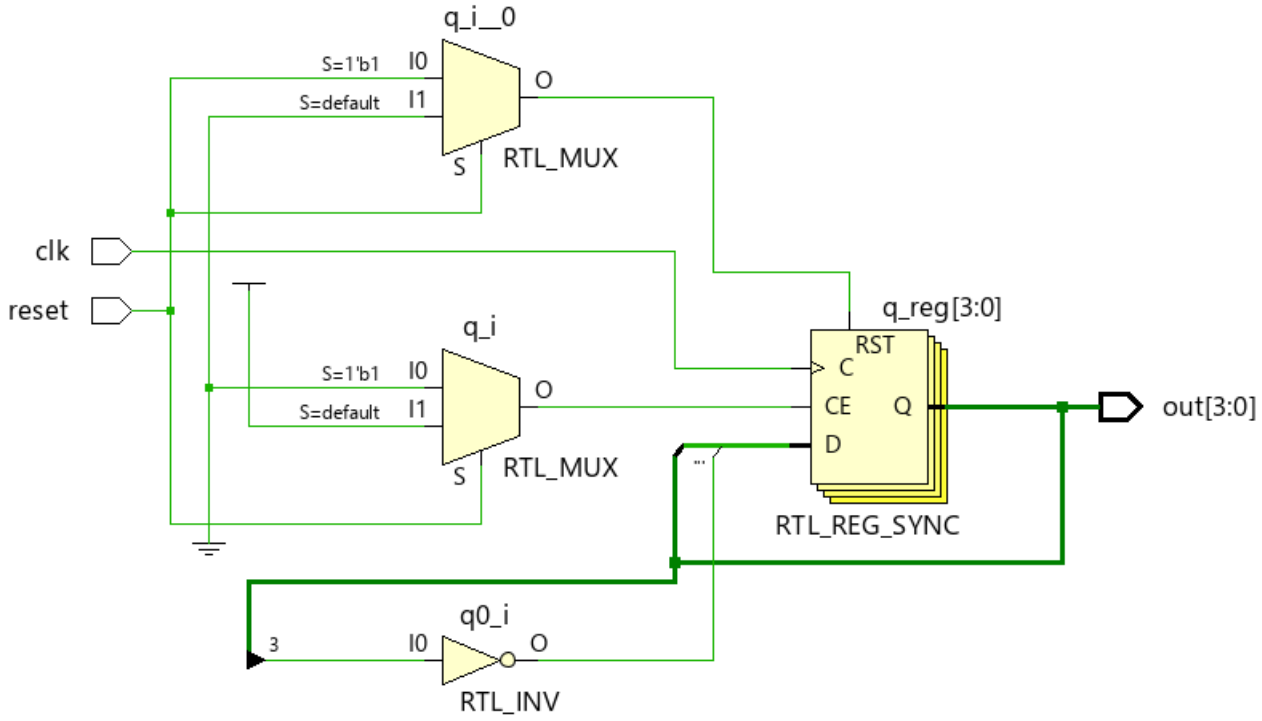
```
module johnson_counter( out,reset,clk);
input clk,reset;
output [3:0] out;

reg [3:0] q;

always @(posedge clk)
begin

if(reset)
 q=4'd0;
 else
    begin
        q[3]<=q[2];
        q[2]<=q[1];
        q[1]<=q[0];
        q[0]<=(~q[3]);
    end
 end

assign out=q;
endmodule
```

Testbench:

```
module jc_tb;
  reg clk,reset;
  wire [3:0] out;

  johnson_counter dut (.out(out), .reset(reset), .clk(clk));

  always
    #5 clk =~clk;

  initial begin
    reset=1'b1; clk=1'b0;
   #20 reset= 1'b0;
  end

  initial
    begin
     $monitor( $time, " clk=%b, out= %b, reset=%b", clk,out,reset);
     #105  $stop;
   end

endmodule
```

Simulation:

Schematic:



Synthesis report:

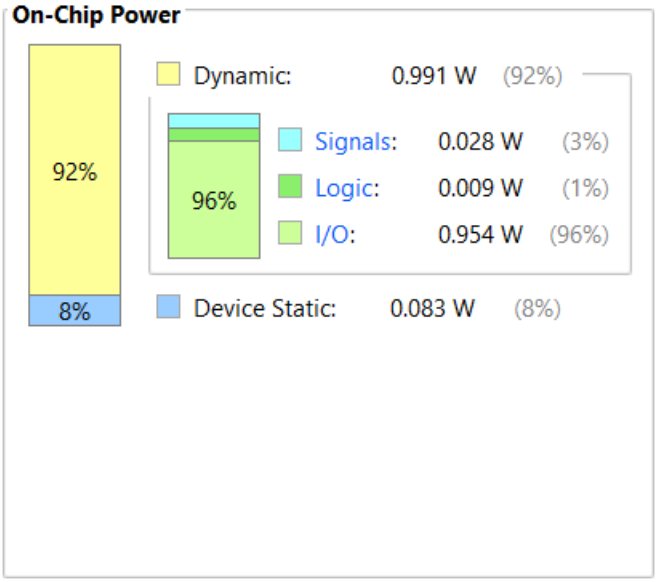
```
Start Writing Synthesis Report
-----------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |BUFG |     1|
|2     |LUT1 |     1|
|3     |FDRE |     4|
|4     |IBUF |     2|
|5     |OBUF |     4|
+------+-----+------+

Report Instance Areas:
+------+---------+-------+------+
|      |Instance |Module |Cells |
+------+---------+-------+------+
|1     |top      |       |    12|
+------+---------+-------+------+
-----------------------------------
Finished Writing Synthesis Report :
```

Power report:

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**1.074 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**27.0°C**
Thermal Margin:	58.0°C (30.6 W)
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



3. Ring Counter

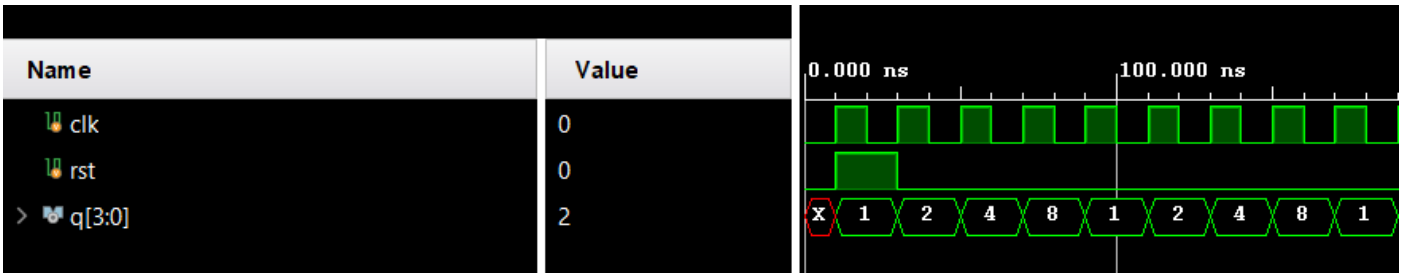
Verilog code:

```
module ring_counter(
    input clk,
    input rst,
    output reg [3:0] q
    );

     always @(posedge clk)
     begin
          if(rst==1)

              q <= 4'b0001;

           else
               begin
                   q[0]<=q[3];
                   q[1]<=q[0];
                   q[2]<=q[1];
                   q[3]<=q[2];
               end
    end
endmodule
```

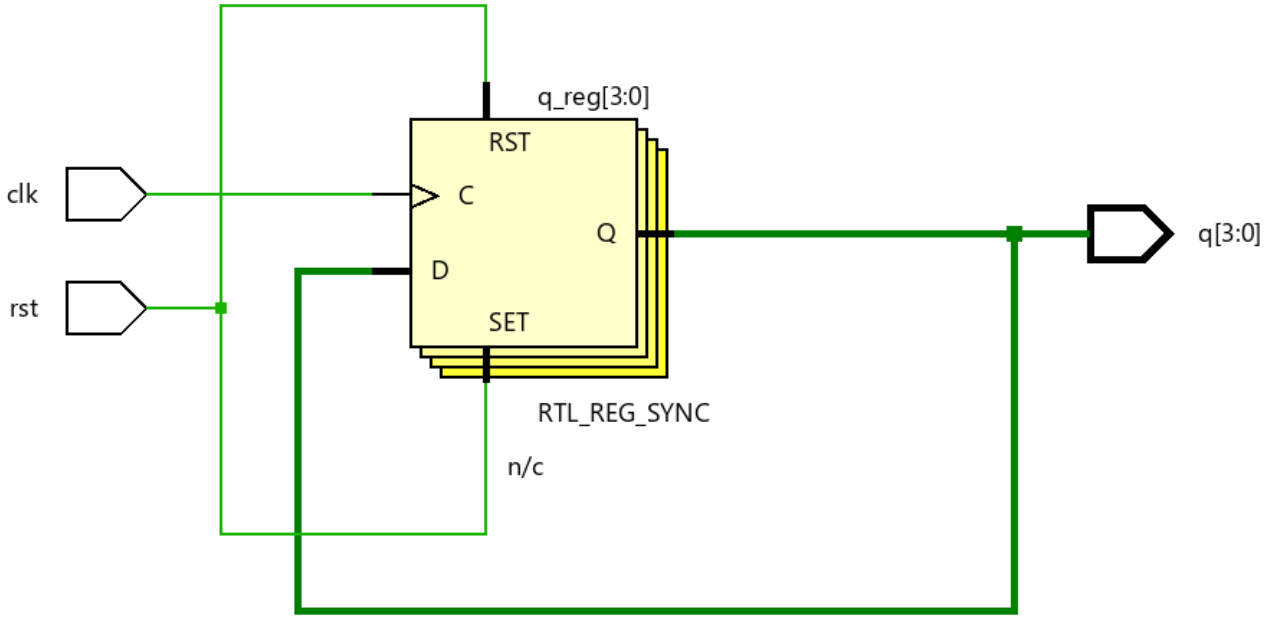
Testbench:

```
module ring_counter_tb(

    );

    reg clk;
    reg rst;
    wire [3:0]q;

    ring_counter uut(clk,rst,q);

    initial begin
    #0 clk=1'b0;
    #0 rst = 1'b0;
    end

    always
    #10 clk = ~clk;
    initial
    begin
     #10 rst =1'b1;
     #20 rst =1'b0;
     #500 $finish;
     end


endmodule
```

Simulation:



Schematic:



Synthesis report:

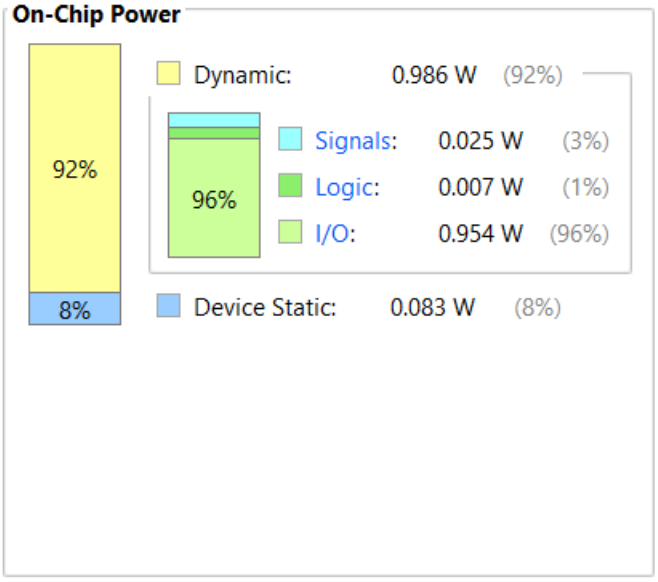
```
Start Writing Synthesis Report
---------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |BUFG |     1|
|2     |FDRE |     3|
|3     |FDSE |     1|
|4     |IBUF |     2|
|5     |OBUF |     4|
+------+-----+------+

Report Instance Areas:
+------+---------+-------+------+
|      |Instance |Module |Cells |
+------+---------+-------+------+
|1     |top      |       |    11|
+------+---------+-------+------+
---------------------------------
Finished Writing Synthesis Report
```

Power report:

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**1.069 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**27.0°C**
Thermal Margin:	58.0°C (30.6 W)
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



4. 5 Input Majority circuit

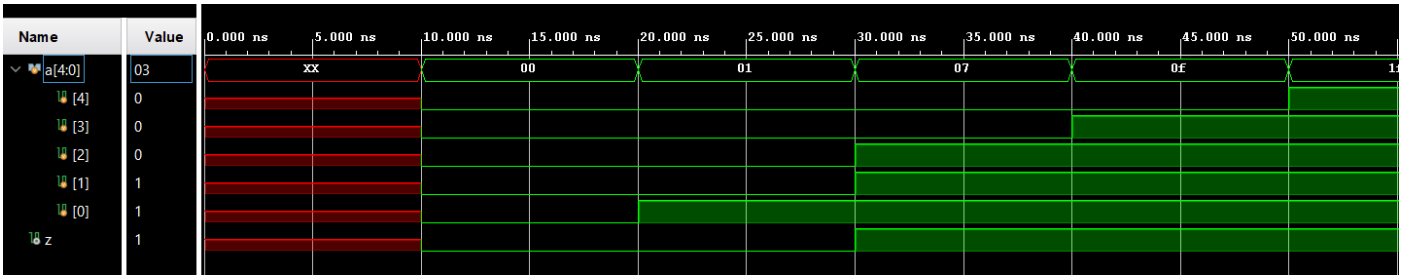
Verilog code:

```
module majority_of_five(input [4:0] sw, output led);

assign led =    (sw[0] & sw[1] & sw[2]) |
        (sw[0] & sw[1] & sw[3]) |
        (sw[0] & sw[1] & sw[4]) |
        (sw[0] & sw[2] & sw[3]) |
        (sw[0] & sw[2] & sw[4]) |
        (sw[0] & sw[3] & sw[4]) |
        (sw[1] & sw[2] & sw[3]) |
        (sw[1] & sw[2] & sw[4]) |
        (sw[1] & sw[3] & sw[4]) |
        (sw[2] & sw[3] & sw[4]);
endmodule
```

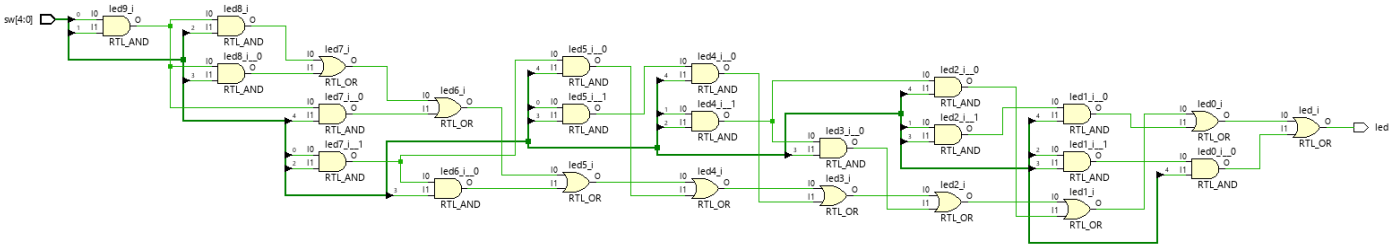
Testbench:

```
module majority_of_five_tb;

reg [4:0] sw;
wire led;

majority_of_five cut (.sw(sw),.led(led));

integer k;

initial
begin
    sw = 0;

    for (k=0; k<32; k=k+1)
        #20 sw = k;

    #20 $finish;
end
endmodule
```

Simulation:



Schematic:



Synthesis report:

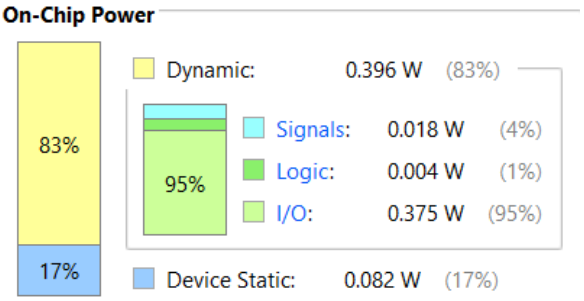
```
Start Writing Synthesis Report
-----------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |LUT5 |     1|
|2     |IBUF |     5|
|3     |OBUF |     1|
+------+-----+------+

Report Instance Areas:
+------+---------+-------+------+
|      |Instance |Module |Cells |
+------+---------+-------+------+
|1     |top      |       |     7|
+------+---------+-------+------+
-----------------------------------
Finished Writing Synthesis Report
```

Power report:

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**0.478 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**25.9°C**
Thermal Margin:	59.1°C (31.2 W)
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



5. Parity Generator

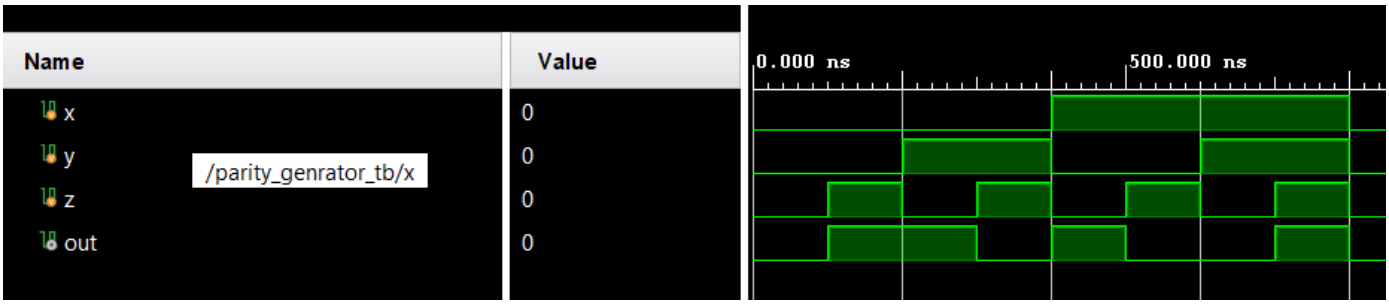
Verilog code:

```
module parity_genrator(
    input x,
    input y,
    input z,
    output out
    );

    xor (out,x,y,z);

endmodule
```

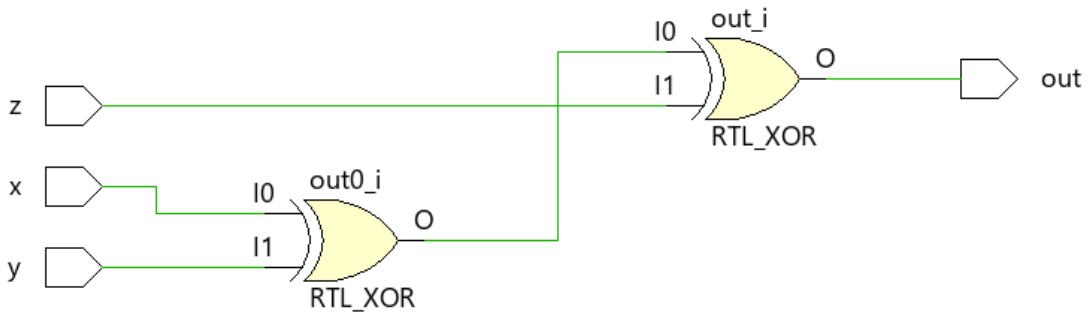
Testbench:

```
module parity_genrator_tb(

    );
    reg x,y,z;
    wire out;

    parity_genrator uut(x,y,z,out);

    initial
    begin

    #00  x=0 ; y=0 ; z=0;
    #100 x=0 ; y=0 ; z=1;
    #100 x=0 ; y=1 ; z=0;
    #100 x=0 ; y=1 ; z=1;
    #100 x=1 ; y=0 ; z=0;
    #100 x=1 ; y=0 ; z=1;
    #100 x=1 ; y=1 ; z=0;
    #100 x=1 ; y=1 ; z=1;
    #100 x=0 ; y=0 ; z=0;
    end

    initial begin

       $dumpfile("dump.vcd");
       $dumpvars(0);

    end
endmodule
```

Simulation:



Schematic:



Synthesis report:

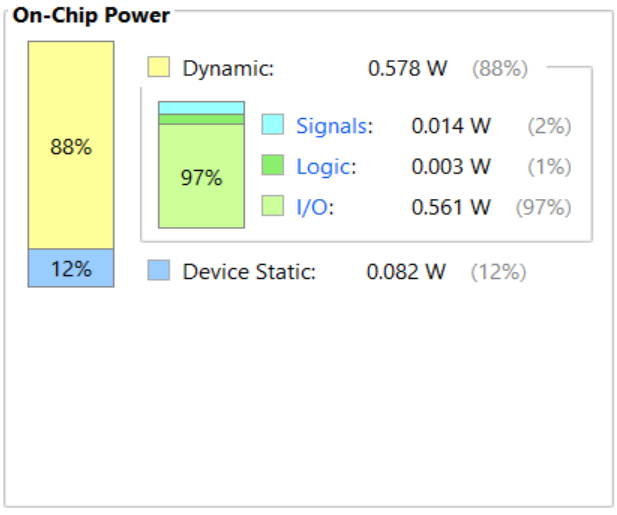
```
Start Writing Synthesis Report
-------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |LUT3 |     1|
|2     |IBUF |     3|
|3     |OBUF |     1|
+------+-----+------+

Report Instance Areas:
+------+---------+-------+------+
|      |Instance |Module |Cells |
+------+---------+-------+------+
|1     |top      |       |     5|
+------+---------+-------+------+
-------------------------------
Finished Writing Synthesis Report
```

Power report:

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**0.661 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**26.2°C**
Thermal Margin:	58.8°C (31.0 W)
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



6. Binary to one hot encoder

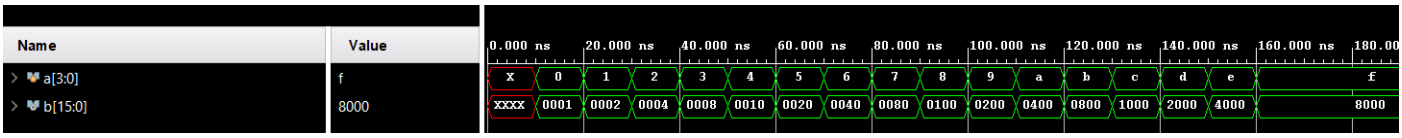
Verilog code:

```
`timescale 1ns / 1ps

module binary_to_one_hot_encoder(
    input [3:0] a,
    output [15:0] b
    );

      assign b = 1'b1 <<a;

endmodule
```

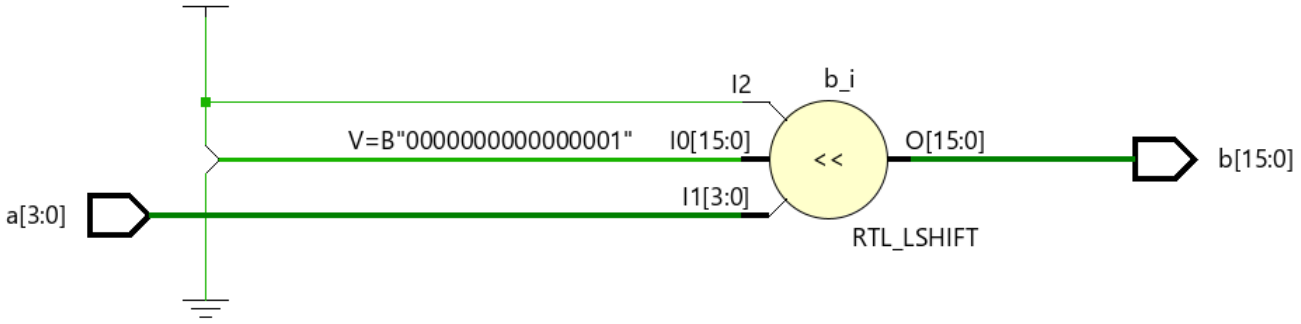
Testbench:

```
`timescale 1ns / 1ps

module binary_to_one_hot_encoder_tb;
    reg [3:0] a;
    wire [15:0] b;

    binary_to_one_hot_encoder uut(a,b);


    initial begin

    #10 a=4'b0000;
    #10 a=4'b0001;
    #10 a=4'b0010;
    #10 a=4'b0011;
    #10 a=4'b0100;
    #10 a=4'b0101;
    #10 a=4'b0110;
    #10 a=4'b0111;
    #10 a=4'b1000;
    #10 a=4'b1001;
    #10 a=4'b1010;
    #10 a=4'b1011;
    #10 a=4'b1100;
    #10 a=4'b1101;
    #10 a=4'b1110;
    #10 a=4'b1111;


    end
     initial begin

       $dumpfile("dump.vcd");
       $dumpvars(0);

     end
endmodule
```

Simulation:



Schematic:



Synthesis report:

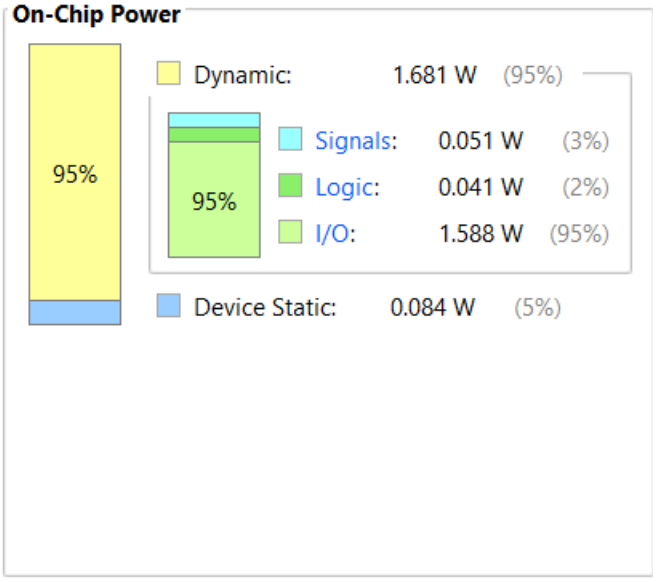
```
Start Writing Synthesis Report
---------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |LUT4 |    16|
|2     |IBUF |     4|
|3     |OBUF |    16|
+------+-----+------+

Report Instance Areas:
+------+---------+-------+------+
|      |Instance |Module |Cells |
+------+---------+-------+------+
|1     |top      |       |    36|
+------+---------+-------+------+
---------------------------------
Finished Writing Synthesis Report
```

Power report:

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**1.765 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**28.3°C**
Thermal Margin:	56.7°C (29.9 W)
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



7. 4-Bit BCD Synchronous Counter

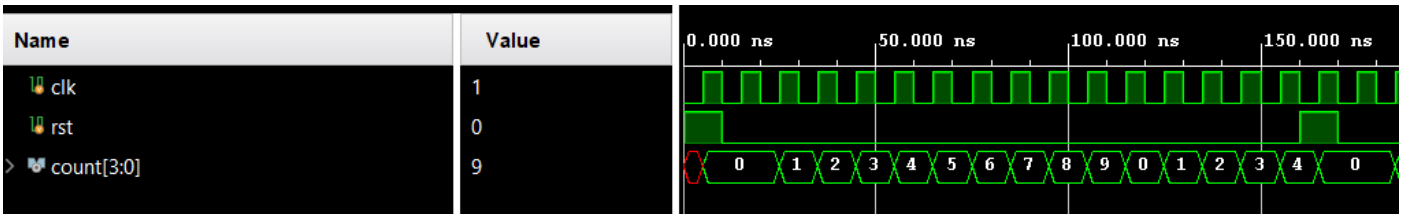
Verilog code:

```
`timescale 1ns / 1ps

module bcd_4_bit_synchronous_counter(
    input clk,
    input rst,
    output reg [3:0] count
    );
    reg [3:0]t;
    always @ (posedge clk)
    begin
      if (rst)
      begin
        t <= 4'b0000;
        count <= 4'b0000;
      end
      else
      begin
        t <= t + 1;
        if (t == 4'b1001)
        begin
          t <= 4'b0000;
        end
        count <= t;
      end
    end

endmodule
```

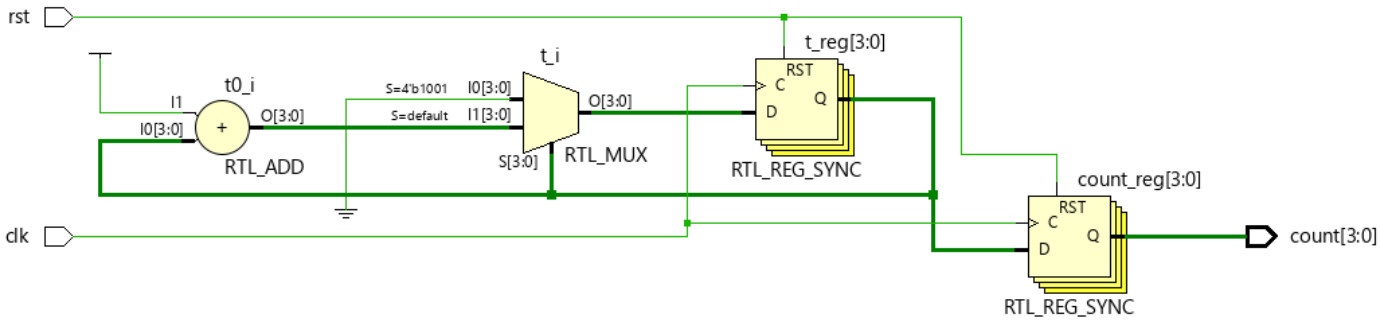
Testbench:

```
`timescale 1ns / 1ps

module bcd_4_bit_synchronous_counter_tb(

    );
    reg clk;
    reg rst;
     wire [3:0]count;

    bcd_4_bit_synchronous_counter uut(clk,rst,count);

     initial begin
       clk = 0;
       forever #5 clk = ~clk;
     end

     initial begin
       rst = 1;
       #10 rst = 0;
        $monitor ("T=%0t out=%b", $time, count);
       #150 rst = 1;
      #10 rst = 0;
      #200
      $finish;
      end

endmodule
```

Simulation:



Schematic:



Synthesis report:

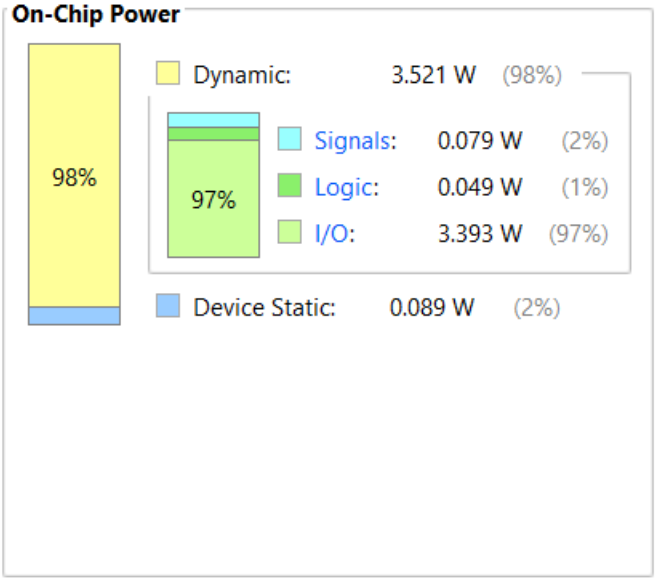
```
Start Writing Synthesis Report
---------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |BUFG |     1|
|2     |LUT1 |     1|
|3     |LUT3 |     1|
|4     |LUT4 |     2|
|5     |FDRE |     8|
|6     |IBUF |     2|
|7     |OBUF |     4|
+------+-----+------+

Report Instance Areas:
+------+---------+-------+------+
|      |Instance |Module |Cells |
+------+---------+-------+------+
|1     |top      |       |    19|
+------+---------+-------+------+
---------------------------------
Finished Writing Synthesis Report
```

Power report:

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**3.609 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**31.8°C**
Thermal Margin:	53.2°C (28.1 W)
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



8. 4-Bit carry lookahead adder

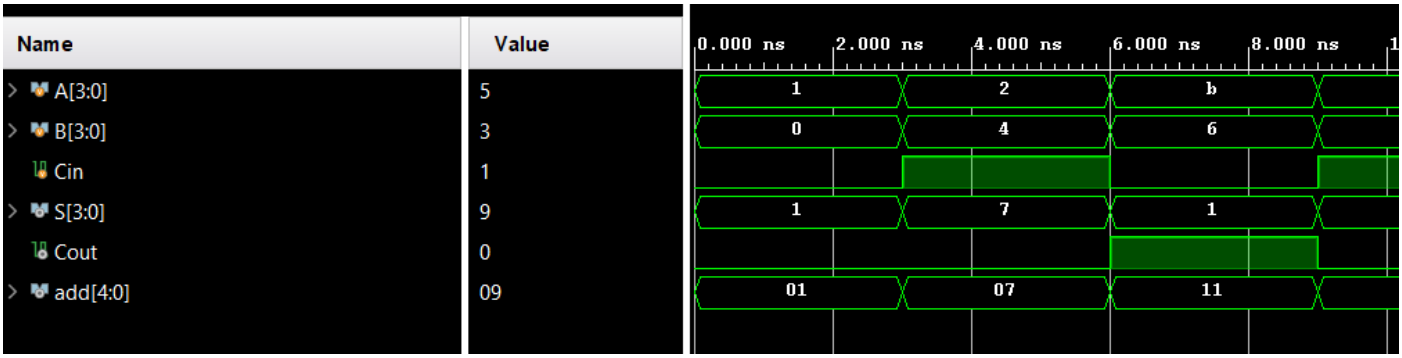
Verilog code:

```
`timescale 1ns / 1ps


module carry_lookahead_adder_4bit(
  input [3:0]A, B,
  input Cin,
  output [3:0] S,
  output Cout
    );
     wire [3:0] Ci;

  assign Ci[0] = Cin;
  assign Ci[1] = (A[0] & B[0]) | ((A[0]^B[0]) & Ci[0]);
  assign Ci[2] = (A[1] & B[1]) | ((A[1]^B[1]) & ((A[0] & B[0]) | ((A[0]^B[0]) & Ci[0])));
  assign Ci[3] = (A[2] & B[2]) | ((A[2]^B[2]) & ((A[1] & B[1]) | ((A[1]^B[1]) & ((A[0] & B[0]) | ((A[0]^B[0]) & Ci[0])))));
  assign Cout  = (A[3] & B[3]) | ((A[3]^B[3]) & ((A[2] & B[2]) | ((A[2]^B[2]) & ((A[1] & B[1]) | ((A[1]^B[1]) & ((A[0] & B[0]) | ((A[0]^B[0]) & Ci[0])))))));

  assign S = A^B^Ci;

endmodule
```

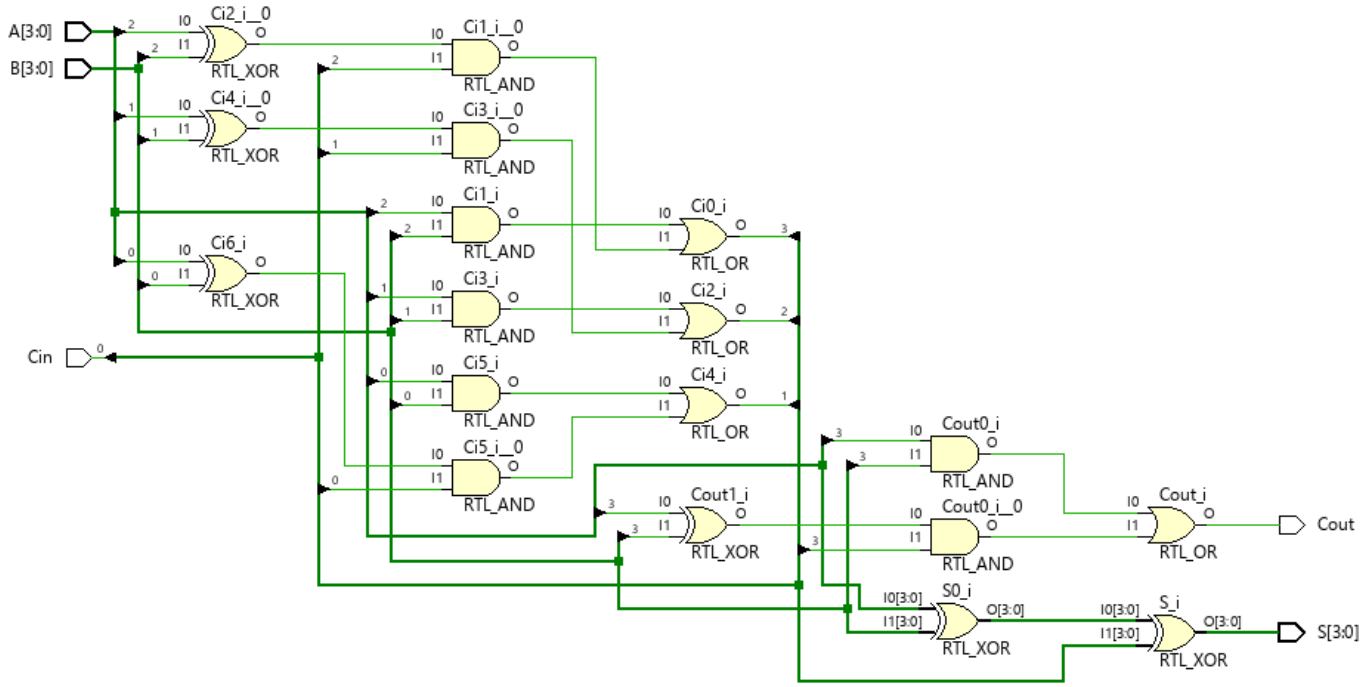
Testbench:

```
`timescale 1ns / 1ps


module carry_lookahead_adder_4bit_tb(

    );
      reg [3:0]A, B;
  reg Cin;
  wire [3:0] S;
  wire Cout;
  wire[4:0] add;

  carry_lookahead_adder_4bit uut(A, B, Cin, S, Cout);

  assign add = {Cout, S};
  initial begin
    $monitor("A = %b: B = %b, Cin = %b --> S = %b, Cout = %b, Addition = %0d", A, B, Cin, S, Cout, add);
    A = 1; B = 0; Cin = 0; #3;
    A = 2; B = 4; Cin = 1; #3;
    A = 4'hb; B = 4'h6; Cin = 0; #3;
    A = 5; B = 3; Cin = 1;
  end
endmodule
```

Simulation:



Schematic:



Synthesis report:

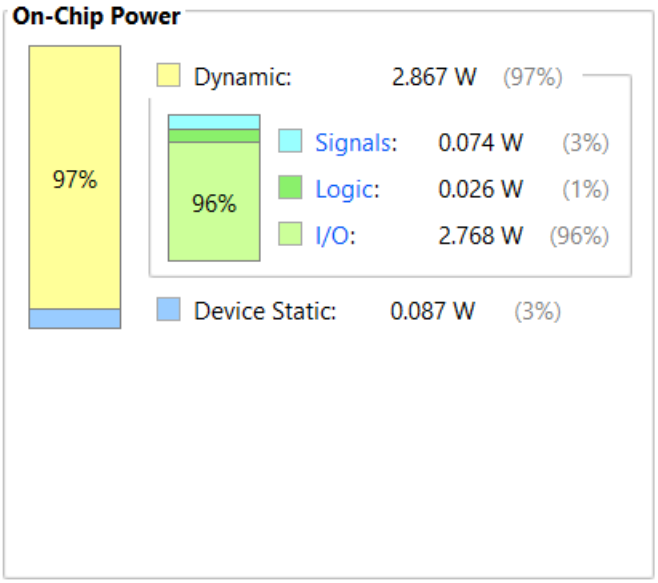
```
Start Writing Synthesis Report
---------------------------------

Report BlackBoxes:
+-+---------------+----------+
| |BlackBox name |Instances |
+-+---------------+----------+
+-+---------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |LUT3 |     2|
|2     |LUT5 |     4|
|3     |IBUF |     9|
|4     |OBUF |     5|
+------+-----+------+

Report Instance Areas:
+------+---------+-------+------+
|      |Instance |Module |Cells |
+------+---------+-------+------+
|1     |top      |       |    20|
+------+---------+-------+------+
---------------------------------
Finished Writing Synthesis Report
```

Power report:

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**2.954 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**30.6°C**
Thermal Margin:	54.4°C (28.7 W)
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



9. N-Bit Comparator

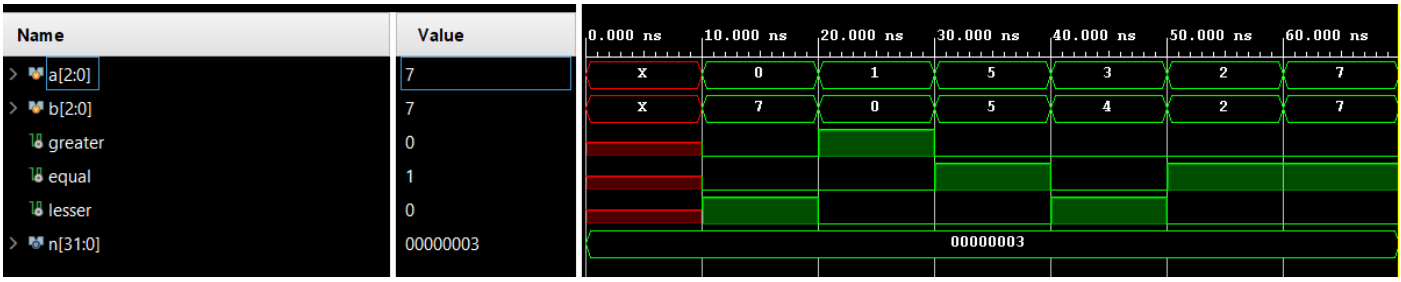
Verilog code:

```
`timescale 1ns / 1ps


module n_bit_comparator(
    input [n-1:0] a,
    input [n-1:0] b,
    output reg greater,
    output reg equal,
    output reg lesser
    );
    parameter n=3 ;
    always @ (a,b)
    begin

    if(a>b)
    begin
    greater = 1;
    equal   = 0;
    lesser  = 0;
    end

    else if(a==b)
        begin
        greater = 0;
        equal   = 1;
        lesser  = 0;
        end
    else if(a<b)
            begin
            greater = 0;
            equal   = 0;
            lesser  = 1;
            end

    end
endmodule
```

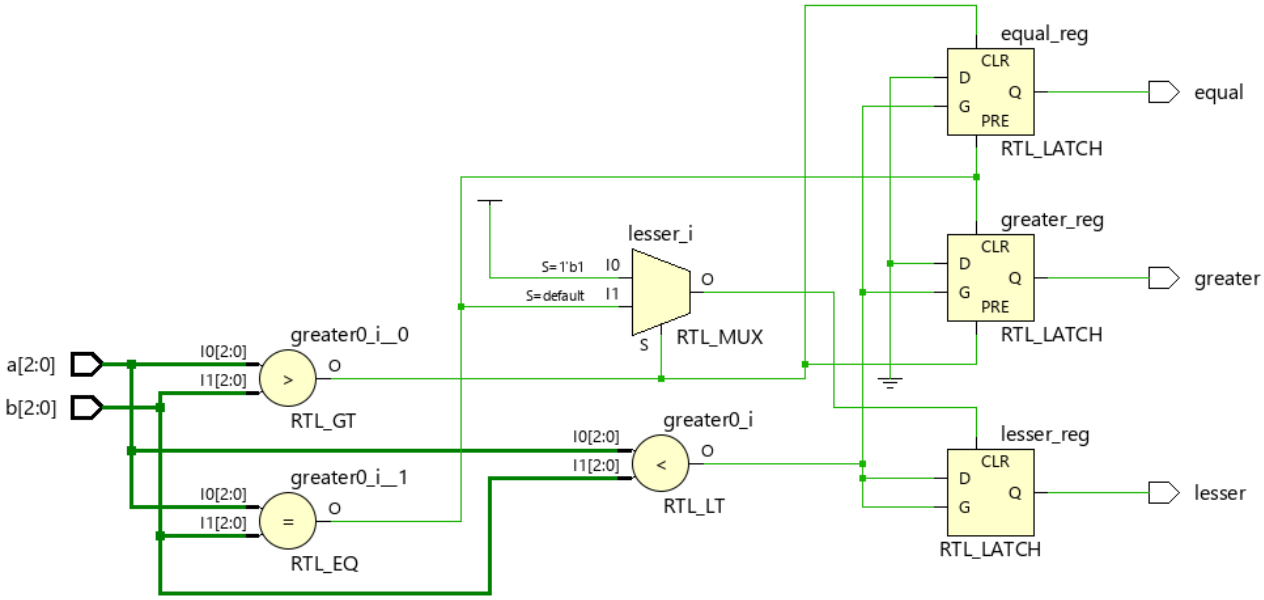
Testbench:

```
`timescale 1ns / 1ps


module n_bit_comparator__tb(

    );
   parameter n=3;
    reg [(n-1):0]a;
    reg[(n-1):0]b;
    wire greater,equal,lesser;

    n_bit_comparator uut(a,b,greater,equal,lesser);

    initial begin

    #10 a=3'b000; b=3'b111;
    #10 a=3'b001; b=3'b000;
    #10 a=3'b101; b=3'b101;
    #10 a=3'b011; b=3'b100;
    #10 a=3'b010; b=3'b010;
    #10 a=3'b111; b=3'b111;
    #10 $finish;
    end

     initial begin
       $dumpfile("dump.vcd");
       $dumpvars(0);
     end
endmodule
```

Simulation:



Schematic:



Synthesis report:

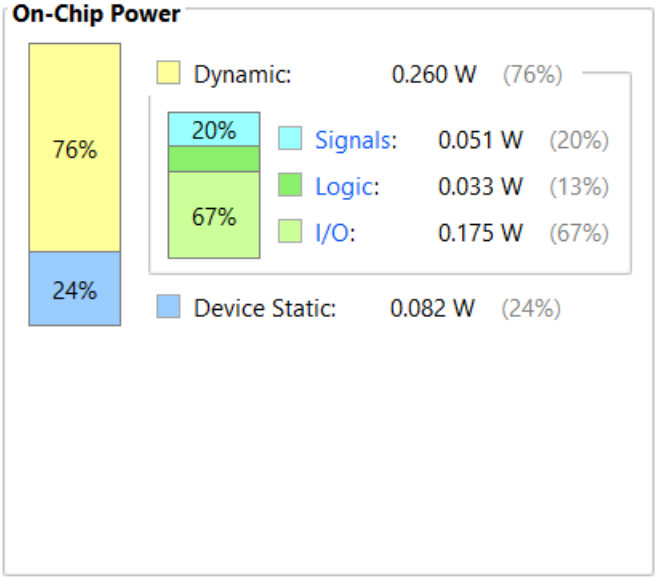
```
---------------------------------
Start Writing Synthesis Report
---------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |LUT6 |     5|
|2     |LDC  |     1|
|3     |LDCP |     2|
|4     |IBUF |     6|
|5     |OBUF |     3|
+------+-----+------+

Report Instance Areas:
+------+---------+-------+------+
|      |Instance |Module |Cells |
+------+---------+-------+------+
|1     |top      |       |    17|
+------+---------+-------+------+
---------------------------------
Finished Writing Synthesis Report
```

Power report:

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**0.341 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**25.6°C**
Thermal Margin:	59.4°C (31.3 W)
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



10.Serial in serial out shift register

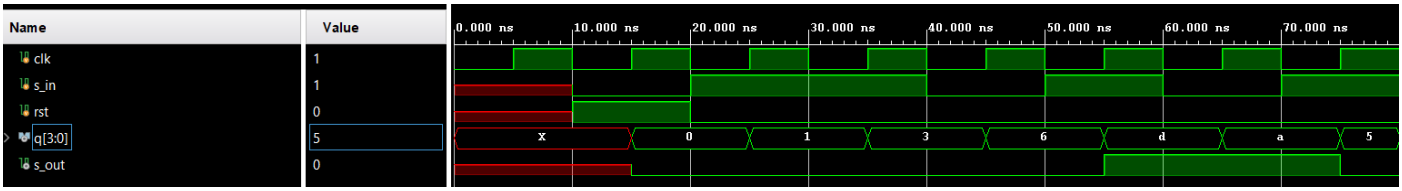
Verilog code:

```
`timescale 1ns / 1ps

module serial_in_serial_out(
    input clk,
    input rst,
    output reg [3:0] q,
    input s_in,
    output reg s_out
    );


    always @ (posedge clk)
    begin
    if(rst)
    begin
    q=4'b0000;
    s_out=1'b0;
    end
    else
    begin
        q=q<<1;
        q[0]=s_in;
        s_out = q[3];
    end
  end

endmodule
```

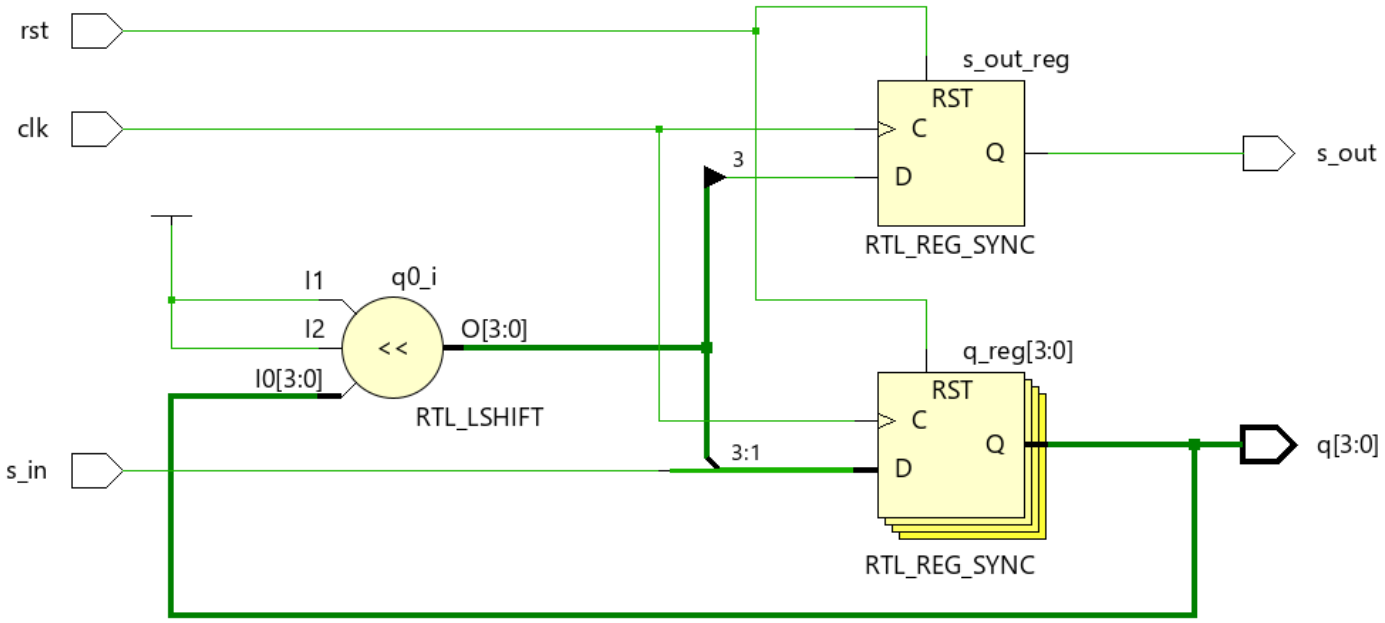
Testbench:

```
`timescale 1ns / 1ps


module serial_in_serial_out_tb(

    );

        reg clk,s_in;
        reg rst;
        wire [3:0]q;
        wire s_out;

        serial_in_serial_out uut(clk,rst,q,s_in,s_out);

        initial begin
               clk = 0;
               forever #5 clk = ~clk;
             end
             initial
               begin
                 #10 rst = 1'b1;
                 #10 rst = 1'b0;
                 #100 $finish;

               end
             initial begin

               #10 s_in = 1'b0;
               #10 s_in = 1'b1;
               #10 s_in = 1'b1;
               #10 s_in = 1'b0;
               #10 s_in = 1'b1;
               #10 s_in = 1'b0;
               #10 s_in = 1'b1;
               #10 $finish;
               end
endmodule
```

Simulation:



Schematic:



Synthesis report:

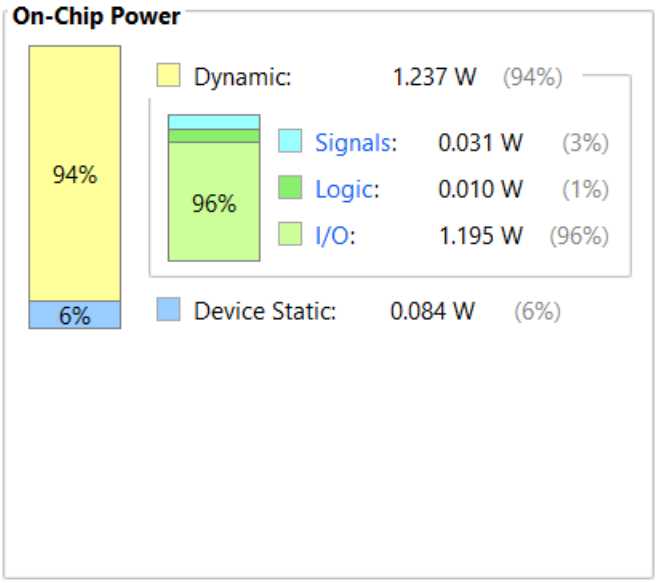
```
Start Writing Synthesis Report
---------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |BUFG |     1|
|2     |LUT2 |     2|
|3     |FDRE |     4|
|4     |IBUF |     3|
|5     |OBUF |     5|
+------+-----+------+

Report Instance Areas:
+------+---------+-------+------+
|      |Instance |Module |Cells |
+------+---------+-------+------+
|1     |top      |       |    15|
+------+---------+-------+------+
---------------------------------
Finished Writing Synthesis Report
```

Power report:

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**1.32 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**27.5°C**
Thermal Margin:	57.5°C (30.3 W)
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



11.Serial in parallel out shift register

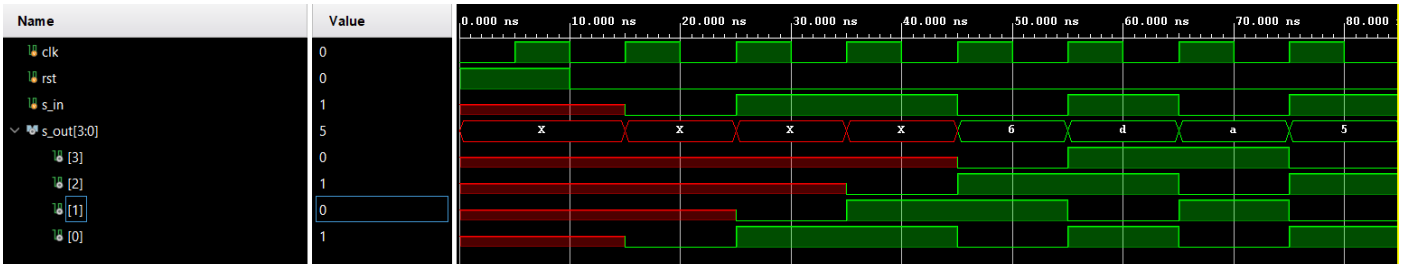
Verilog code:

```
`timescale 1ns / 1ps


module serial_in_parallel_out(
    input clk,
    input rst,
    input s_in,
    output [3:0] s_out
    );
       Dff d1(clk,reset,s_in,s_out[0]);
       Dff d2(clk,reset,s_out[0],s_out[1]);
       Dff d3(clk,reset,s_out[1],s_out[2]);
       Dff d4(clk,reset,s_out[2],s_out[3]);
endmodule

module Dff(
    input clk,
    input rst,
    input d,
    output reg q
    );
      always @ (posedge clk)
      begin
      if(rst)
        q=0;

      else if(clk)

        q = d ;
      end
endmodule
```

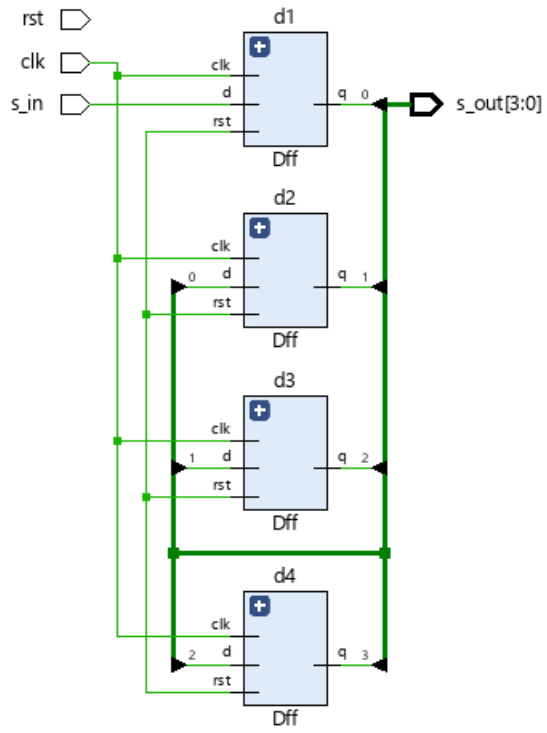
Testbench:

```
module serial_in_parallel_out_tb(

    );
  reg clk,rst;
  reg s_in;
  wire [3:0]s_out;

   serial_in_parallel_out uut(clk,rst,s_in,s_out);

    initial begin

    clk = 1'b0;
    forever #5 clk = ~clk;
    end

     initial begin
     rst=1'b1;

     #10 rst = 1'b0;

     end

    always @ (posedge clk,s_in)
    begin

                    #10 s_in = 1'b0;
                    #10 s_in = 1'b1;
                    #10 s_in = 1'b1;
                    #10 s_in = 1'b0;
                    #10 s_in = 1'b1;
                    #10 s_in = 1'b0;
                    #10 s_in = 1'b1;
                    #10 $finish;
   end

endmodule
```

Simulation:



Schematic:



Synthesis report:

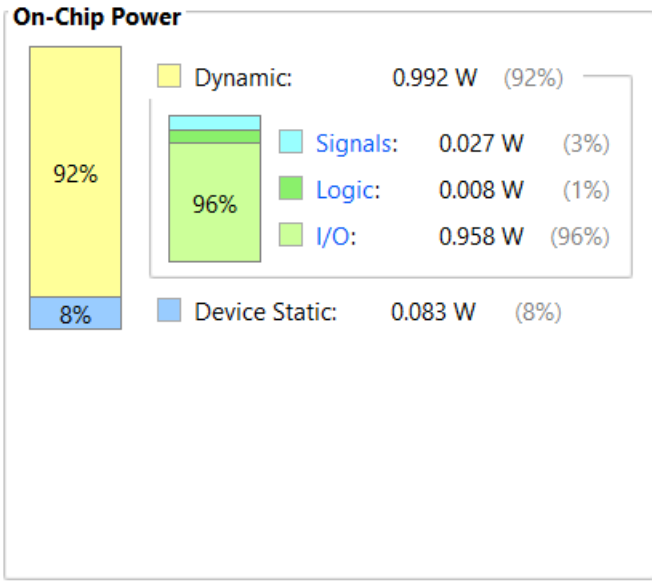
```
Start Writing Synthesis Report
---------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |BUFG |     1|
|2     |FDRE |     4|
|3     |IBUF |     2|
|4     |OBUF |     4|
+------+-----+------+

Report Instance Areas:
+------+---------+-------+------+
|      |Instance |Module |Cells |
+------+---------+-------+------+
|1     |top      |       |    11|
|2     |  d1     |Dff    |     1|
|3     |  d2     |Dff_0  |     1|
|4     |  d3     |Dff_1  |     1|
|5     |  d4     |Dff_2  |     1|
+------+---------+-------+------+
---------------------------------
Finished Writing Synthesis Report
```

Power report:

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**1.075 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**27.0°C**
Thermal Margin:	58.0°C (30.6 W)
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



12.Parallel in parallel out register

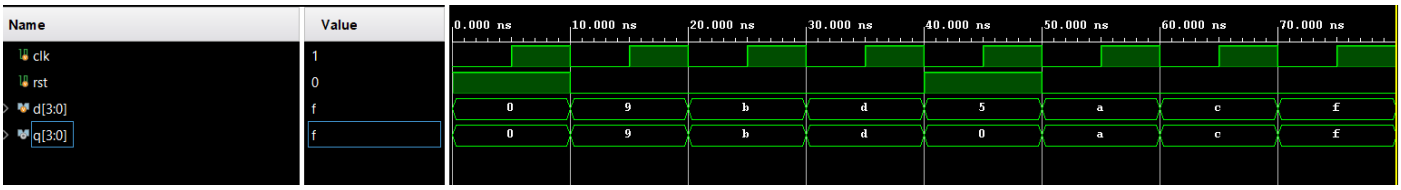
Verilog code:

```
module parallel_in_parallel_out(
 input clk,
    input rst,
    input [3:0] d,
    output reg [3:0] q
    );
     always @ (posedge clk,d)
    begin
    if(rst)
    q<=4'b0000;
    else
    q<=d;

    end
endmodule
```

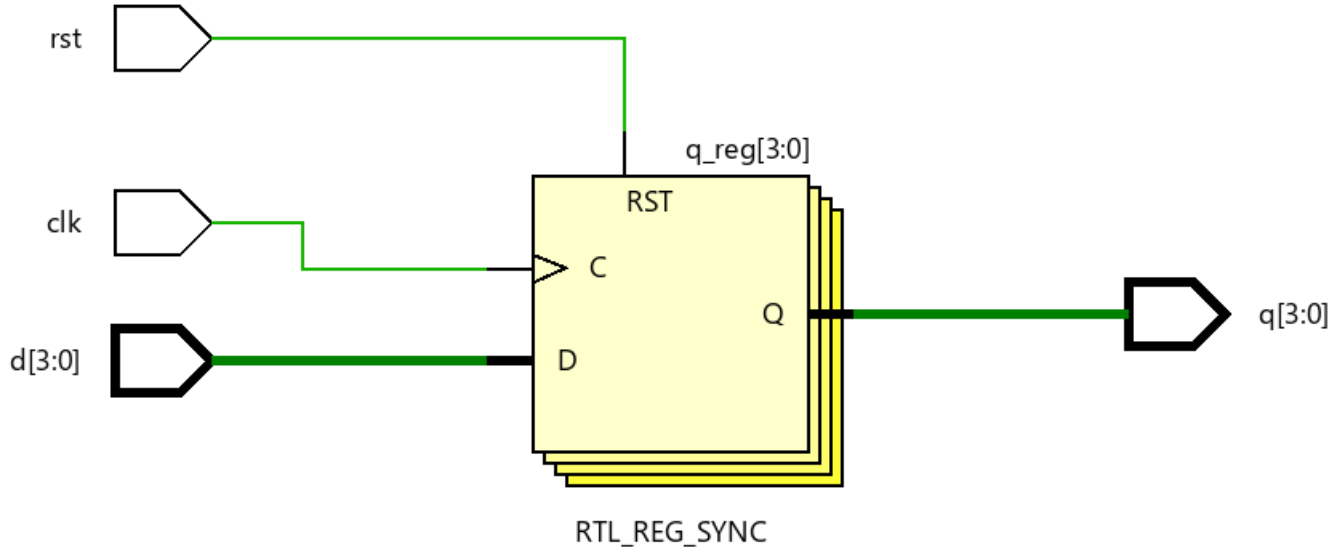
Testbench:

```
module parallel_in_parallel_out_tb(

    );
    reg clk,rst;
reg [3:0]d;
wire [3:0]q;

     parallel_in_parallel_out uut(clk,rst,d,q);

  initial begin
    $monitor("%t | d = %b | q = %b",$time,d,q);
  end

  initial begin
    clk=1'b0;
    forever #5 clk=~clk;
  end

  initial begin
    rst = 1'b1;
    #10 rst = 1'b0;
  end

  initial begin
      #00 d=4'b0000;
      #10 d=4'b1001;
      #10 d=4'b1011;
      #10 d=4'b1101;
      #10 d=4'b0101;rst=1'b1;
      #10 d=4'b1010;rst=1'b0;
      #10 d=4'b1100;
      #10 d=4'b1111;
      #10 $finish;
      end

endmodule
```

Simulation:



Schematic:



Synthesis report:

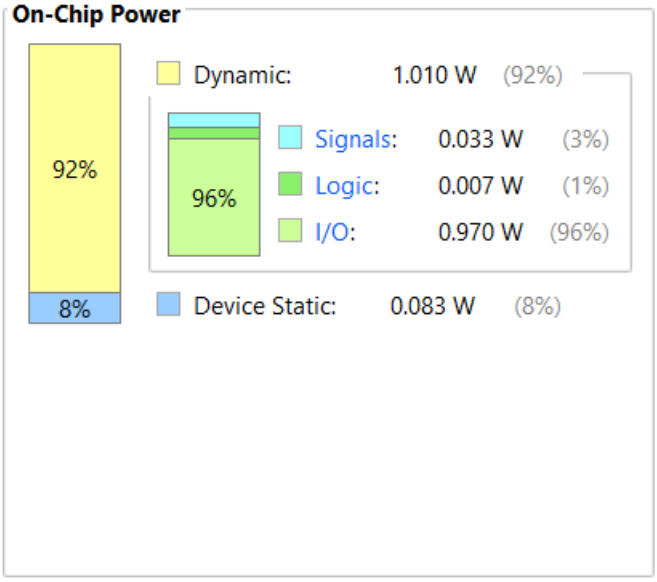
```
Start Writing Synthesis Report
---------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |BUFG |     1|
|2     |FDRE |     4|
|3     |IBUF |     6|
|4     |OBUF |     4|
+------+-----+------+

Report Instance Areas:
+------+---------+-------+------+
|      |Instance |Module |Cells |
+------+---------+-------+------+
|1     |top      |       |    15|
+------+---------+-------+------+
---------------------------------
Finished Writing Synthesis Report
```

Power report:

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**1.093 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**27.1°C**
Thermal Margin:	57.9°C (30.6 W)
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



13.Parallel in serial out register

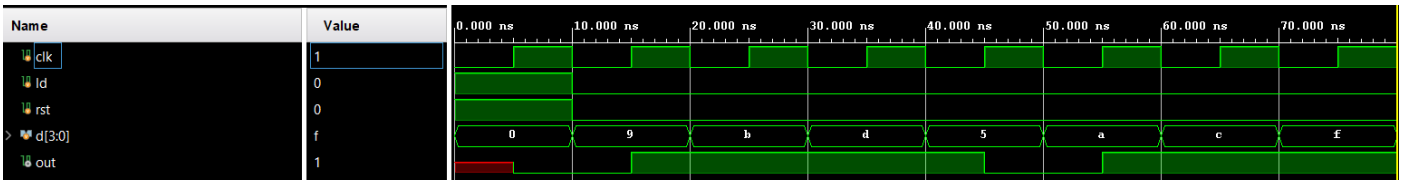
Verilog code:

```
module parallel_in_serial_out(
    input clk,ld,rst,[3:0] d,
    output  out,
    output [3:0]q
    );
    wire x1,x2,x3;

     d_ff d1(clk,rst,d[0],x1);
     logic s1(d[1],x1,ld,q[0]);

     d_ff d2(clk,rst,q[0],x2);
     logic s2(d[2],x2,ld,q[1]);

     d_ff d3(clk,rst,q[1],x3);
     logic s3(d[3],x3,ld,q[2]);

     d_ff d4(clk,rst,q[2],out);
endmodule

module d_ff(
input clk, rst,d,
output reg q
);

always @ (posedge clk)
     begin
        if(rst)
        q = 1'b0;
        else
        q = d;
     end
endmodule

module logic(
 input d,si,ld,
 output q
);

assign q = (si & ld) | (d & ~ld);
endmodule
```

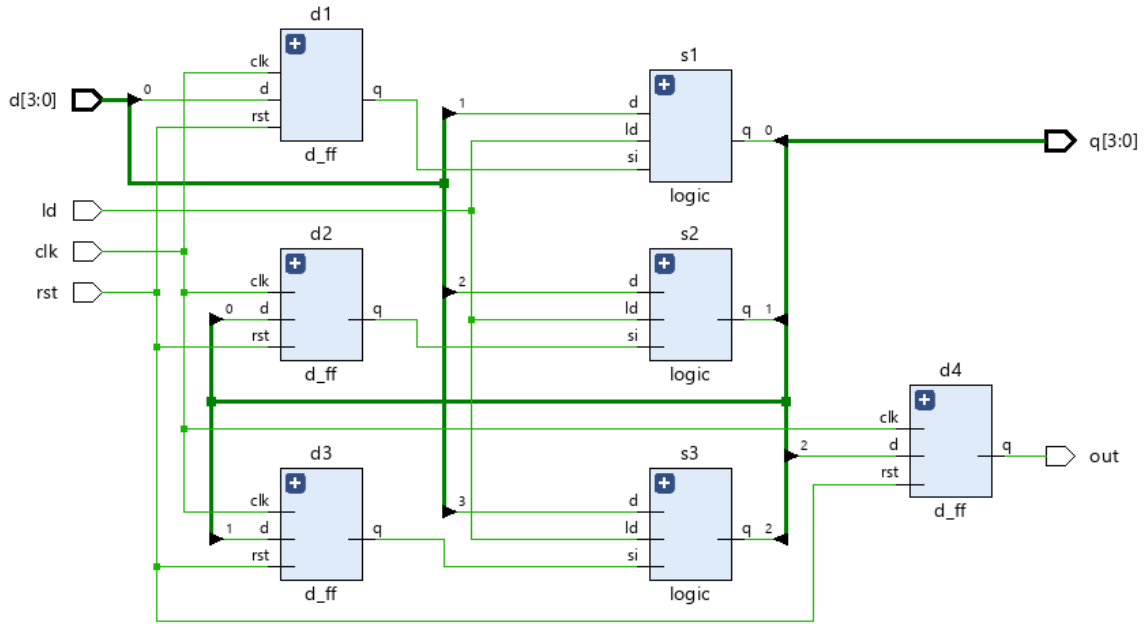
Testbench:

```
module parallel_in_serial_out_tb(

    );
reg clk,ld;
reg rst;
reg [3:0]d;
wire out;

parallel_in_serial_out uut(clk,ld,rst,d,out);

   initial begin
   clk = 1'b0;
   forever #5 clk = ~clk;
   end

   initial begin
       rst = 1'b1;  ld  = 1'b1;
   #10 rst = 1'b0;  ld  = 1'b0;
    end

     initial begin
       #00 d=4'b0000;
       #10 d=4'b1001;
       #10 d=4'b1011;
       #10 d=4'b1101;
       #10 d=4'b0101;
       #10 d=4'b1010;
       #10 d=4'b1100;
       #10 d=4'b1111;

       #10 $finish;
       end

endmodule
```

Simulation:



Schematic:



Synthesis report:

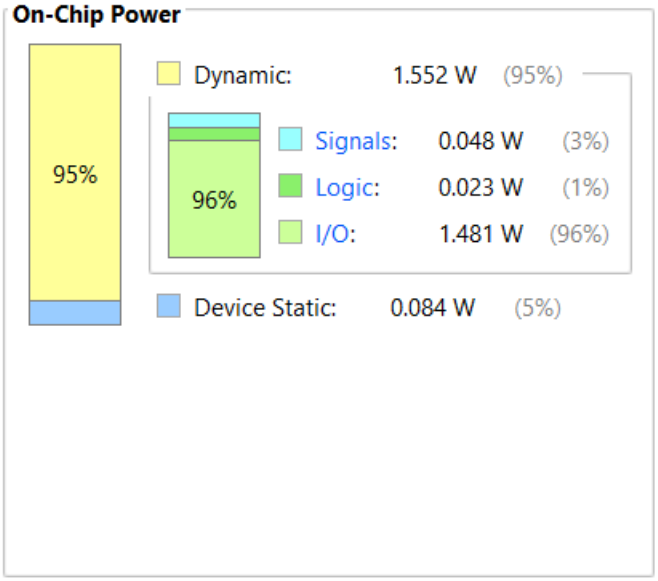
```
Start Writing Synthesis Report
---------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+------+------+
|      |Cell  |Count |
+------+------+------+
|1     |BUFG  |     1|
|2     |LUT3  |     3|
|3     |LUT4  |     2|
|4     |FDRE  |     4|
|5     |IBUF  |     7|
|6     |OBUF  |     4|
|7     |OBUFT |     1|
+------+------+------+

Report Instance Areas:
+------+---------+--------+------+
|      |Instance |Module  |Cells |
+------+---------+--------+------+
|1     |top      |        |    22|
|2     |  d1     |d_ff    |     2|
|3     |  d2     |d_ff_0  |     2|
|4     |  d3     |d_ff_1  |     1|
|5     |  d4     |d_ff_2  |     1|
|6     |  s1     |logic   |     1|
|7     |  s2     |logic_3 |     1|
|8     |  s3     |logic_4 |     1|
+------+---------+--------+------+
---------------------------------
Finished Writing Synthesis Report
```

Power report:

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**1.636 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**28.1°C**
Thermal Margin:	56.9°C (30.0 W)
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



14.Bidirection shift register

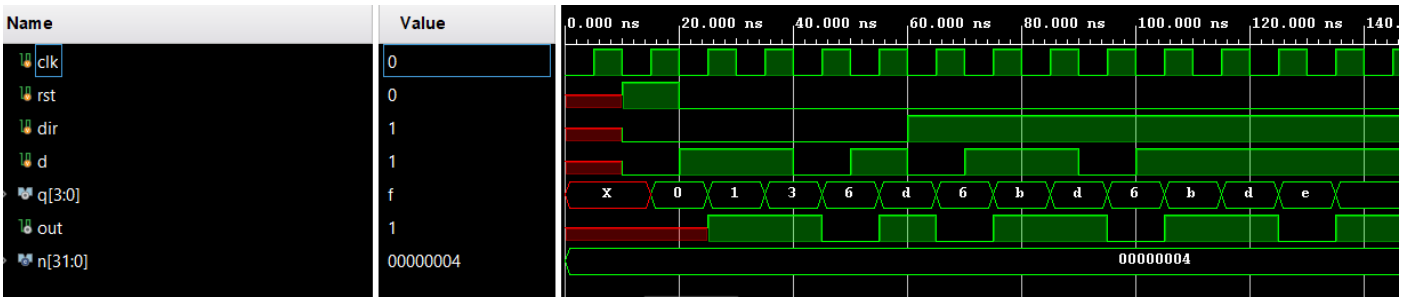
Verilog code:

```
module bidirection_shift_register(
 input clk,rst,dir,d,
 output reg [n-1:0]q,
 output reg out
     );
  parameter n = 4;

  always @ (posedge clk)
    begin

      if(rst)
         q = 4'b0000;
       else
          begin
           case(dir)
              0  : begin  q = {q[n-2:0],d}; out <= q[0]; end
              1  : begin  q = {d,q[n-1:1]}; out <= q[0]; end
           endcase
          end

    end
endmodule
```

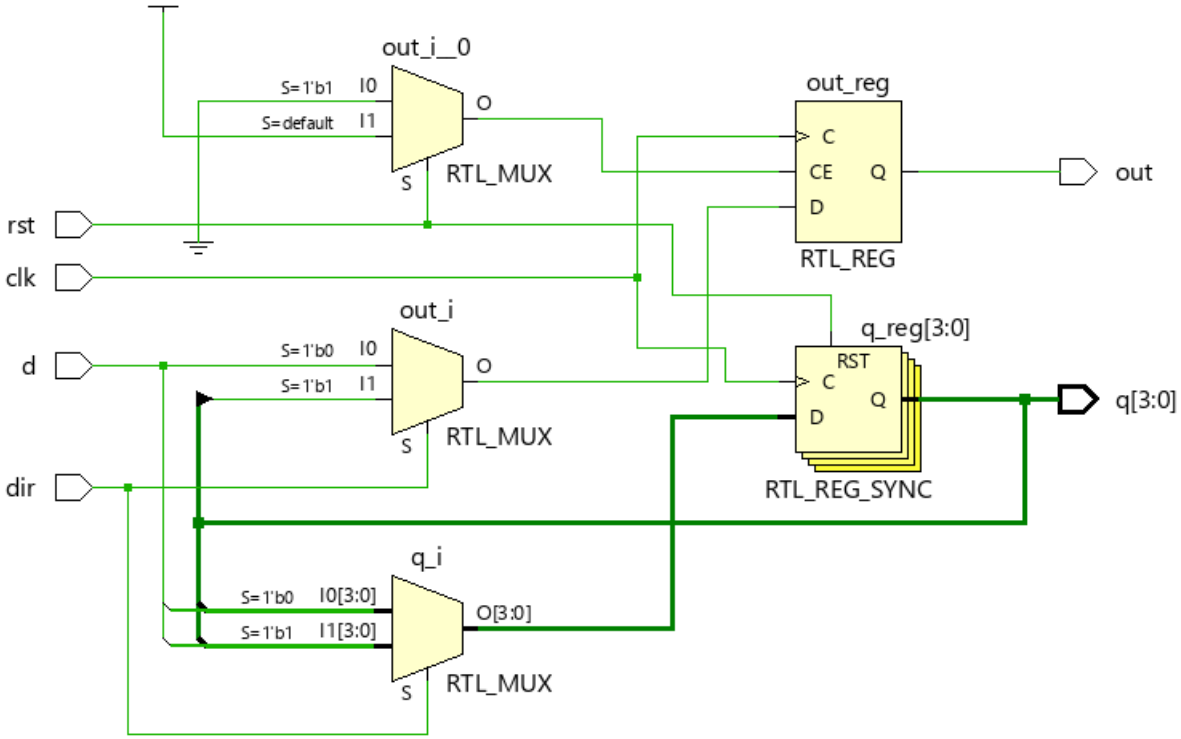
Testbench:

```
module bidirection_shift_register_tb( );
     parameter n = 4;
          reg clk,rst,dir,d;
          wire [n-1:0]q;
          wire out;

          bidirection_shift_register uut(clk,rst,dir,d,q,out );

          initial begin
          $monitor("clk = %t | dir = %b | d = %b | q = %b",$time,dir,d,q);
          end

          initial begin
          clk = 1'b0;
          forever #5 clk = ~clk;
          end

          initial begin
          #10 rst = 1'b1;
          #10 rst = 1'b0;
          end

          initial begin

          #10  dir = 0 ; d=1'b0;
          #10  dir = 0 ; d=1'b1;
          #10  dir = 0 ; d=1'b1;
          #10  dir = 0 ; d=1'b0;
          #10  dir = 0 ; d=1'b1;
          #10  dir = 1 ; d=1'b0;
          #10  dir = 1 ; d=1'b1;
          #10  dir = 1 ; d=1'b1;
          #10  dir = 1 ; d=1'b0;
          #10  dir = 1 ; d=1'b1;

          end
endmodule
```

Simulation:



Schematic:



Synthesis report:

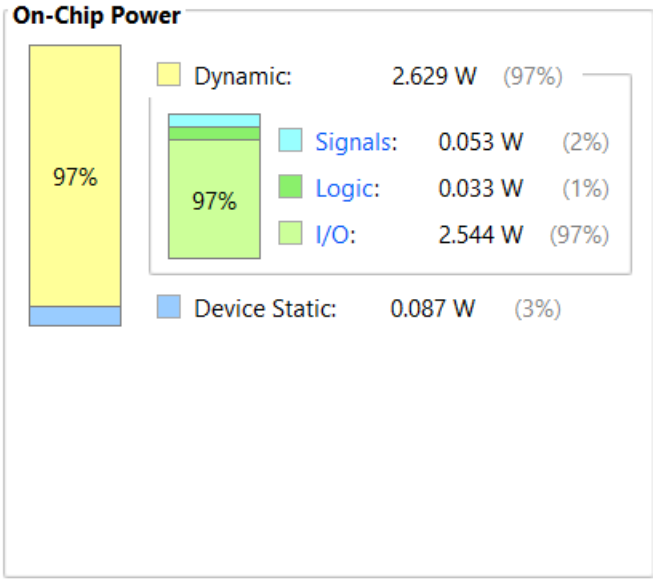
```
Start Writing Synthesis Report
---------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |BUFG |     1|
|2     |LUT1 |     1|
|3     |LUT3 |     5|
|4     |FDRE |     5|
|5     |IBUF |     4|
|6     |OBUF |     5|
+------+-----+------+

Report Instance Areas:
+------+---------+-------+------+
|      |Instance |Module |Cells |
+------+---------+-------+------+
|1     |top      |       |    21|
+------+---------+-------+------+
---------------------------------
Finished Writing Synthesis Report
---------------------------------
```

Power report:

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**2.716 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**30.1°C**
Thermal Margin:	54.9°C (28.9 W)
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



15.PRBS Sequence generator

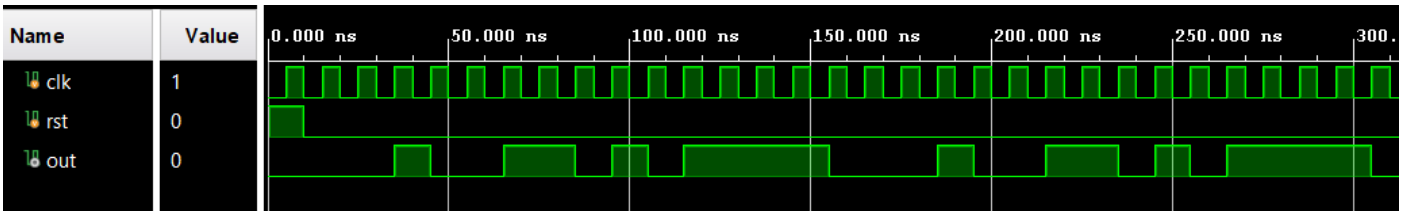
Verilog code:

```
module prbs(
    input clk,
    input rst,
    output out
    );
    reg [3:0] temp;

    always @ (posedge clk or posedge rst)
    begin
     if(rst)
       temp =4'b1000;
      else if(clk)

      temp <={temp[1] ^ temp[0],temp[3],temp[2],temp[1]};
     end
  assign out = temp[0];
endmodule
```

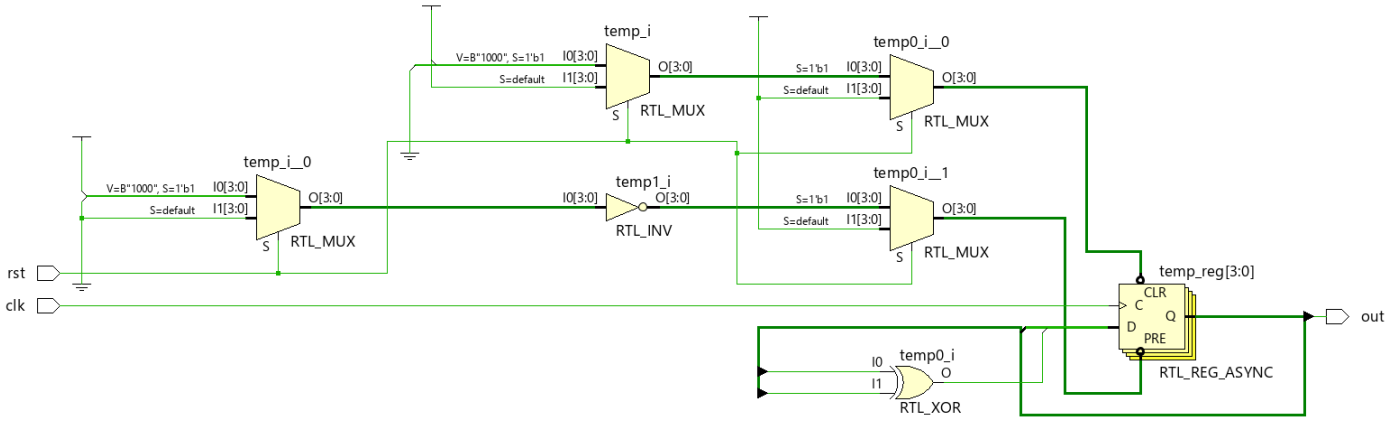
Testbench:

```
module prbs_tb();

    reg clk, rst;
    wire out;

   prbs uut ( clk, rst,out);

   initial begin
   $monitor("clk = %t | rst = %b | out = %b ",$time,rst,out);
   end

  initial begin
      clk <= 0;
   forever #5  clk <= ~clk;
    end

    initial begin
           rst = 1;
     #10   rst = 0;
   end

     initial begin
       #500 $finish;
     end
endmodule
```

Simulation:



Schematic:



Synthesis report:

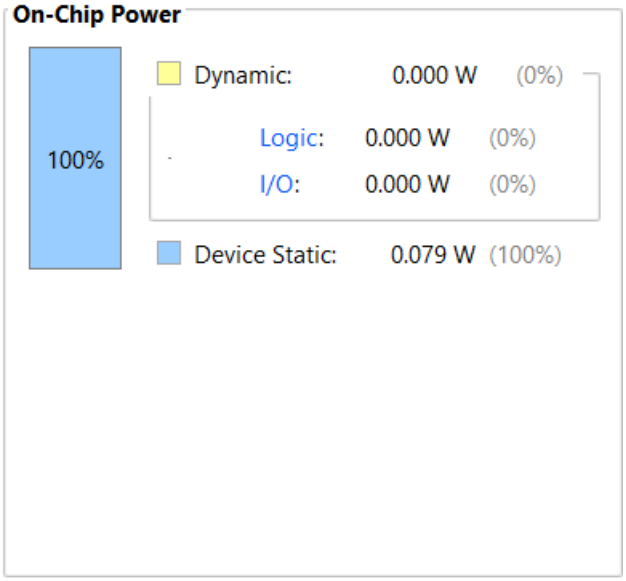
```
Start Writing Synthesis Report
-------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |OBUF |     1|
+------+-----+------+

Report Instance Areas:
+------+---------+-------+------+
|      |Instance |Module |Cells |
+------+---------+-------+------+
|1     |top      |       |     1|
+------+---------+-------+------+
-------------------------------
Finished Writing Synthesis Report
```

Power report:

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**0.079 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**25.1°C**
Thermal Margin:	59.9°C (31.6 W)
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	High

Launch Power Constraint Advisor to find and fix invalid switching activity



16.8-Bit Subtractor

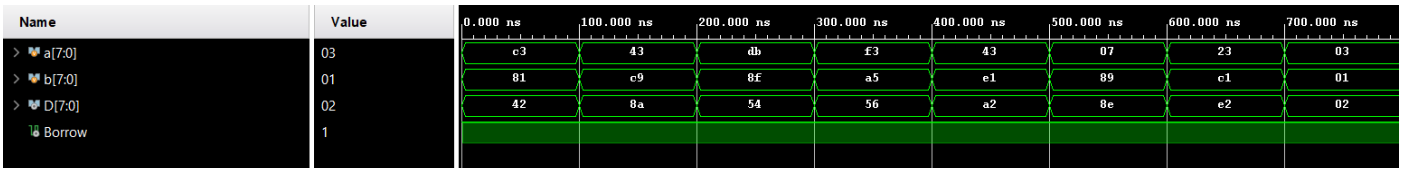
Verilog code:

```
module subtractor_8bit(
 input [7:0] a,[7:0] b,[7:0]D,
 output Borrow
    );
    wire x1,x2,x3,x4,x5,x6,x7;

    full_subtractor  s1(a[0],b[0],1'b0,x1,D[0]);
    full_subtractor  s2(a[1],b[1],1'b0,x2,D[1]);
    full_subtractor  s3(a[2],b[2],1'b0,x3,D[2]);
    full_subtractor  s4(a[3],b[3],1'b0,x4,D[3]);
    full_subtractor  s5(a[4],b[4],1'b0,x5,D[4]);
    full_subtractor  s6(a[5],b[5],1'b0,x6,D[5]);
    full_subtractor  s7(a[6],b[6],1'b0,x7,D[6]);
    full_subtractor  s8(a[7],b[7],1'b0,Borrow,D[7]);

endmodule

module full_subtractor(
    input x,y,z,
    output borrow,diff
    );

    assign diff = x^y^z;
    assign borrow = ~x^y | ~x^z | y^z;
endmodule
```

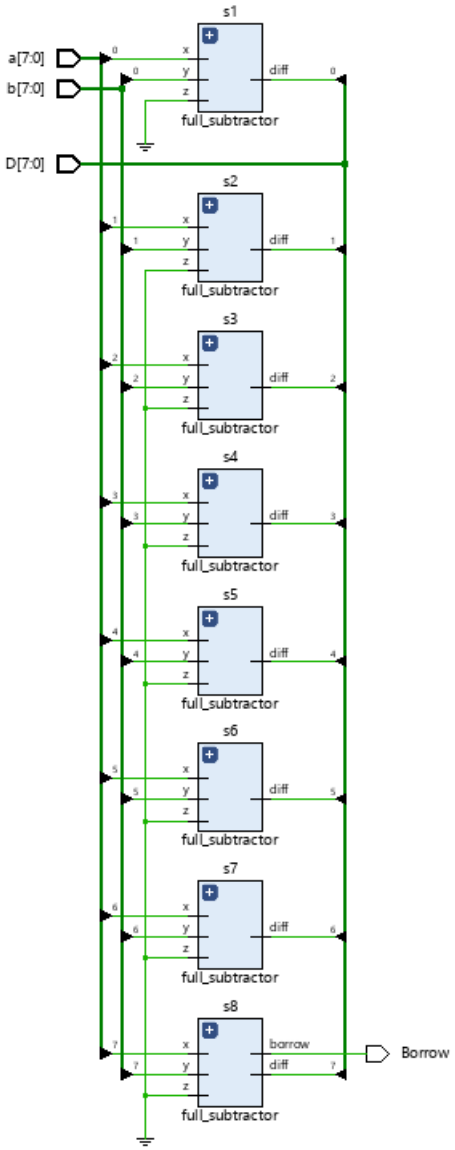
Testbench:

```
module subtractor_8bit_tb(

    );
    reg[7:0]a;
    reg[7:0]b;
    wire [7:0] D;
    wire Borrow;

    initial begin
     $monitor($time |" $time |a = %b | b = %b | borrow = %b | D = %b | borrow = %b ",a,b,Borrow,D);
    end

       subtractor_8bit uut(a,b,D,Borrow);

      initial begin

        #000 a=8'b11000011; b=8'b10000001;
        #100 a=8'b01000011; b=8'b11001001;
        #100 a=8'b11011011; b=8'b10001111;
        #100 a=8'b11110011; b=8'b10100101;
        #100 a=8'b01000011; b=8'b11100001;
        #100 a=8'b00000111; b=8'b10001001;
        #100 a=8'b00100011; b=8'b11000001;
        #100 a=8'b00000011; b=8'b00000001;

        #100 $finish;

        end

      initial begin
        $dumpfile("dump.vcd");
        $dumpvars(0);
      end
endmodule
```

Simulation:



Schematic:



Synthesis report:

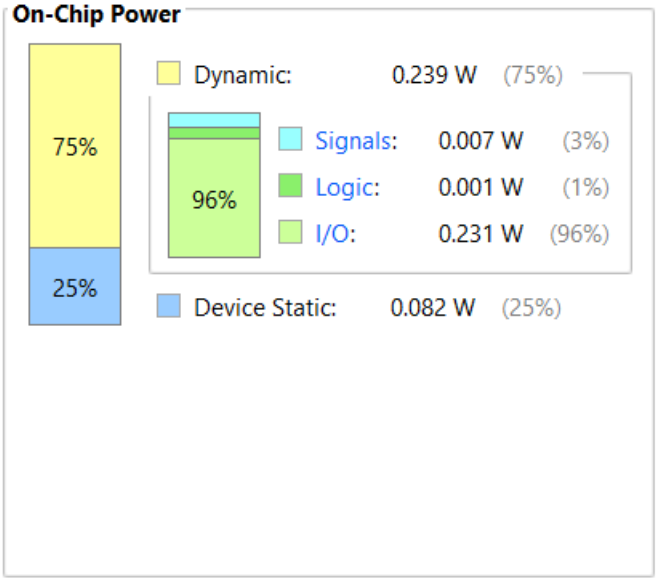
```
Start Writing Synthesis Report
---------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |LUT2 |     1|
|2     |IBUF |     2|
|3     |OBUF |     1|
+------+-----+------+

Report Instance Areas:
+------+---------+-------+------+
|      |Instance |Module |Cells |
+------+---------+-------+------+
|1     |top      |       |     4|
+------+---------+-------+------+
---------------------------------
Finished Writing Synthesis Report
```

Power report:

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**0.321 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**25.6°C**
Thermal Margin:	59.4°C (31.3 W)
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



17.8-Bit Adder/subtractor

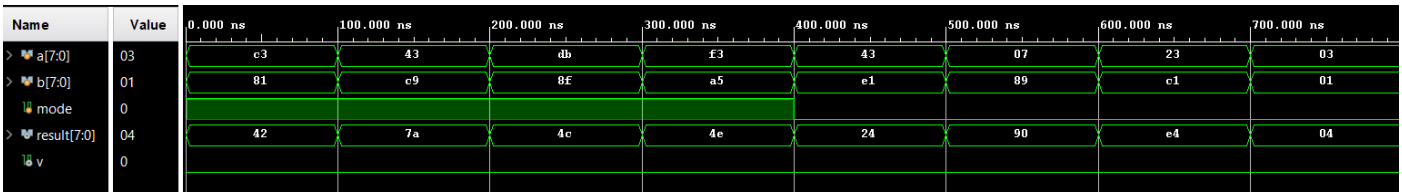
Verilog code:

```
module bit8_adder_sub(
    input [7:0] a,
    input [7:0] b,
    input mode,
    output reg [7:0] result,
    output reg v
    );

    reg [7:0]com;

    always @ (a,b,mode)
     begin
       if(mode == 1)
        begin
          com = ~b + 1'b1;
          result = a + com;
            v = (a[7]&com[7]&~result[7]) | (~a[7]&~com[7]&result[7]);
        end
       else if(mode == 0)
        begin
           result = a + b;
            v = (a[7]&b[7]&~result[7]) | (~a[7]&~b[7]&result[7]);
        end
      end


endmodule
```

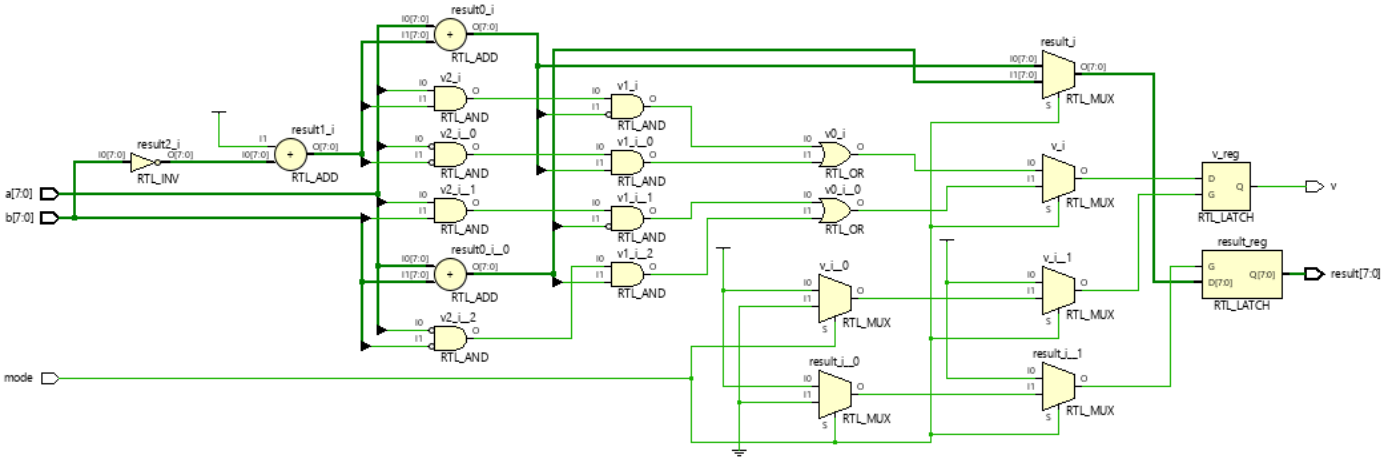
Testbench:

```
module bit8_sub_add_tb(
    );
        reg [7:0] a,b;
        reg mode;
        wire [7:0] result;
        wire v;

         initial begin
                $monitor($time |" $time |a = %b | b = %b | mode = %b | v = %b | result = %b ",a,b,mode,v,result);
         end

               bit8_adder_sub uut(a,b,mode,result,v);

              initial begin
                #000 mode = 1'b1; a=8'b11000011; b=8'b10000001;
                #100 mode = 1'b1; a=8'b01000011; b=8'b11001001;
                #100 mode = 1'b1; a=8'b11011011; b=8'b10001111;
                #100 mode = 1'b1; a=8'b11110011; b=8'b10100101;
                #100 mode = 1'b0; a=8'b01000011; b=8'b11100001;
                #100 mode = 1'b0; a=8'b00000111; b=8'b10001001;
                #100 mode = 1'b0; a=8'b00100011; b=8'b11000001;
                #100 mode = 1'b0; a=8'b00000011; b=8'b00000001;
                #100 $finish;
                end

              initial begin
                $dumpfile("dump.vcd");
                $dumpvars(0);
              end

endmodule
```

Simulation:



Schematic:



Synthesis report:

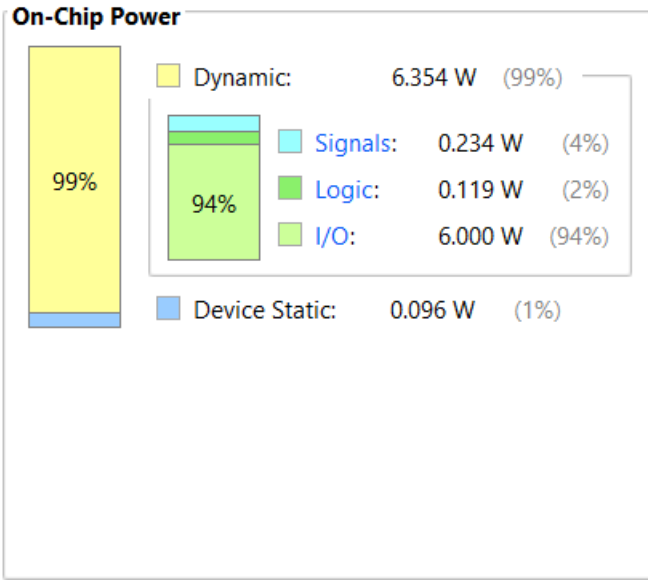
```
Start Writing Synthesis Report
---------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-------+------+
|      |Cell   |Count |
+------+-------+------+
|1     |CARRY4 |     4|
|2     |LUT2   |    16|
|3     |LUT3   |     8|
|4     |LUT4   |     2|
|5     |LUT6   |     1|
|6     |IBUF   |    17|
|7     |OBUF   |     9|
+------+-------+------+

Report Instance Areas:
+------+---------+-------+------+
|      |Instance |Module |Cells |
+------+---------+-------+------+
|1     |top      |       |    57|
+------+---------+-------+------+
---------------------------------
Finished Writing Synthesis Report
```

Power report:

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**6.45 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**37.1°C**
Thermal Margin:	47.9°C (25.2 W)
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



18.4-Bit Multiplier

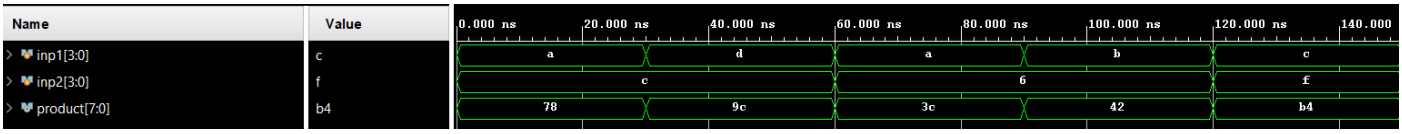
Verilog code:

```
module multiplier_4bit(
product,inp1,inp2
    );
      output [7:0]product;
  input [3:0]inp1;
  input [3:0]inp2;

  assign product[0]=(inp1[0]&inp2[0]);

  wire x1,x2,x3,x4,x5,x6,x7,x8,x9,x10,x11,x12,x13,x14,x15,x16,x17;

  HA HA1(product[1],x1,(inp1[1]&inp2[0]),(inp1[0]&inp2[1]));
  FA FA1(x2,x3,inp1[1]&inp2[1],(inp1[0]&inp2[2]),x1);
  FA FA2(x4,x5,(inp1[1]&inp2[2]),(inp1[0]&inp2[3]),x3);
  HA HA2(x6,x7,(inp1[1]&inp2[3]),x5);

  HA HA3(product[2],x15,x2,(inp1[2]&inp2[0]));
  FA FA5(x14,x16,x4,(inp1[2]&inp2[1]),x15);
  FA FA4(x13,x17,x6,(inp1[2]&inp2[2]),x16);
  FA FA3(x9,x8,x7,(inp1[2]&inp2[3]),x17);

  HA HA4(product[3],x12,x14,(inp1[3]&inp2[0]));
  FA FA8(product[4],x11,x13,(inp1[3]&inp2[1]),x12);
  FA FA7(product[5],x10,x9,(inp1[3]&inp2[2]),x11);
  FA FA6(product[6],product[7],x8,(inp1[3]&inp2[3]),x10);
endmodule

module HA(sout,cout,a,b);
  output sout,cout;
  input a,b;
  assign sout=a^b;
  assign cout=(a&b);
endmodule

module FA(sout,cout,a,b,cin);
  output sout,cout;
  input a,b,cin;
  assign sout=(a^b^cin);
  assign cout=((a&b)|(a&cin)|(b&cin));
endmodule
```

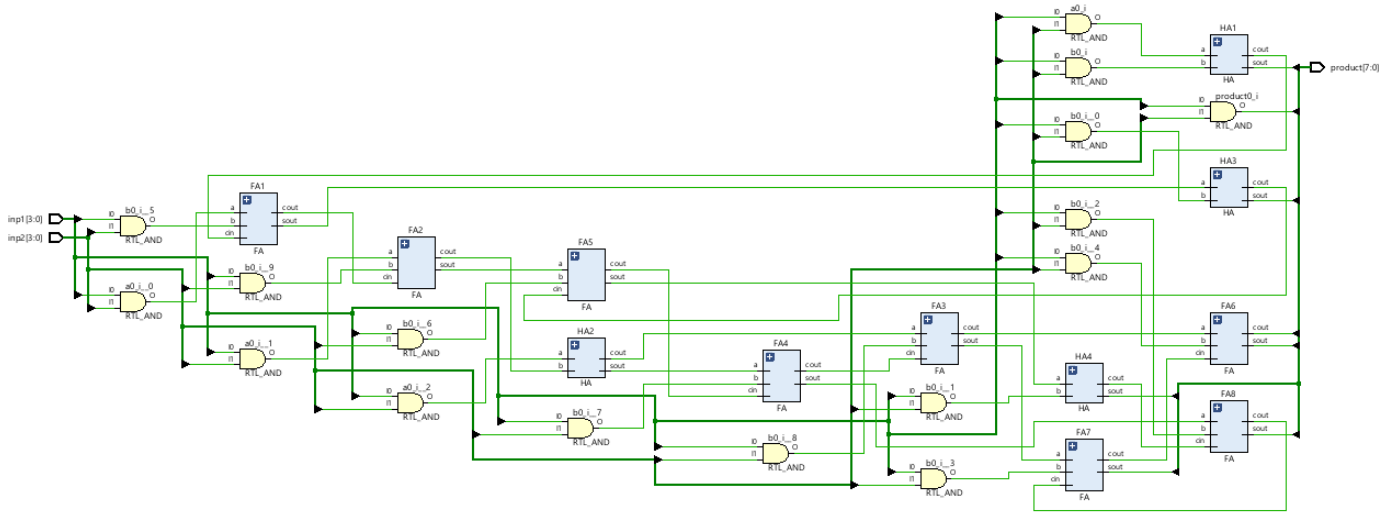
Testbench:

```
module multiplier_4bit_tb(

    );
   reg [3:0]inp1;
   reg [3:0]inp2;
   wire [7:0]product;

    multiplier_4bit uut(.inp1(inp1),.inp2(inp2),.product(product));

   initial
   begin
     inp1=10;
     inp2=12;
     #30 ;

     inp1=13;
     inp2=12;
     #30 ;

     inp1=10;
     inp2=22;
     #30 ;

     inp1=11;
     inp2=22;
     #30 ;

     inp1=12;
     inp2=15;
     #30 ;

     $finish;
   end
endmodule
```

Simulation:



Schematic:



Synthesis report:

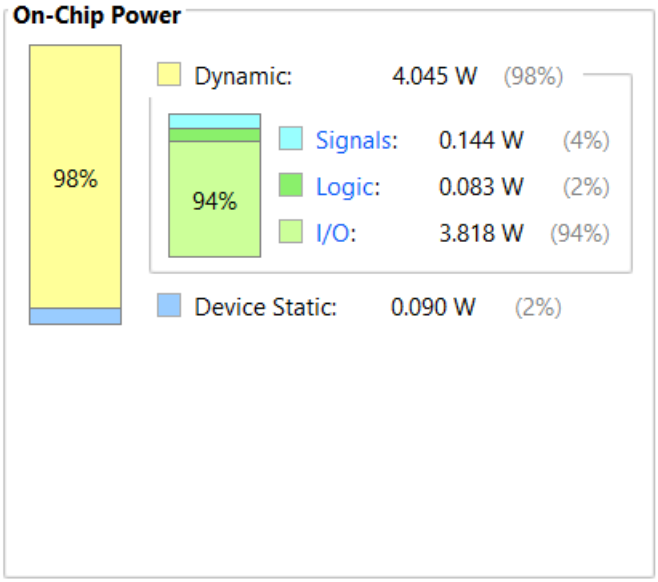
```
Start Writing Synthesis Report
---------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |LUT2 |     1|
|2     |LUT4 |     6|
|3     |LUT6 |    11|
|4     |IBUF |     8|
|5     |OBUF |     8|
+------+-----+------+

Report Instance Areas:
+------+---------+-------+------+
|      |Instance |Module |Cells |
+------+---------+-------+------+
|1     |top      |       |    34|
+------+---------+-------+------+
---------------------------------
Finished Writing Synthesis Report
---------------------------------
```

Power report:

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**4.135 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**32.8°C**
Thermal Margin:	52.2°C (27.5 W)
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



19.Fixed point division

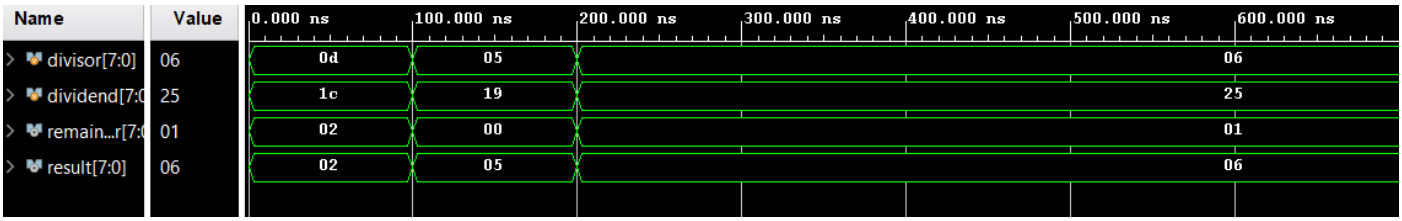
Verilog code:

```
module fixed_point_division(divisor, dividend, remainder, result);

input [7:0] divisor, dividend;
output reg [7:0] result, remainder;


integer i;
reg [7:0] divisor_copy, dividend_copy;
reg [7:0] temp;

always @(divisor or dividend)
begin
    divisor_copy = divisor;
    dividend_copy = dividend;
    temp = 0;
    for(i = 0;i < 8;i = i + 1)
    begin
        temp = {temp[6:0], dividend_copy[7]};
        dividend_copy[7:1] = dividend_copy[6:0];

        temp = temp - divisor_copy;

        if(temp[7] == 1)
        begin

            dividend_copy[0] = 0;
            temp = temp + divisor_copy;
        end
        else
        begin

            dividend_copy[0] = 1;
        end
    end
    result = dividend_copy;
    remainder = dividend - (divisor_copy*dividend_copy);
end
endmodule
```

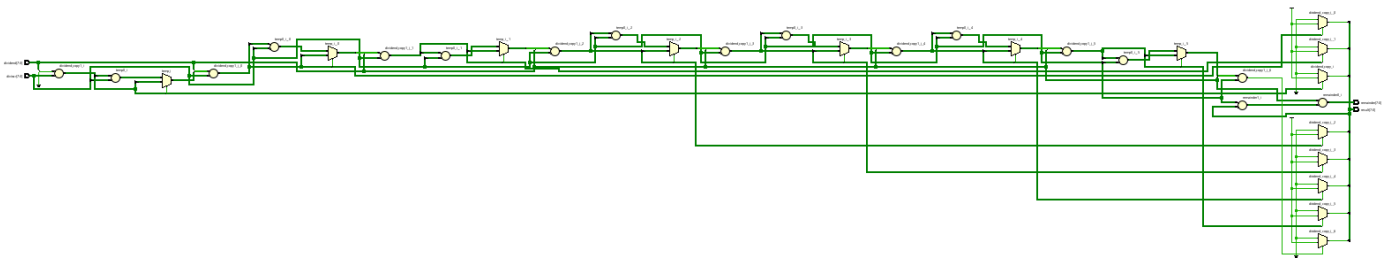
Testbench:

```
module fixed_point_division_tb;

    reg [7:0] divisor;
    reg [7:0] dividend;

    wire [7:0] remainder;
    wire [7:0] result;

    fixed_point_division uut (divisor, dividend, remainder, result);

    initial begin
        divisor = 13;
        dividend = 28;

        #100;

        divisor = 5;
        dividend = 25;

        #100
        divisor = 6;
        dividend = 37;
    end

    initial begin
        $monitor("Divisor: %d, Dividend: %d, Remainder: %d, Result: %d\n", divisor, dividend,remainder, result);
    end
endmodule
```

Simulation:



Schematic:



Synthesis report:

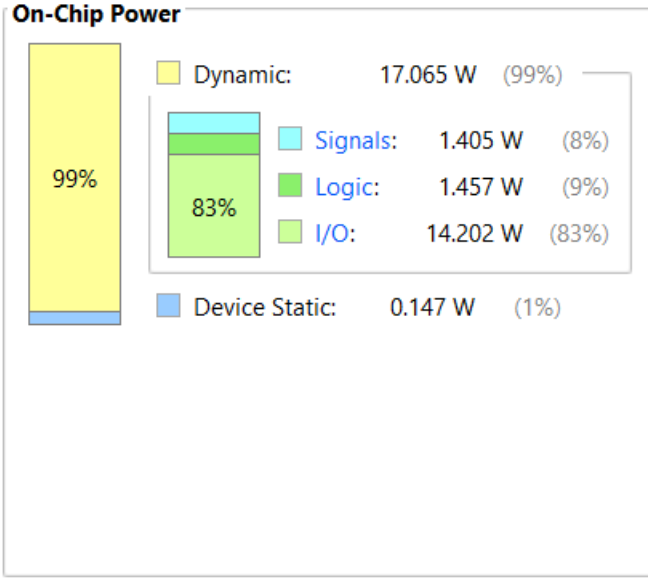
```
Start Writing Synthesis Report
--------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-------+------+
|      |Cell   |Count |
+------+-------+------+
|1     |CARRY4 |    36|
|2     |LUT1   |     7|
|3     |LUT2   |    75|
|4     |LUT3   |    49|
|5     |LUT4   |    11|
|6     |LUT5   |     4|
|7     |LUT6   |    23|
|8     |IBUF   |    16|
|9     |OBUF   |    16|
+------+-------+------+

Report Instance Areas:
+------+---------+-------+------+
|      |Instance |Module |Cells |
+------+---------+-------+------+
|1     |top      |       |   237|
+------+---------+-------+------+
---------------------------------
Finished Writing Synthesis Report
```

Power report:

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**17.212 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**57.4°C**
Thermal Margin:	27.6°C (14.5 W)
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



20.Master slave JK flip flop

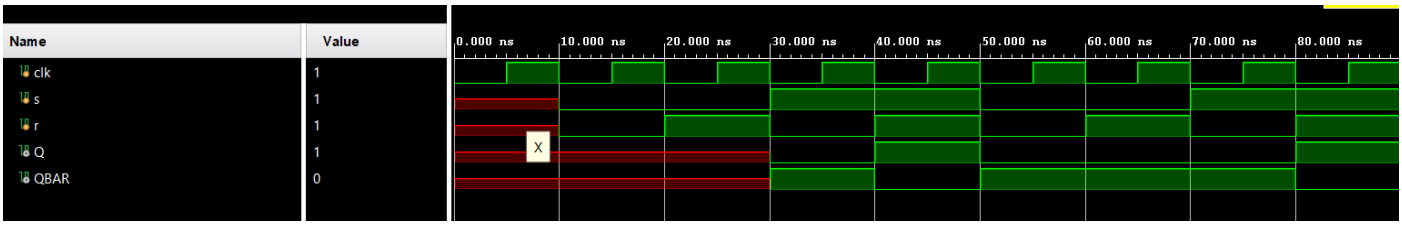
Verilog code:

```
module master_slave_ff(
 input clk,s,r,
 output Q,QBAR
    );

    wire w1,w2,w3,w4;
    wire sclk;

    assign sclk = ~clk;

    jk_flipflop master(clk,s,r,w1,w2);
    jk_flipflop slave(sclk,w1,w2,Q,QBAR);
endmodule

module jk_flipflop(
    input clk,
    input j,
    input k,
    output reg q,
    output reg qbar
    );

    always @ (posedge clk)
    begin

    case ({j,k})

       2'b00 : begin q <= q;  qbar<= ~q; end
       2'b01 : begin q <= 0;  qbar<=  1; end
       2'b10 : begin q <= 1;  qbar<=  0; end
       2'b11 : begin q <= ~q; qbar<=  q; end

     endcase
    end
endmodule
```

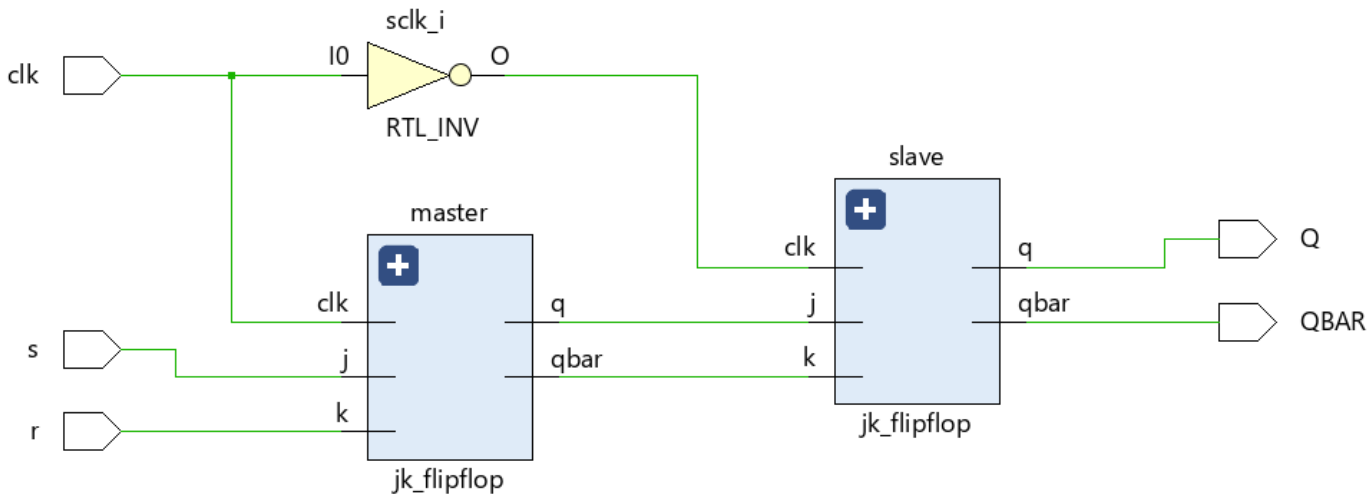
Testbench:

```
module master_slave_ff_tb(

    );
       reg clk;
        reg s;
        reg r;
        wire Q;
        wire QBAR;

        master_slave_ff uut(clk,s,r,Q,QBAR);

        initial begin
                $display("Time=%0t clk=%b s=%b r=%b Q=%b QBAR=%b", $time, clk, s, r, Q, QBAR);
         end

        initial begin
        clk=1'b0;
        forever #5 clk=~clk;
        end

        initial begin

       #10  s=1'b0;  r=1'b0;
       #10  s=1'b0;  r=1'b1;
       #10  s=1'b1;  r=1'b0;
       #10  s=1'b1;  r=1'b1;
       #10  s=1'b0;  r=1'b0;
       #10  s=1'b0;  r=1'b1;
       #10  s=1'b1;  r=1'b0;
       #10  s=1'b1;  r=1'b1;
       #10 $finish;
       end
endmodule
```

Simulation:



Schematic:



Synthesis report:

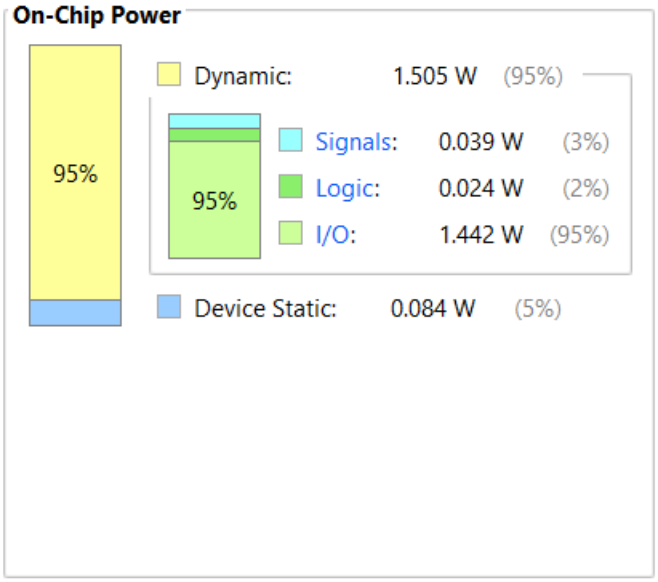
```
Start Writing Synthesis Report
---------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |BUFG |     1|
|2     |LUT1 |     1|
|3     |LUT3 |     4|
|4     |FDRE |     4|
|5     |IBUF |     3|
|6     |OBUF |     2|
+------+-----+------+

Report Instance Areas:
+------+---------+--------------+------+
|      |Instance |Module        |Cells |
+------+---------+--------------+------+
|1     |top      |              |    15|
|2     |  master |jk_flipflop   |     5|
|3     |  slave  |jk_flipflop_0 |     3|
+------+---------+--------------+------+
---------------------------------------
Finished Writing Synthesis Report : Time
```

Power report:

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**1.589 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**28.0°C**
Thermal Margin:	57.0°C (30.1 W)
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



21.Positive edge detector

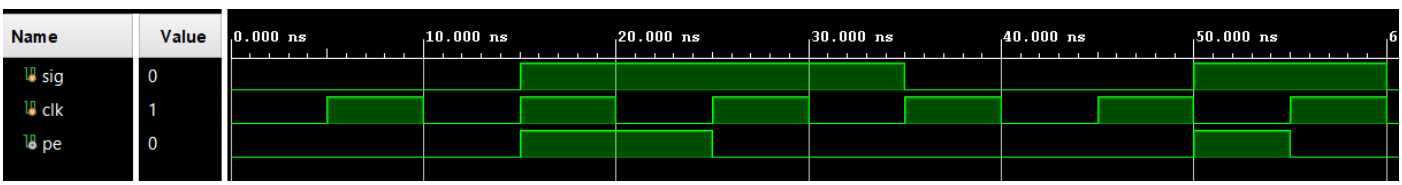
Verilog code:

```
module pos_edge_det (
        input sig,
        input clk,
         output pe
         );

    reg   sig_dly;

  always @ (posedge clk) begin
    sig_dly <= sig;
  end


  assign pe = sig & ~sig_dly;
endmodule
```

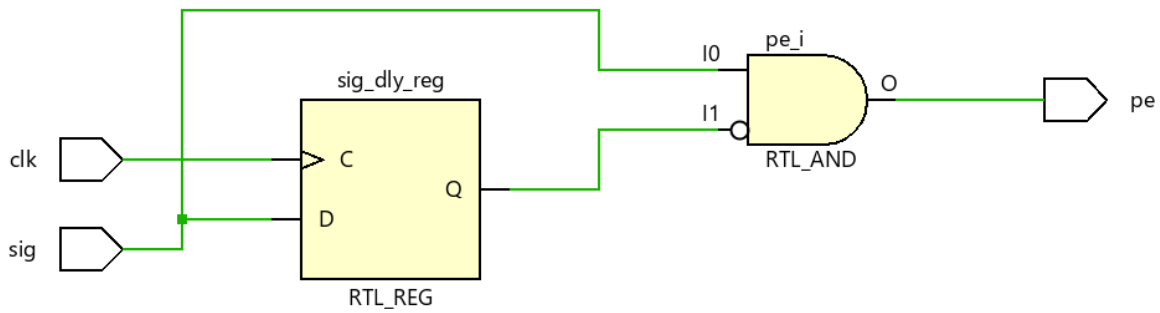
Testbench:

```
module pos_edge_det_tb;
    reg sig;
    reg clk;
    wire pe;
    pos_edge_det uut (sig,clk, pe);

    always #5 clk = ~clk;
    initial begin
        clk <= 0;
        sig <= 0;
        #15 sig <= 1;
        #20 sig <= 0;
        #15 sig <= 1;
        #10 sig <= 0;
        #20 $finish;
    end

    initial begin
        $dumpvars;
      $dumpfile("dump.vcd");
    end
endmodule
```

Simulation:



Schematic:



Synthesis report:

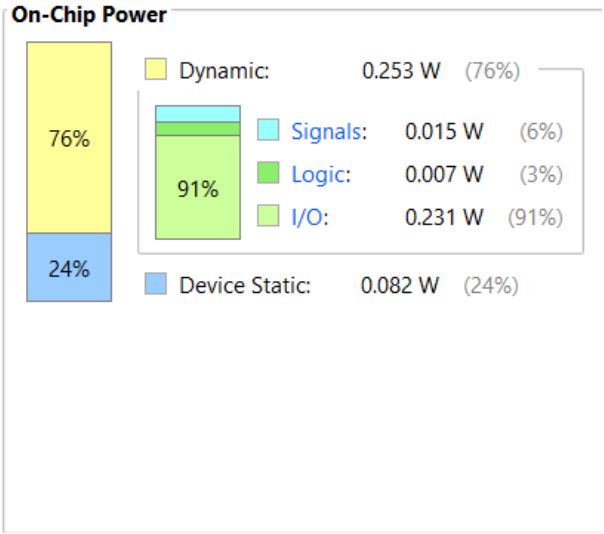
```
Start Writing Synthesis Report
-------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |BUFG |     1|
|2     |LUT2 |     1|
|3     |FDRE |     1|
|4     |IBUF |     2|
|5     |OBUF |     1|
+------+-----+------+

Report Instance Areas:
+------+---------+-------+------+
|      |Instance |Module |Cells |
+------+---------+-------+------+
|1     |top      |       |     6|
+------+---------+-------+------+
-------------------------------------
Finished Writing Synthesis Report
```

Power report:

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**0.335 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**25.6°C**
Thermal Margin:	59.4°C (31.3 W)
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



22.BCD adder

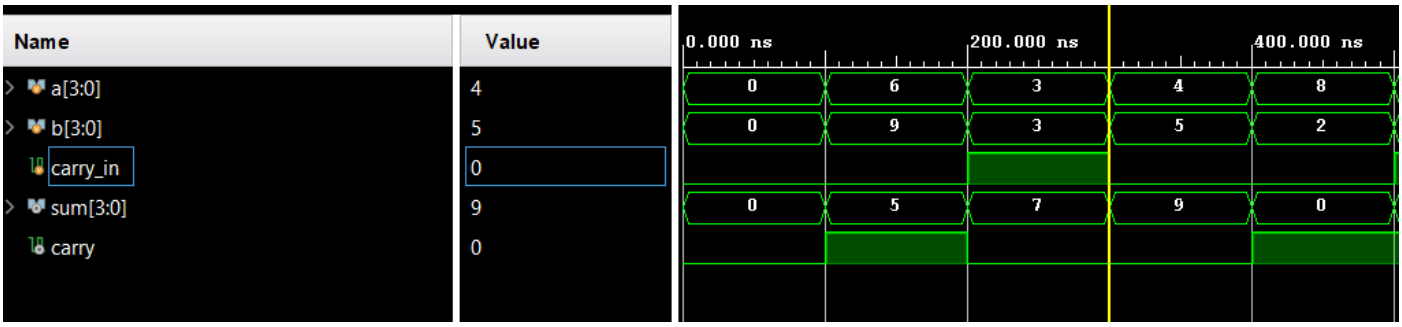
Verilog code:

```
module bcd_adder(
a,b,carry_in,sum,carry
    );
    input [3:0] a,b;
    input carry_in;
    output [3:0] sum;
    output carry;

    reg [4:0] sum_temp;
    reg [3:0] sum;
    reg carry;

    always @(a,b,carry_in)
    begin
        sum_temp = a+b+carry_in;
        if(sum_temp > 9)    begin
            sum_temp = sum_temp+6;
            carry = 1;
            sum = sum_temp[3:0];    end
        else    begin
            carry = 0;
            sum = sum_temp[3:0];
        end
    end

endmodule
```

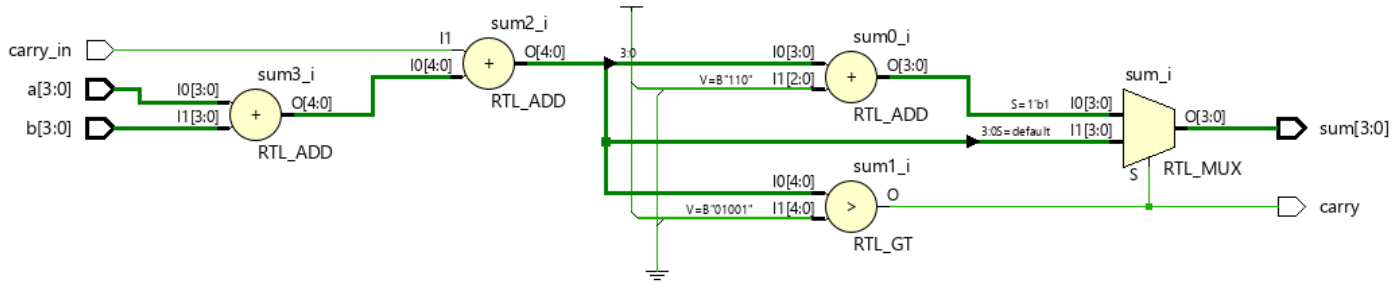
Testbench:

```
module bcd_adder_tb(
    );
     reg [3:0] a;
    reg [3:0] b;
    reg carry_in;

    wire [3:0] sum;
    wire carry;

    bcd_adder uut (
        .a(a),
        .b(b),
        .carry_in(carry_in),
        .sum(sum),
        .carry(carry)
    );

    initial begin

        a = 0;  b = 0;  carry_in = 0;   #100;
        a = 6;  b = 9;  carry_in = 0;   #100;
        a = 3;  b = 3;  carry_in = 1;   #100;
        a = 4;  b = 5;  carry_in = 0;   #100;
        a = 8;  b = 2;  carry_in = 0;   #100;
        a = 9;  b = 9;  carry_in = 1;   #100;
    end
endmodule
```

Simulation:



Schematic:



Synthesis report:

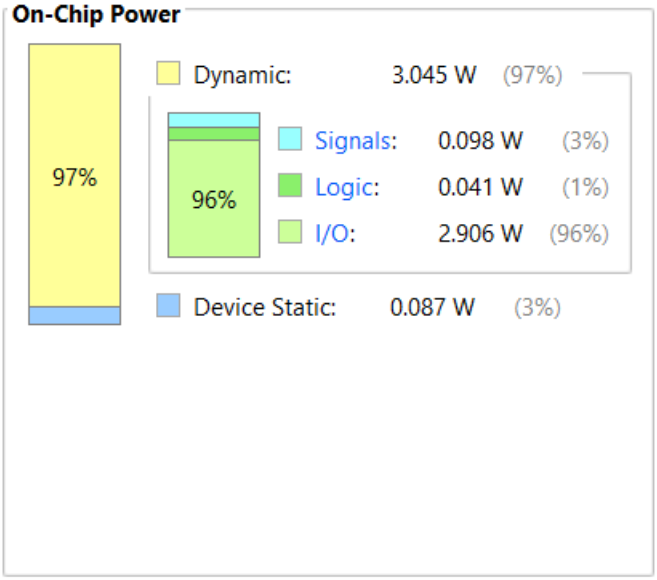
```
Start Writing Synthesis Report
-------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |LUT3 |     1|
|2     |LUT5 |     2|
|3     |LUT6 |     4|
|4     |IBUF |     9|
|5     |OBUF |     5|
+------+-----+------+

Report Instance Areas:
+------+---------+-------+------+
|      |Instance |Module |Cells |
+------+---------+-------+------+
|1     |top      |       |    21|
+------+---------+-------+------+
-------------------------------
Finished Writing Synthesis Report
```

Power report:

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**3.133 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**30.9°C**
Thermal Margin:	54.1°C (28.5 W)
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



23.4-Bit carry select adder

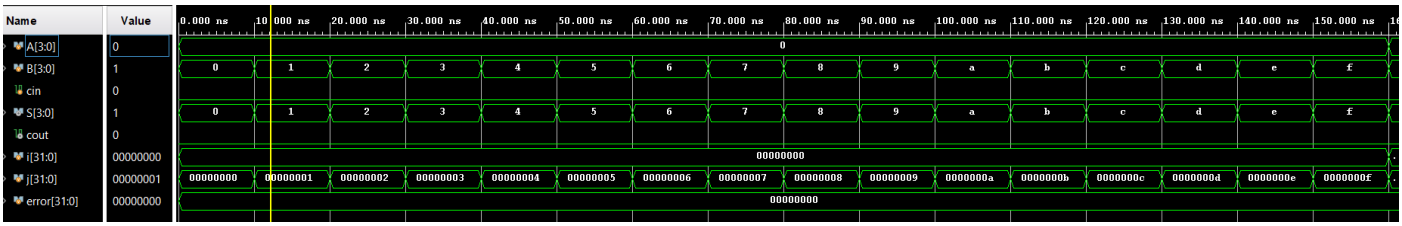
Verilog code:

```
module carry_select_adder
        (   input [3:0] A,B,
            input cin,
            output [3:0] S,
            output cout
            );


wire [3:0] temp0,temp1,carry0,carry1;

//for carry 0
fulladder fa00(A[0],B[0],1'b0,temp0[0],carry0[0]);
fulladder fa01(A[1],B[1],carry0[0],temp0[1],carry0[1]);
fulladder fa02(A[2],B[2],carry0[1],temp0[2],carry0[2]);
fulladder fa03(A[3],B[3],carry0[2],temp0[3],carry0[3]);

//for carry 1
fulladder fa10(A[0],B[0],1'b1,temp1[0],carry1[0]);
fulladder fa11(A[1],B[1],carry1[0],temp1[1],carry1[1]);
fulladder fa12(A[2],B[2],carry1[1],temp1[2],carry1[2]);
fulladder fa13(A[3],B[3],carry1[2],temp1[3],carry1[3]);

//mux for carry
multiplexer2 mux_carry(carry0[3],carry1[3],cin,cout);
//mux's for sum
multiplexer2 mux_sum0(temp0[0],temp1[0],cin,S[0]);
multiplexer2 mux_sum1(temp0[1],temp1[1],cin,S[1]);
multiplexer2 mux_sum2(temp0[2],temp1[2],cin,S[2]);
multiplexer2 mux_sum3(temp0[3],temp1[3],cin,S[3]);

endmodule
```

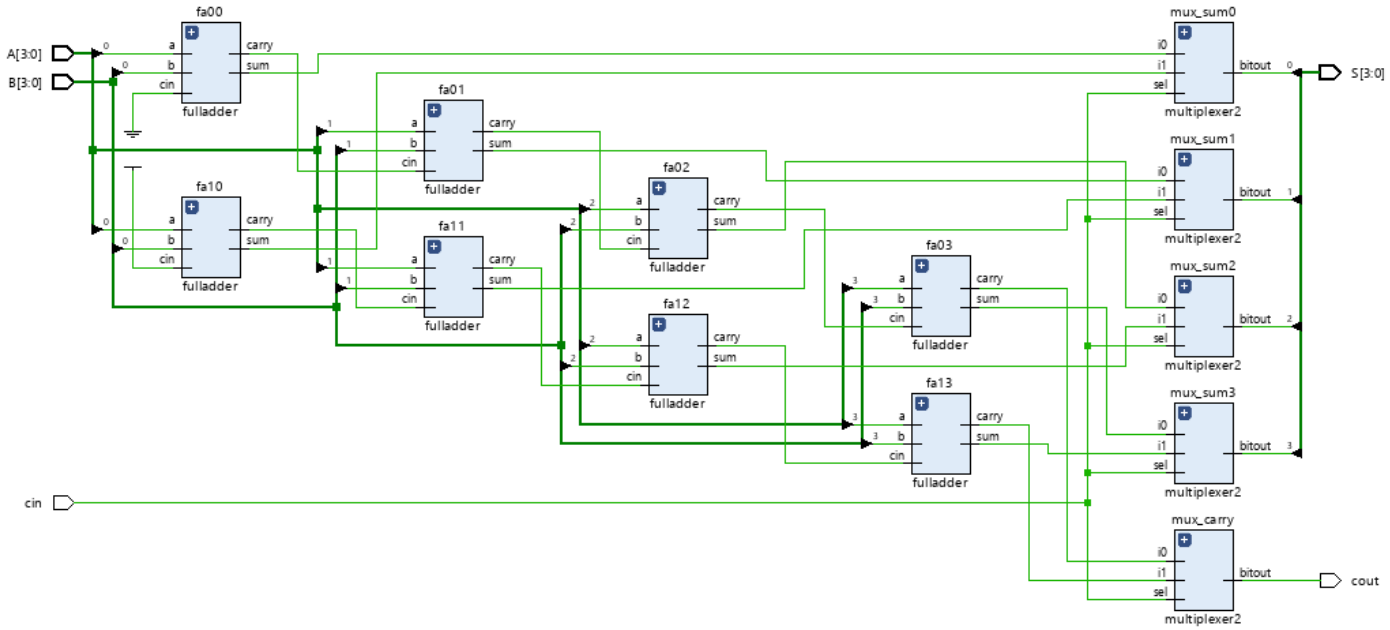
Testbench:

```
module fulladder
        (   input a,b,cin,
            output sum,carry
            );

assign sum = a ^ b ^ cin;
assign carry = (a & b) | (cin & b) | (a & cin);

endmodule


module multiplexer2
        (   input i0,i1,sel,
            output reg bitout
            );

always@(i0,i1,sel)
begin
if(sel == 0)
    bitout = i0;
else
    bitout = i1;
end

endmodule
```

Simulation:



Schematic:



Synthesis report:

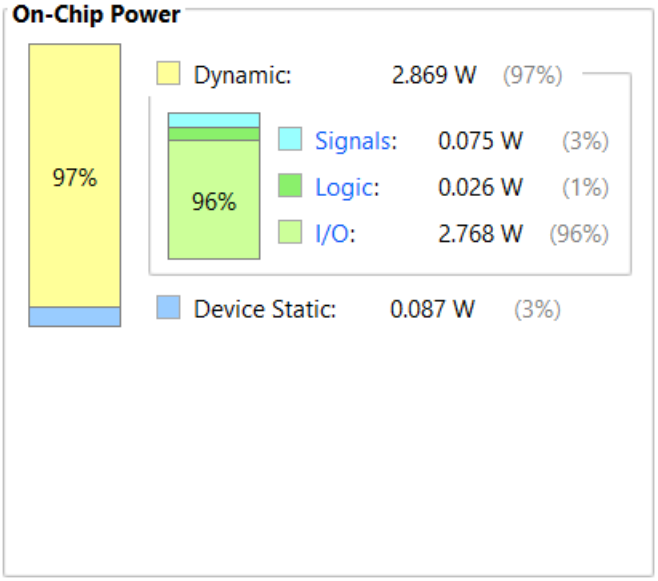
```
Start Writing Synthesis Report
--------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |LUT3 |     2|
|2     |LUT5 |     4|
|3     |IBUF |     9|
|4     |OBUF |     5|
+------+-----+------+

Report Instance Areas:
+------+---------+-------+------+
|      |Instance |Module |Cells |
+------+---------+-------+------+
|1     |top      |       |    20|
+------+---------+-------+------+
--------------------------------
Finished Writing Synthesis Report
```

Power report:

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**2.956 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**30.6°C**
Thermal Margin:	54.4°C (28.7 W)
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



24.Moore FSM 1010 sequence detector

Verilog code:

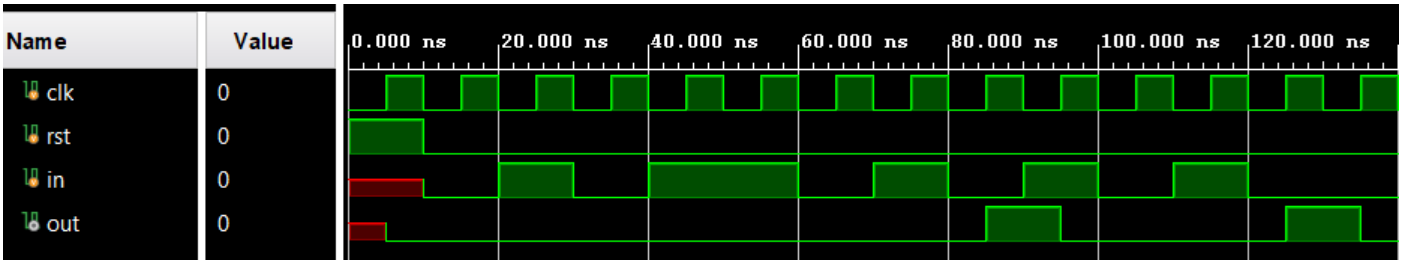
```
module moore_fsm_1010(
    input clk,
    input rst,
    input in,
    output reg out
    );

    reg [2:0]state,next_state;
    parameter s0 = 3'b001;
    parameter s1 = 3'b010;
    parameter s2 = 3'b011;
    parameter s3 = 3'b100;
    parameter s4 = 3'b101;

    always @ (state or in)
     begin
     case (state)
       s0: if (in == 1'b1)
              begin
             next_state = s1;
              out=1'b0;
              end
          else
              begin
              next_state = s0;
              out=1'b0;
              end

        s1: if (in == 1'b0)
              begin
              next_state = s2;
              out=1'b0;
              end
            else
              begin
              next_state = s1;
              out=1'b0;
              end
```

```
        s2: if (in == 1'b1)
                begin
                next_state = s3;
                out=1'b0;
                end
            else
                begin
                next_state = s0;
                out=1'b0;
                end
         s3: if (in == 1'b0)
              begin
              next_state = s4;
              out=1'b0;
              end
            else
              begin
              next_state = s1;
              out=1'b0;
              end
          s4: if (in == 1'b0)
              begin
              next_state = s0;
              out=1'b1;
              end
            else
              begin
              next_state = s1;
              out=1'b1;
              end
          default: next_state = s0;
       endcase
     end
     always@(posedge clk)
                begin
                 if (rst)
                   state <= s0;
                 else
                   state <= next_state;
                end
endmodule
```

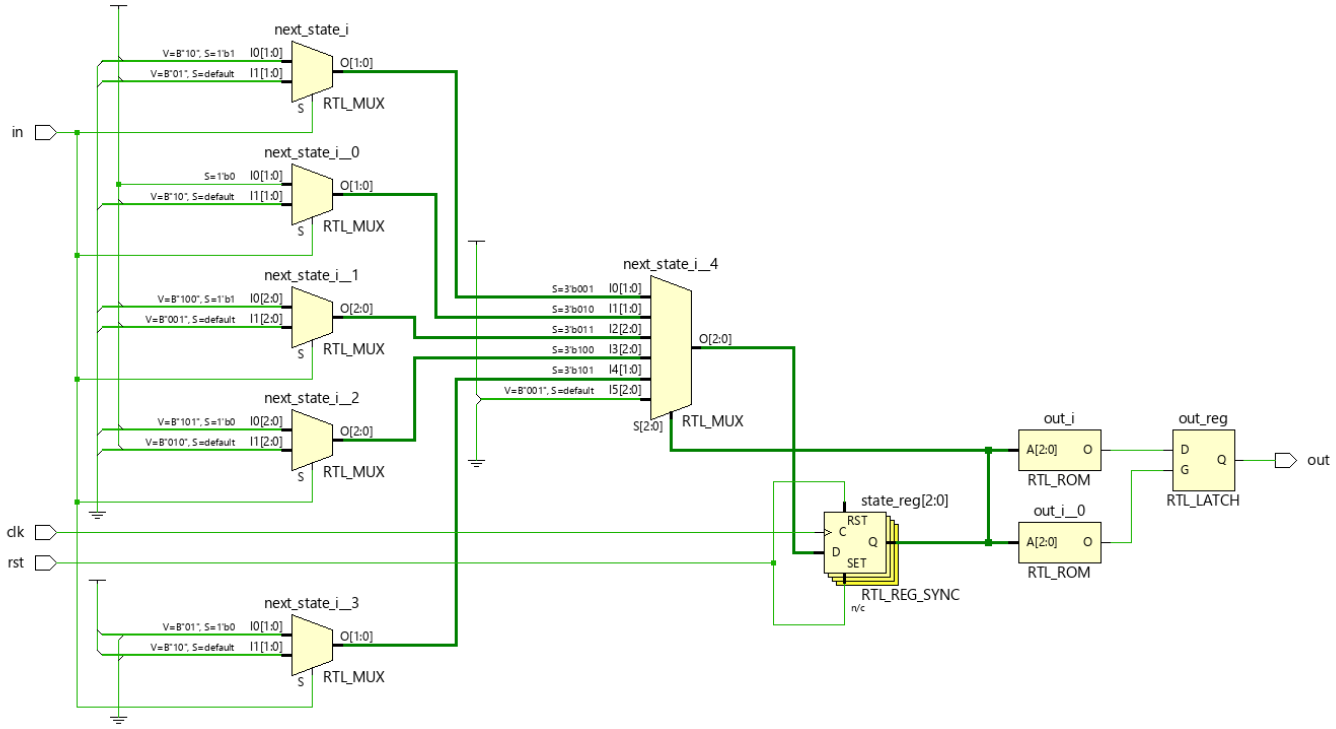
Testbench:

```
module moore_fsm_1010_tb(
    );
    reg clk;
    reg rst;
    reg in;
    wire out;

    moore_fsm_1010 uut(clk,rst,in,out);
    initial begin
    $monitor($time," | rst=%b | in=%b | out=%b",rst,in,out );
    end
    initial begin
    clk = 1'b0;
    forever #5 clk = ~clk;
    end

    initial begin
      rst = 1'b1;
     #10 rst = 1'b0; in=1'b0;
     #10  in=1'b1;
     #10  in=1'b0;
     #10  in=1'b1;
     #10  in=1'b1;
     #10  in=1'b0;
     #10  in=1'b1;
     #10  in=1'b0;
     #10  in=1'b1;
     #10  in=1'b0;
     #10  in=1'b1;
     #10  in=1'b0;
     #10  in=1'b0;

        end

endmodule
```

Simulation:



Schematic:



Synthesis report:

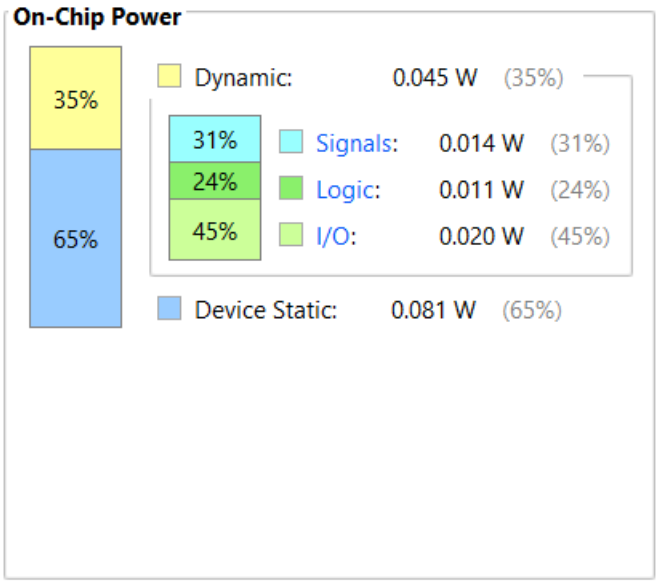
```
Start Writing Synthesis Report
--------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |BUFG |     1|
|2     |LUT2 |     3|
|3     |LUT4 |     1|
|4     |LUT5 |     2|
|5     |FDRE |     4|
|6     |FDSE |     1|
|7     |LD   |     1|
|8     |IBUF |     3|
|9     |OBUF |     1|
+------+-----+------+

Report Instance Areas:
+------+---------+-------+------+
|      |Instance |Module |Cells |
+------+---------+-------+------+
|1     |top      |       |    17|
+------+---------+-------+------+
--------------------------------
Finished Writing Synthesis Report
```

Power report:

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**0.126 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**25.2°C**
Thermal Margin:	59.8°C (31.5 W)
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



25.N:1 MUX

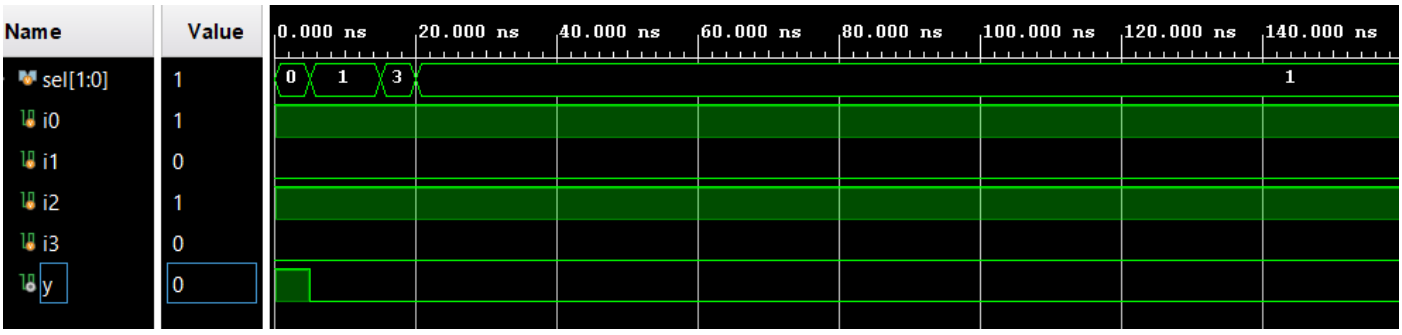
Verilog code:

```
module mux_4_1(
  input [1:0] sel,
  input  i0,i1,i2,i3,
  output reg y);

  always @(*) begin
    case(sel)
      2'h0: y = i0;
      2'h1: y = i1;
      2'h2: y = i2;
      2'h3: y = i3;
      default: $display("Invalid sel input");
    endcase
  end
endmodule
```

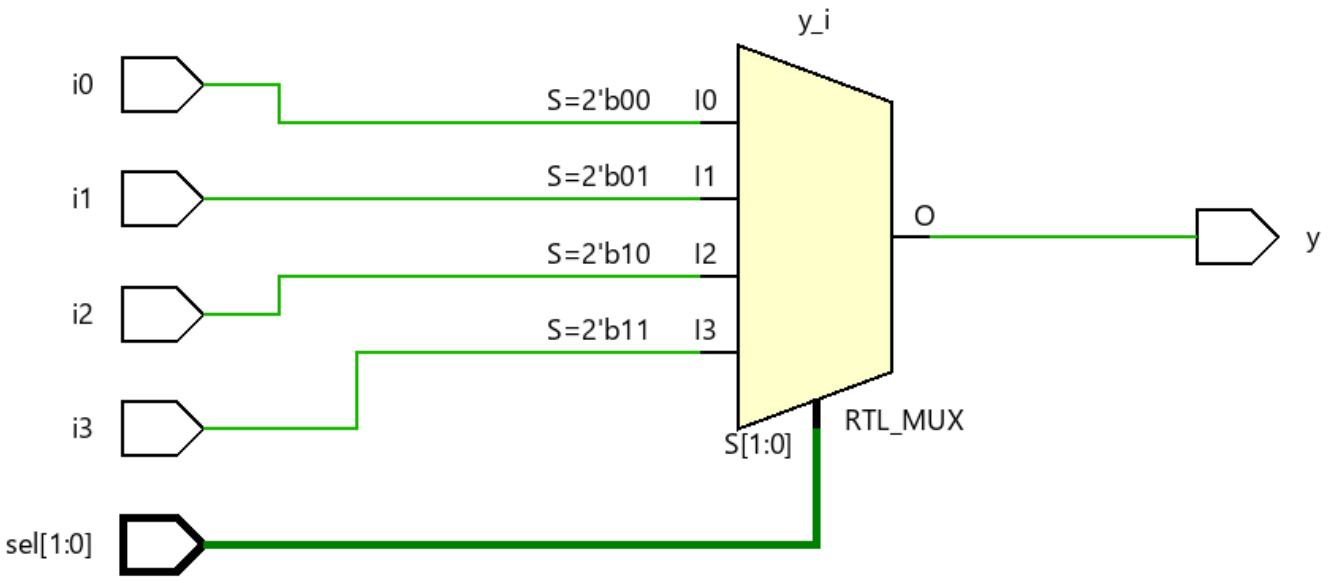
Testbench:

```
module tb;
  reg [1:0] sel;
  reg i0,i1,i2,i3;
  wire y;

  mux_4_1 mux(sel, i0, i1, i2, i3, y);

  initial begin
    $monitor("sel = %b -> i3 = %0b, i2 = %0b ,i1 = %0b, i0 = %0b -> y = %0b", sel,i3,i2,i1,i0, y);
    {i3,i2,i1,i0} = 4'h5;
    repeat(6) begin
      sel = $random;
      #5;
    end
  end
endmodule
```

Simulation:



Schematic:



Synthesis report:

```
Start Writing Synthesis Report
---------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |LUT6 |     1|
|2     |IBUF |     6|
|3     |OBUF |     1|
+------+-----+------+

Report Instance Areas:
+------+---------+-------+------+
|      |Instance |Module |Cells |
+------+---------+-------+------+
|1     |top      |       |     8|
+------+---------+-------+------+
---------------------------------
Finished Writing Synthesis Report
---------------------------------
```

Power report:

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**0.535 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**26.0°C**
Thermal Margin:	59.0°C (31.1 W)
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity