Bangladesh University of Engineering and Technology

Department of Computer Science and Engineering

Course: CSE 206
Digital Logic Design Sessional
Experiment No. 5

Topic: Encoder and Decoder Circuits.

Design and Implement the following problems:

1. Using basic gates, design and implement a 4 to 2 priority encoder with the priority of the input data bits ($D_3D_2D_1D_0$) as given below. Here, $D_x > D_y$ implies D_x has higher priority than D_y.

Lab Group #	Priority
1	D2 > D0 > D1 > D3
2	D2 > D3 > D1 > D0
3	D0 > D1 > D3 > D2
4	D3 > D2 > D0 > D1
5	D1 > D2 > D0 > D3
6	D0 > D3 > D1 > D2

2. Implement the function given below using <u>two</u> 3 × 8 decoders (IC - 74138) and basic gates as required.
   a) f(W,X,Y,Z) = ∑(0,2,4,11,14)
   b) f(W,X,Y,Z) = Π(1,2,4,7,12,15)

Answer the following question:

1. Implement a circuit which generates the 1's complement of a 2-bit number when the controller bit is 0, and the 2's complement of that number when the controller bit is 1. You can use <u>only one</u> 3 × 8 decoder (IC - 74138) and basic gates as required.
2. Using IC – 74154, design a 2-bit comparator to compare two 2-bit numbers *X* and *Y*. The circuit should provide three output lines to indicate *X>Y, X=Y, X<Y*.

Report:

For each of the problems/questions report should cover:

- Problem definition.
- Required equation in minimized form with necessary steps and corresponding Truth table.
- Circuit diagram with pin number.
- Required instruments for implementation.

Moreover, include the following sections to your report.

- Answer to the questions.
- Observations/Discussions