Bangladesh University of Engineering and Technology

Department of Computer Science and Engineering

Course: CSE 206
Digital Logic Design Sessional

Experiment No. 7

Topic: Design and Implementation of Latch and Flip-Flop circuits.

Implement the following problems:

1. Design and implement a gated (i.e., controlled) S-R latch using only NAND gates with asynchronous PRESET (active low) and CLEAR (active low).

2. Extend the circuit implemented in (1) to make a negative-edge triggered master-slave D flip-flop with asynchronous PRESET (active low) and CLEAR (active low) using only NAND gates. Use the circuit of (1) as the slave part.

Note: IC 7400 (Quad two-input NAND) and IC 7410 (Triple three-input NAND) gates may be used as part of this experiment.

Answer the following question:

1. Design sequential circuits to transform a J-K FF to D FF and T FF.
2. Design sequential circuits to transform a T FF and a D FF to J-K FF.

Report:

For each of the problems/questions report should cover:

- Problem specification.
- Required instruments.
- Characteristic Table & Excitation Table.
- Function minimization (if required)
- Circuit diagram with pin number.