

SMTInterpol

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Description

SMTInterpol is an SMT solver written in Java and available under LGPL v3. It supports the quantifier-free combination of the theories of uninterpreted functions, linear arithmetic over integers and reals, and arrays. Furthermore it can produce models, proofs, unsatisfiable cores, and interpolants. The solver reads input in SMTLIB format. It includes parsers for DIMACS, AIGER, and SMTLIB version 1.2 and 2.

The solver uses variants of standard algorithms for CNF conversion [PG86], congruence closure [NO05], Simplex [DdM06] and branch-and-cut for integer arithmetic [CH15a, DDA09]. The array decision procedure is based on *weak equivalences* [CH15b]. Theory combination is performed based on partial models produced by the theory solvers [dMB08].

The main focus of SMTInterpol is the application track where the incremental usage of the solver is required. This track simulates the typical application of SMTInterpol where a user asks multiple queries. The main focus of the development team of SMTInterpol is the interpolation engine [CHN13]. This makes it useful as a backend for software verification tools. In particular, UltimateAutomatizer, the winner of the SV-COMP 2016, uses SMTInterpol.

Competition Version

The version submitted to the SMT-COMP 2016 is a preliminary release of version 2.2. This release will include quantifier-free interpolation for the theory of arrays which is still missing in the current solver.

Further information about SMTInterpol can be found at

<http://ultimate.informatik.uni-freiburg.de/smtinterpol/>

The sources are available via GitHub

<https://github.com/ultimate-pa/smtinterpol>

Logics, Tracks and Magic Number

SMTInterpol participates in all tracks: the main track, the application track, and the unsat core track. It supports the logics QF_UF, QF_IDL, QF_RDL, QF_LIA, QF_LRA, QF_LIRA, QF_AX and every combinations of these logics: QF_ALIA, QF_AUFLIA, QF_AUFLIRA, QF_UFIDL, QF_UFLIA, QF_UFLRA.

Magic Number: 3 536 504

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