

Free/Open-source Hardware

An overview on the Open-source philosophy and Open Hardware state of the art

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Introduction

Free (as in Freedom)/Open-source Hardware

Hardware directives or designs that can be freely:

- Used
- Studied
- Shared
- Improved

FO-S Hardware can be observed in many variations such as:

- Electronics (the focus of this talk)
- Mechatronics (3D printers, Prosthetics, etc.)
- And many other

Introduction-Timeline and Licenses

- Hit some licenses here like the OHL etc. be fast we want to go to the eng. meat

Why Free/Open Hardware?

From the researcher/developer standpoint:

- More tools available that are:
 - Free (as in freedom) to use
 - Documented
 - Open for study
 - Overall, **adaptable**
- Community spearheaded
 - *Linus Law*: “Given enough eyeballs, all bugs are shallow”

From the adept/costumer standpoint:

- Transparency and Respect for the user
- Reparability
- Upgradability

Open Hardware State of the Art

We can split open hardware projects into seven main groups:

- Tools for Hardware Development*
- Instruction Set Architectures (ISAs)
- Systems-on-Chip (SoC)
- Micro-controllers
- Embedded Systems
- Single-Board computers
- Other Computing Systems
- FPGAs

Tools for Hardware Development

Open ISAs

Directives for processing operations (i.e. structure and set of instructions)

Talk about AVR and the other Berkley ISAs up until RISC-V.

Cascading effect for opening other technologies.

Digital system designs for implementing into FPGAs or silicon: - Processors
VexRISC-V for example.

Pinecil

Microcontrollers

Microcontrollers are computing systems that contain a microprocessor, that can run a simple deterministic Operating System (such as a RTOS) or a simply flashed program, making them ideal for low-power and low-cost IoT integration and tasks.

Arduino

Launched in Italy in 2005 it is arguably the most well known microcontroller and Open Hardware Project as of 2023. The initial project goal was to create simple, low cost tools for creating digital projects by non-engineers, which has since evolved into the production of , which since have been replicated multiple times

Most Arduino boards have either :

- A closed-design Atmel AVR microprocessor (built with a open modified-Harvard ISA)
 - Bulk of the Arduino market
 - Simple to use
 - Low-cost
- A ARM-Cortex (Since Revision 4)

The Seed project

HiFive Boards

Single-Board Computers

Single-Board Computers (SBCs) are full computing systems, running an Operating System (such as Linux-based OS's) and providing above-microcontroller performance at a relative low-power and low-cost. Therefore they can be designated for more complex IoT and Embedded functions and simple Desktop operations.

- **Raspberry Pi** (2012-present): Partial Open board design, Closed Processor and ISA (ARM)
- **VisionFive** (2021-present): Open board design, Closed Processor, Open ISA (RISC-V)
- **MangoPi** (2022): Open board design, Closed Processor Design, Open ISA (RISC-V)
- **BeagleV®-Ahead** (2023): Open board design, Open Processor Design, Open ISA (RISC-V)
- **Lichee Pi 4A** (2023): Open board design, Open Processor Design, Open ISA (RISC-V)

Single-Board Computers

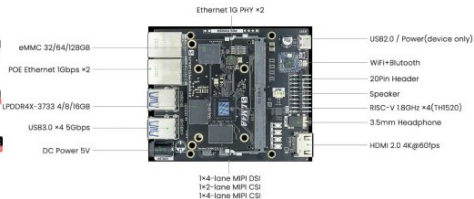
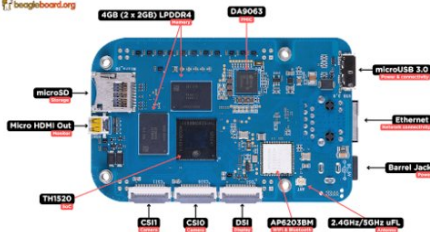
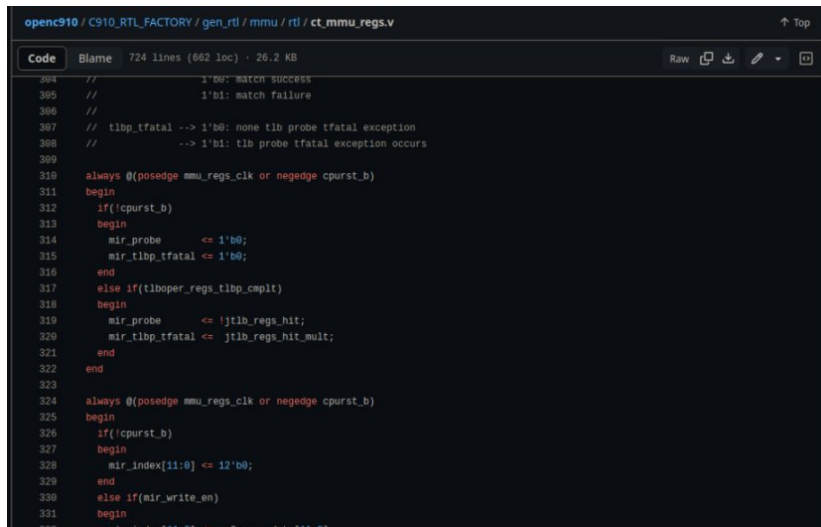


Figure 1: BeagleV-Ahead and Lichee Pi 4A

C910 processor



The image shows a screenshot of a code editor displaying a Verilog design file. The file path at the top is 'openc910 / C910_RTL_FACTORY / gen_rtl / mmu / rtl / ct_mmu_regs.v'. The editor shows lines 304 through 332 of the code. The code is a Verilog module for the C910 processor's mmu registers. It includes comments for match success/failure and tlb probe fatal exceptions. It contains two 'always' blocks triggered by 'posedge mmu_regs_clk or negedge cpurst_b'. The first block handles mir_probe and mir_tlbp_tfatal signals based on tlboper_regs_tlbp_cmplt. The second block handles mir_index[11:0] and mir_write_en signals. The code is syntax-highlighted with colors for keywords, comments, and identifiers.

```
openc910 / C910_RTL_FACTORY / gen_rtl / mmu / rtl / ct_mmu_regs.v
Code Blame 724 lines (662 loc) · 26.2 KB
304 //          1'b0: match success
305 //          1'b1: match failure
306 //
307 // tlbp_tfatal --> 1'b0: none tlb probe tfatal exception
308 //          --> 1'b1: tlb probe tfatal exception occurs
309
310 always @(posedge mmu_regs_clk or negedge cpurst_b)
311 begin
312     if(!cpurst_b)
313     begin
314         mir_probe      <= 1'b0;
315         mir_tlbp_tfatal <= 1'b0;
316     end
317     else if(tlboper_regs_tlbp_cmplt)
318     begin
319         mir_probe      <= !jtlb_regs_hit;
320         mir_tlbp_tfatal <= jtlb_regs_hit_mult;
321     end
322 end
323
324 always @(posedge mmu_regs_clk or negedge cpurst_b)
325 begin
326     if(!cpurst_b)
327     begin
328         mir_index[11:0] <= 12'b0;
329     end
330     else if(mir_write_en)
331     begin
332         mir_index[11:0] <= mir_write_data[11:0];
333     end
334 end
```

Figure 2: Verilog Design files for the C910 processor

FPGAs

Field-Programmable Gate Arrays are the smallest unit for reconfigurable hardware:

- A mesh of CLBs (Configurable Logic Blocks) containing LUTs (Look-Up tables) allows hardware-level reconfigurability
 - Look-Up Tables are small memory devices that contain the logic outputs for different logic inputs
- The mesh then interacts with DSPs (Digital Signal Processor)
- The FPGA can then be integrated into a board to expand on the I/O capabilities

As of now most Open-Hardware FPGA boards are based on:

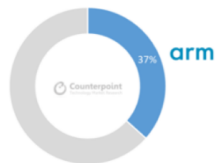
- Lattice's ICeStorm designed devices:
 - ICe40 boards
 - ECP5 -Microchip PolarFire devices:
 - BeagleV®-Fire

Roadmap

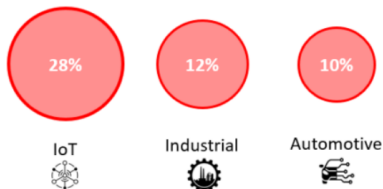
Semiconductor IP market size, 2020 vs 2025



ARM dominates global pure play IP market with 37% share



RISC-V Penetration Rate by 2025



Advantages RISC-V offers



So you want to develop F-OS Hardware?

Conclusion

To sum up here are some bullet points that you hopefully retained from this presentation:

- What is Free and Open Hardware
- Basic notions on the presented technologies
- Advantages of opening hardware designs