

Introductory Lab

Please answer the questions below and upload on fenix-projects your final report and your Vivado+Vitis design files of the matprod PS+PL system (as indicated in the final section).

Part 1. Dot product using axil_macc IP

1. Consider the C-based synthesis of the axil_macc IP.
 - a) Indicate the performance (latency and minimum clock period) estimates for your IP. How many clock cycles does the synthesized multiplier take?
 - b) List the main I/O ports of your IP and relate them to the AXI-Lite interface channels.
2. Consider the C/RTL co-simulation of the axil_macc IP and the RTL waveforms obtained.
 - a) Explain briefly how the AXI-Lite interface works and which AXI-Lite signals are active when the input data and control values are written to the IP, for the first multiplication-accumulation of the simulation.
 - b) Indicate at which time the read transaction of the first partial result value is accomplished. What are the signals (and signal values) that define when the transfer takes place?
 - c) Indicate at which time the read transaction of the final **done** control signal is accomplished. What are the signals (and signal values) that define this transaction?
3. Consider your PS+PL system
 - a) Which base address has been assigned to the axil_macc IP?
 - b) Indicate the number (total and per component) of resources needed to implement your PL design (in terms of LUTs, FFs and DSPs).
 - c) Compare the real resource consumption of the axil_macc IP with the high-level estimate (from Vitis HLS).
 - d) Could your PL system use a faster clock frequency? Justify briefly.

Part 2. Matrix product IP

4. Consider the HLS matprod IP for full matrix multiplication, with an AXI-Lite interface using 3 BRAM_36K = 6 BRAM_18K local memories. Consider the matrix elements as 32-bit integers. In one execution, the new IP does a full matrix multiplication. The dimensions of the matrices are configurable, up to the defined MEM_SIZE (per matrix).

a) Do a C/RTL Co-simulation, using the 4×4 matrices in file m4.bin (add the input matrix file as a project testbench file) and using MEM_SIZE = 16.

Indicate at which time the read transaction of the data read of the last element of the result matrix is accomplished.

Implement the IP (using MEM_SIZE = 1024) in a PS+PL system.

b) Indicate the number (total and per component) of resources needed to implement the PL part of the design.

c) Compare the real resource consumption of the axil_matprod IP with the high-level estimate (from Vitis HLS).

d) Estimate the maximum clock frequency that can be used in the PL.

Complete the C application to execute the matrix multiplication on your HW/SW system.

Add a function to compare the results between the software-only and the HW/SW application.

Place all the sections of your program on the OCM.

e) Measure the execution time of the HW/SW application (executing on the Zynq device on your board) for 25×25 matrices.

f) Compare the measured performance with that of the software-only 25×25 matrix multiplication.

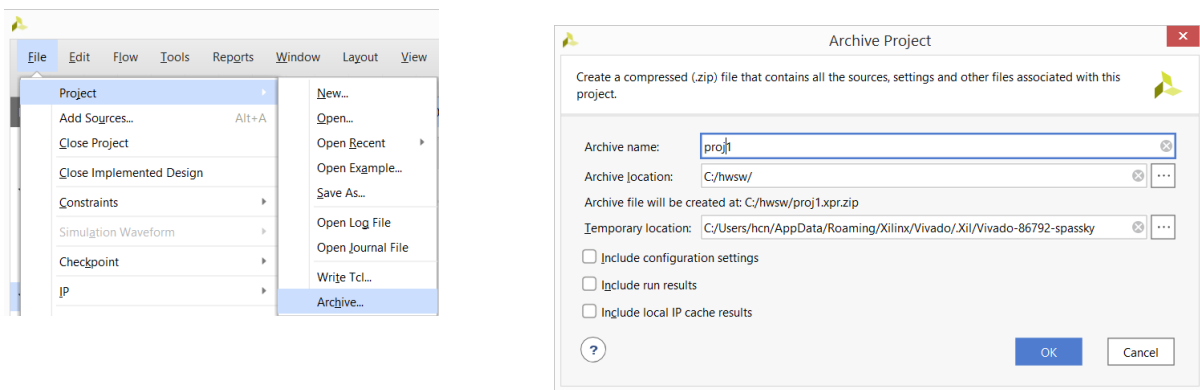
5. Estimate the performance improvements that could be achieved if the input matrix elements were 8-bit integers.

Electronic delivery

Electronic delivery must be made with a single zip file including:

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Report*.pdf (simple pdf report answering the questions above, in single-column report format),  
proj*.xpr.zip, (archive of the Vivado design of the matprod PS+PL system)  
hls: *.cpp, (all HLS specification and testbench files for the matprod IP)  
      *.h,  
      tb*.cpp  
vitis: *.c *.h (C application for the HW/SW system)  
      lscript.ld
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The Vivado design archive must be generated using the command **File->Project->Archive** in Vivado, and deactivating the additional inclusions, for the archive to be as small as possible (~20MB):



The uploaded zip file should not include other files or use overly complex folder structures that make it difficult to access the content.

Each group must do a presential project demonstration for evaluation at the lab. All elements of the group must be present at the lab.