Project 3 – MIPS simulator

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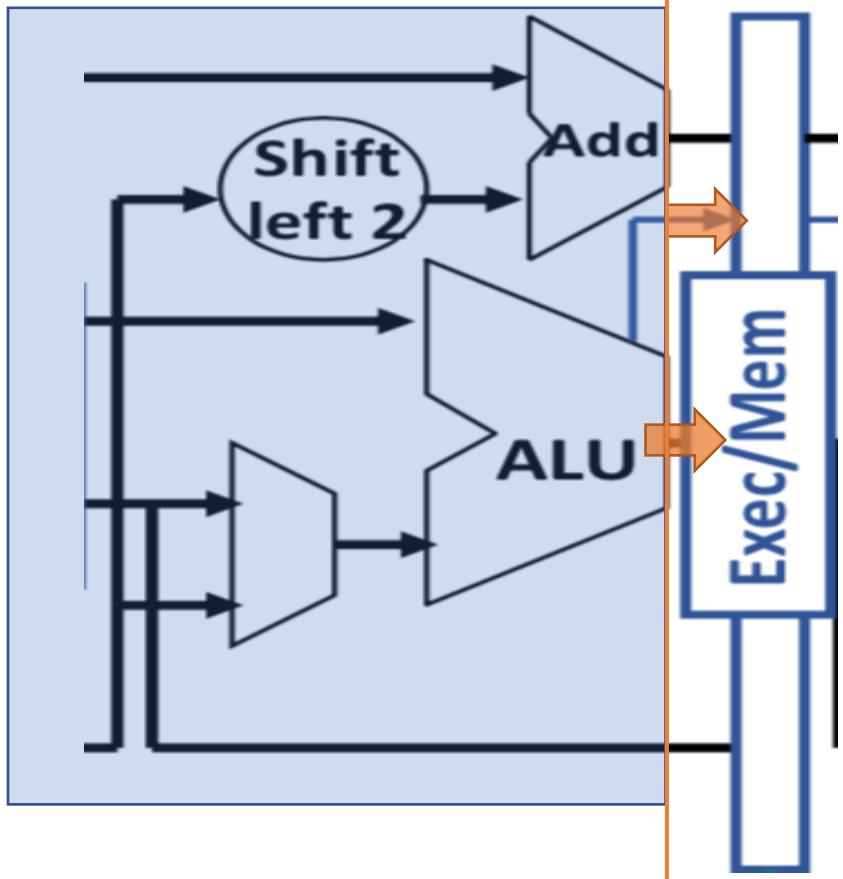
- pipeline design
- hazard detection
- demo show

pipeline design

- do()
- excute a result
- all changes to variable0



- transfer()
- put result into latch
- variable = variable0

pipeline design

- Implement parallelism with a sequential program

✓ All do() of five stages done ⟶ transfer()

- RAW strategy

✓ change the order of .do(): put WB.do() higher

Hazard detection – Control hazard

- ✓ insert NOP
- ✓ branch to expected instruction

	IF stage	ID stage	EX stage	MEM stage	WB stage
Cycle0	ins0(beq)	NOP	NOP	NOP	NOP
Cycle1	NOP	decode0	NOP	NOP	NOP
Cycle2	ins branch	NOP	result0	NOP	NOP

Update PC here when it's a beq

Hazard detection – Data hazard

- ✓ data hazard between ins0 and ins1
  - ➢ write target of ins0
  - ➢ operand of ins1

	IF stage	ID stage	EX stage	MEM stage	WB stage
Cycle0	ins0	NOP	NOP	NOP	NOP
Cycle1	ins1	decode0	NOP	NOP	NOP
Cycle2	ins1	NOP	result0	NOP	NOP
Cycle3	ins1	NOP	NOP	mem0	NOP
Cycle4	ins2	decode1	NOP	NOP	wb0

Data hazard – sensitive to what operand?

- Sensitive to

✓R- format - rs,rt

✓I – format – rs

- !exception : sw(I - format) – rs, rt

beq(I - format) – rs, rt

demo show with this simulator