Latch-up TESTING REPORT

Applicant/Department:	Nations Technologies Inc.		
Product:	N32WB031	**LOT:**	
Case NO:	S220223046	**Quantity:**	6 ea
Test Item:	Latch-up (LU)	**Package/Pin Count:**	QFN32
Application Date:	2022/2/23	**Date Finished:**	2022/3/1
Reference:	JESD78E	**Temperature:**	25/85/105 ± 5 °C **Humidity:** 55 ± 5%
Test Instrument:	MK2(SN0204336)	**Calibration Due Date:**	2021/08/19~2022/08/18
Failure Criteria:			
If absolute Inom is ⩽ 25 mA,then absolute Inom + 10 mA is used Or If absolute Inom is >25mA, then > 1.4X absolute Inom is used			
Trigger Current:	±100mA	**Minimum Pass Level = ±**	±100mA
Trigger Voltage:	/	**Minimum Pass Level = ±**	/
Vsupply Over Voltage:	1.5*VDDmax	**Minimum Pass Level = ±**	+5.5V

NOTE 1: ESD/latch-up test is employed as one of qualification tests for electronic products. However, the pass / fail results of this test can NOT be taken as go/no-go criteria for IC tape-out and mass production. Before and after ESD/latch-up test(s), complete parametric and functional testing (F/T) are essential for determining pass/fail of the tested products. (References: Page 9, AEC-Q100-003-Rev-E-2003; and Page 15, ESDA-JEDEC JS-001-2017).

NOTE 2: MA-tek sample storage policy is 14 days after the test data delivery. Prolonged storage can be arranged per client's request.

WE HEREBY CERTIFY THAT:

The test(s) was/were conducted according to test conditions provided by customer.Testing was performed on calibrated and JEDEC-ESDA qualified ESD instruments.The quality and comprehens[illegible]est(s) were delivered by qualified personnel.

Tested by	Reviewed by	Approved by
Joe_Xu	Fly_Fei	Steven Zhu

CERTIFICATE of APPROVAL INDEPENDENT TESTING LABORATORY:

ISO9001:2015 Certificate Registration No. 20001845 QM08, issued by UL DQS Inc.
IEC/IECQ17025 Certificate No. IECQ-L ULTW 09.0009, approved by Certification Body (CB): UL Registered Firm

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1. TEST SUMMARY

IT CLASS: I&II

NOTE:

Class I - Latch-up testing performed at room temperature.

Class II - Latch-up testing performed at maximum ambient rated temperature for the device.

Level: A

Level A - The failure criteria as defined in JEDEC.

Level B - Special failure criteria. Supplier shall provide definition of failure criteria used.

Trigger Model	Test Pin	Sample	Passing Current or Voltage
+IT	+IT_IO_25C	3	Pass(+100mA)
	+IT_IO_85C	3	Pass(+100mA)
	+IT_IO_105C	3	Pass(+100mA)
-IT	-IT_IO_25C	3	Pass(-100mA)
	-IT_IO_85C	3	Pass(-100mA)
	-IT_IO_105C	3	Pass(-100mA)
Vsupply Over voltage test	OV_VCC_25C	3	Pass(+5.5V)
	OV_VCCRF_25C		Pass(+5.5V)
	OV_VCC_85C	3	Pass(+5.5V)
	OV_VCCRF_85C		Pass(+5.5V)
	OV_VCC_105C	3	Pass(+5.5V)
	OV_VCCRF_105C		Pass(+5.5V)

NOTE: Red color in raw data indicates failed pins, if any.

2. Pin ASSIGNMENT

Pin Group	PAD Pins
PA2	1
PA3	2
RESET	3
PB0	4
PA4	5
PA5	6
PA6	7
VDD_FLASH	8
PB8	9
PB9	10
PB1	11
PB2	12
PB3	13
PB4	14
PB5	15
PB6	16
PB7	17
PB10	18
PB12	19
PB11	20
PB13	21
VCC	22
SWITCH	23
VDCDC	24
RFIOP	25
VDD_PA	26
VDCDC_RF	27
VCCRF	28
XO32MM_OUT	29
XO32MP_IN	30
PA0	31
PA1	32
VSSP	33

3. ESD TEST CONDITIONS

Testing Combinations

+IT
-IT
OV

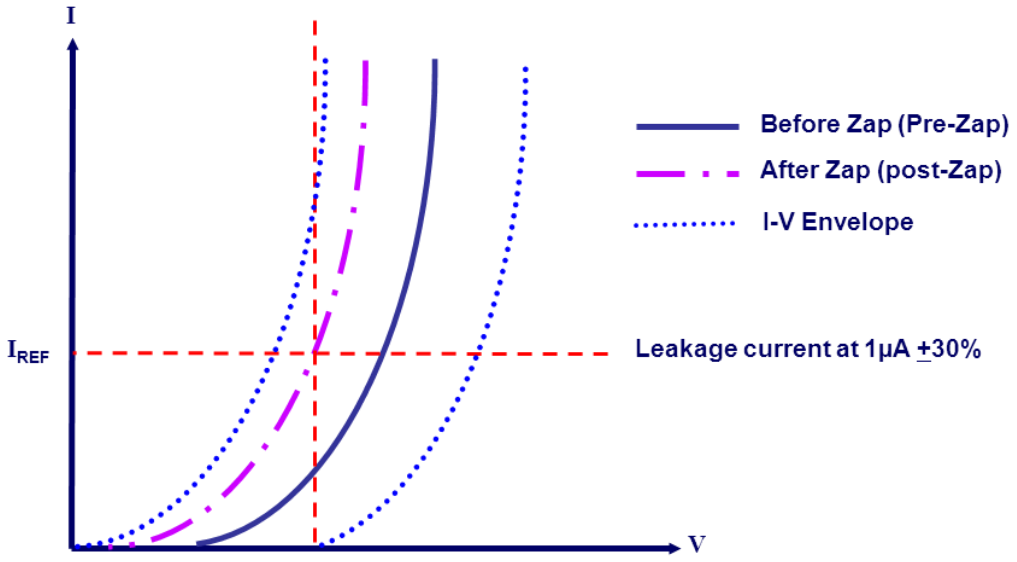
4. Raw Data - 2

Positive/Negative Current Trigger_+/- 100 (Unit:mA) 25C/85C/105C									
Test Pin	Fail Current	#22	#23	#24	Test Pin	Fail Current	#22	#23	#24
1	PA2	Pass	Pass	Pass	16	PB6	Pass	Pass	Pass
2	PA3	Pass	Pass	Pass	17	PB7	Pass	Pass	Pass
3	RESET	Pass	Pass	Pass	18	PB10	Pass	Pass	Pass
4	PB0	Pass	Pass	Pass	19	PB12	Pass	Pass	Pass
5	PA4	Pass	Pass	Pass	20	PB11	Pass	Pass	Pass
6	PA5	Pass	Pass	Pass	21	PB13	Pass	Pass	Pass
7	PA6	Pass	Pass	Pass	23	SWITCH	Pass	Pass	Pass
8	VDD_FLASH	Pass	Pass	Pass	24	VDCDC	Pass	Pass	Pass
9	PB8	Pass	Pass	Pass	25	RFIOP	Pass	Pass	Pass
10	PB9	Pass	Pass	Pass	26	VDD_PA	Pass	Pass	Pass
11	PB1	Pass	Pass	Pass	27	VDCDC_RF	Pass	Pass	Pass
12	PB2	Pass	Pass	Pass	32	PA1	Pass	Pass	Pass
13	PB3	Pass	Pass	Pass	29	XO32MM_OUT	Pass	Pass	Pass
14	PB4	Pass	Pass	Pass	30	XO32MP_IN	Pass	Pass	Pass
15	PB5	Pass	Pass	Pass	31	PA0	Pass	Pass	Pass

Vsupply Over voltage test_+5.5 (Unit:V) 25C/85C/105C									
Test Pin	Fail Voltage	#25	#26	#27	Test Pin	Fail Voltage	#25	#26	#27
22	VCC	Pass	Pass	Pass	28	VCCRF	Pass	Pass	Pass

5. APPENDIX-1 (PASS/FAIL CRITERIA)

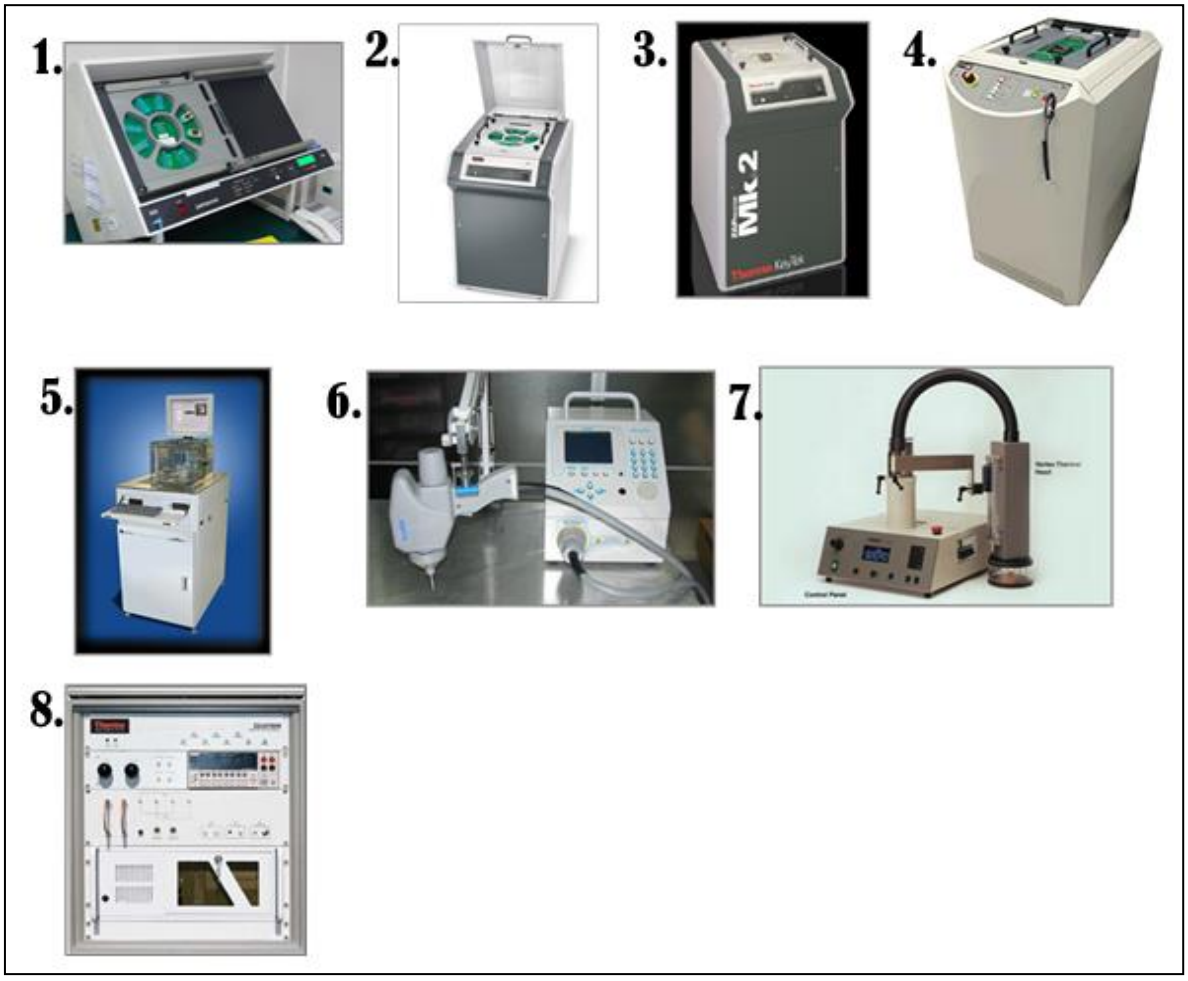
FAILURE CRITERIA	**If absolute Inom is ⩽25 mA,then absolute Inom + 10 mA is used Or If absolute Inom is > 25 mA, then > 1.4X absolute Inom is used.**
Note	**For custom designed ESD testing customers may select variation in Idd, and leakage current as criteria to determine pass/fail results of ESD testing.**



Pass/Fail Criteria:
Variation of Leakage Current and I-V Shift in Pre-Zap and Post-Zap curves

6. APPENDIX-2 (ESD INSTRUMENTATION AT MA-TEK)

No.	Test Tools	Vendors	System Specification
1	Zapmaster	Thermo Keytek	256 Pin Count, ESD Pulse 50 V to 8 KV
2	MK1	Thermo Scientific	256 Pin Count, ESD Pulse 10 V to 8 KV
3	MK2	Thermo Keytek	768 Pin Count, ESD Pulse 10 V to 8 KV
4	MK4	Thermo Scientific	2304 Pin Count, ESD Pulse 10 V to 8 KV
5	CDM Tester	Oryx Orion	100 V to 2 KV
6	ESD Gun	Noiseken	Voltage = 1 KV to 30 KV
7	High Temp. Test Module	Thermonics	Maximum temperature = 150°C.
8	TLP Tester	Thermo Scientific	Voltage = 1 V to 2 KV, Current = 10 nA to 40 A



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