LMC6081 Precision CMOS Single Operational Amplifier

Check for Samples: LMC6081

FEATURES

- **(Typical unless otherwise stated)**
- **Low offset voltage: 150 μV**
- **Operates from 4.5V to 15V single supply**
- **Ultra low input bias current: 10 fA**
- **Output swing to within 20 mV of supply rail, 100k load**
- **Input common-mode range includes V⁻**
- **High voltage gain: 130 dB**
- **Improved latchup immunity**

APPLICATIONS

- **Instrumentation amplifier**
- **Photodiode and infrared detector preamplifier**
- **Transducer amplifiers**
- **Medical instrumentation**
- **D/A converter**
- **Charge amplifier for piezoelectric transducers**

DESCRIPTION

The LMC6081 is a precision low offset voltage operational amplifier, capable of single supply operation. Performance characteristics include ultra low input bias current, high voltage gain, rail-to-rail output swing, and an input common mode voltage range that includes ground. These features, plus its low offset voltage, make the LMC6081 ideally suited for precision circuit applications.

Other applications using the LMC6081 include precision full-wave rectifiers, integrators, references, and sample-and-hold circuits.

This device is built with TI's advanced Double-Poly Silicon-Gate CMOS process.

For designs with more critical power demands, see the LMC6061 precision micropower operational amplifier.

For a dual or quad operational amplifier with similar features, see the LMC6082 or LMC6084 respectively.

Connection Diagram

8-Pin PDIP/SOIC Package - Top View

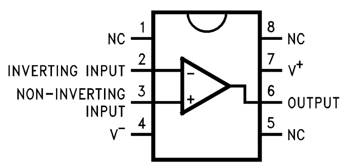


Figure 1. See Package Number P0008E/D0008A

Low-Leakage Sample and Hold

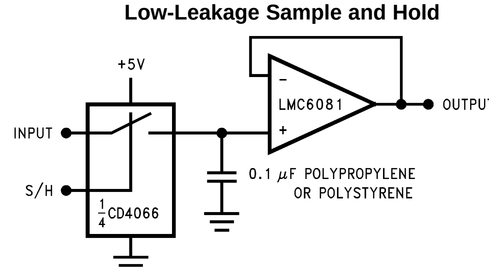


Figure 2.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)

Differential Input Voltage	±Supply Voltage
Voltage at Input/Output Pin	(V^+) +0.3V,
	(V^-) −0.3V
Supply Voltage $(V^+ - V^-)$	16V
Output Short Circuit to V^+	(2)
Output Short Circuit to V^-	(3)
Lead Temperature	
(Soldering, 10 Sec.)	260°C
Storage Temp. Range	−65°C to +150°C
Junction Temperature	150°C
ESD Tolerance (4)	2 kV
Current at Input Pin	±10 mA
Current at Output Pin	±30 mA
Current at Power Supply Pin	40 mA
Power Dissipation	(5)

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed.
(2) Do not connect output to V^+, when V^+ is greater than 13V or reliability will be adversely affected.
(3) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.
(4) Human body model, 1.5 kΩ in series with 100 pF.
(5) The maximum power dissipation is a function of $T_{J(Max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(Max)} - T_A) / \theta_{JA}$.

Operating Ratings (1)

Temperature Range	
LMC6081AM	$-55°C \le T_J \le +125°C$
LMC6081AI, LMC6081I	$-40°C \le T_J \le +85°C$
Supply Voltage	$4.5V \le V^+ \le 15.5V$
Thermal Resistance (θ_{JA}), (2)	
8-Pin PDIP	115°C/W
8-Pin SOIC	193°C/W
Power Dissipation (3)	

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed.
(2) All numbers apply for packages soldered directly into a PC board.
(3) For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$.

DC Electrical Characteristics

Unless otherwise specified, all limits ensured for $T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$ and $R_L > 1M$ unless otherwise specified.

Symbol	Parameter	Conditions	Typ[1]	LMC6081AM Limit[2]	LMC6081AI Limit[2]	LMC6081I Limit[2]	Units
V_{OS}	Input Offset Voltage		150	350	350	800	μV
				1000	**800**	**1300**	Max
TCV_{OS}	Input Offset Voltage Average Drift		1.0				μV/°C
I_B	Input Bias Current		0.010				pA
				100	**4**	**4**	Max
I_{OS}	Input Offset Current		0.005				pA
				100	**2**	**2**	Max
R_{IN}	Input Resistance		>10				Tera Ω
CMRR	Rejection Ratio Common Mode	$0V \le V_{CM} \le 12.0V$, $V^+ = 15V$	85	75	75	66	dB
				72	**72**	**63**	Min
+PSRR	Positive Power Supply Rejection Ratio	$5V \le V^+ \le 15V$, $V_O = 2.5V$	85	75	75	66	dB
				72	**72**	**63**	Min
−PSRR	Negative Power Supply Rejection Ratio	$0V \le V^- \le -10V$	94	84	84	74	dB
				81	**81**	**71**	Min
V_{CM}	Voltage Range Input Common-Mode	$V^+ = 5V$ and 15V for CMRR ≥ 60 dB	−0.4	−0.1	−0.1	−0.1	V
				0	**0**	**0**	Max
			$V^+ - 1.9$	$V^+ - 2.3$	$V^+ - 2.3$	$V^+ - 2.3$	V
				$\mathbf{V^+ - 2.6}$	$\mathbf{V^+ - 2.5}$	$\mathbf{V^+ - 2.5}$	Min
A_V	Large Signal Voltage Gain	$R_L = 2\ k\Omega$ [3], Sourcing	1400	400	400	300	V/mV
				300	**300**	**200**	Min
		$R_L = 2\ k\Omega$ [3], Sinking	350	180	180	90	V/mV
				70	**100**	**60**	Min
		$R_L = 600\Omega$ [3], Sourcing	1200	400	400	200	V/mV
				150	**150**	**80**	Min
		$R_L = 600\Omega$ [3], Sinking	150	100	100	70	V/mV
				35	**50**	**35**	Min

(1) Typical values represent the most likely parametric norm.
(2) All limits are ensured by testing or statistical analysis.
(3) $V^+ = 15V$, $V_{CM} = 7.5V$ and R_L connected to 7.5V. For Sourcing tests, $7.5V \le V_O \le 11.5V$. For Sinking tests, $2.5V \le V_O \le 7.5V$.

DC Electrical Characteristics (continued)

Unless otherwise specified, all limits ensured for T_J = 25°C. **Boldface** limits apply at the temperature extremes. V^+ = 5V, V^- = 0V, V_{CM} = 1.5V, V_O = 2.5V and R_L > 1M unless otherwise specified.

Symbol	Parameter	Conditions	Typ (1)	LMC6081AM Limit (2)	LMC6081AI Limit (2)	LMC6081I Limit (2)	Units
V_O	Output Swing	V^+ = 5V R_L = 2 kΩ to 2.5V	4.87	4.80 **4.70**	4.80 **4.73**	4.75 **4.67**	V Min
			0.10	0.13 **0.19**	0.13 **0.17**	0.20 **0.24**	V Max
		V^+ = 5V R_L = 600Ω to 2.5V	4.61	4.50 **4.24**	4.50 **4.31**	4.40 **4.21**	V Min
			0.30	0.40 **0.63**	0.40 **0.50**	0.50 **0.63**	V Max
		V^+ = 15V R_L = 2 kΩ to 7.5V	14.63	14.50 **14.30**	14.50 **14.34**	14.37 **14.25**	V Min
			0.26	0.35 **0.48**	0.35 **0.45**	0.44 **0.56**	V Max
		V^+ = 15V R_L = 600Ω to 7.5V	13.90	13.35 **12.80**	13.35 **12.86**	12.92 **12.44**	V Min
			0.79	1.16 **1.42**	1.16 **1.32**	1.33 **1.58**	V Max
I_O	V^+ = 5V Output Current	Sourcing, V_O = 0V	22	16 **8**	16 **10**	13 **8**	mA Min
		Sinking, V_O = 5V	21	16 **11**	16 **13**	13 **10**	mA Min
I_O	V^+ = 15V Output Current	Sourcing, V_O = 0V	30	28 **18**	28 **22**	23 **18**	mA Min
		Sinking, V_O = 13V (4)	34	28 **19**	28 **22**	23 **18**	mA Min
I_S	Supply Current	V^+ = +5V, V_O = 1.5V	450	750 **900**	750 **900**	750 **900**	µA Max
		V^+ = +15V, V_O = 7.5V	550	850 **950**	850 **950**	850 **950**	µA Max

(4) Do not connect output to V^+, when V^+ is greater than 13V or reliability will be adversely affected.

AC Electrical Characteristics

Unless otherwise specified, all limits ensured for $T_J = 25°C$, **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$ and $R_L > 1M$ unless otherwise specified.

Symbol	Parameter	Conditions	Typ(1)	LMC6081AM Limit(2)	LMC6081AI Limit(2)	LMC6081 Limit(2)	Units
SR	Slew Rate	(3)	1.5	0.8 **0.5**	0.8 **0.6**	0.8 **0.6**	V/μs Min
GBW	Gain-Bandwidth Product		1.3				MHz
φ_m	Phase Margin		50				Deg
e_n	Input-Referred Voltage Noise	F = 1 kHz	22				$nV\sqrt{Hz}$
i_n	Input-Referred Current Noise	F = 1 kHz	0.0002				$pA\sqrt{Hz}$
T.H.D.	Total Harmonic Distortion	F = 10 kHz, $A_V = -10$ $R_L = 2\ k\Omega$, $V_O = 8\ V_{PP}$ ±5V Supply	0.01				%

(1) Typical values represent the most likely parametric norm.
(2) All limits are ensured by testing or statistical analysis.
(3) $V^+ = 15V$. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

Typical Performance Characteristics

V_S = ±7.5V, T_A = 25°C, Unless otherwise specified

Distribution of LMC6081 Input Offset Voltage (T_A = +25°C)

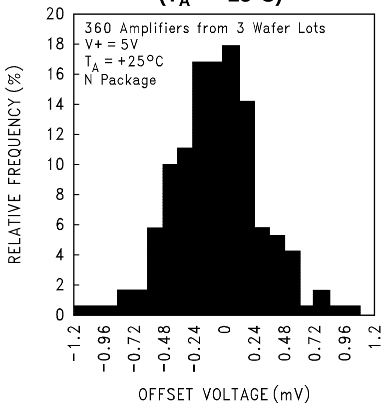


Figure 3.

Distribution of LMC6081 Input Offset Voltage (T_A = −55°C)

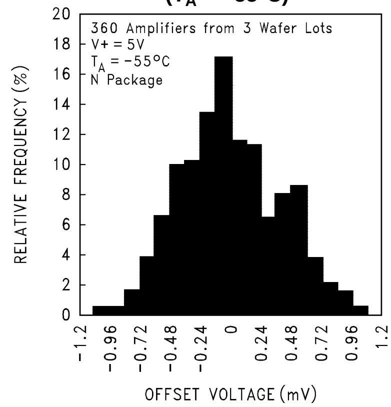


Figure 4.

Distribution of LMC6081 Input Offset Voltage (T_A = +125°C)

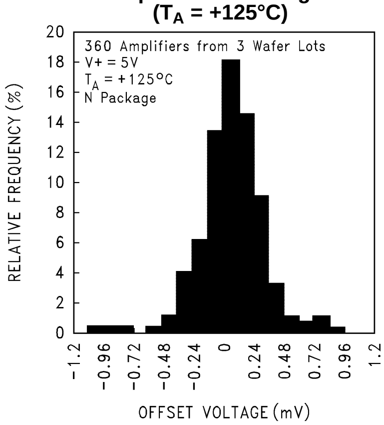


Figure 5.

Input Bias Current vs Temperature

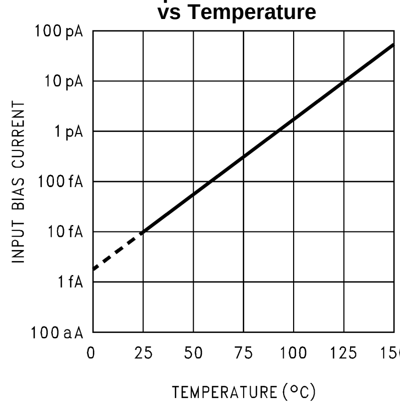


Figure 6.

Supply Current vs Supply Voltage

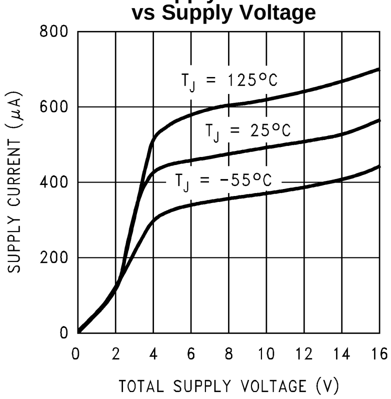


Figure 7.

Input Voltage vs Output Voltage

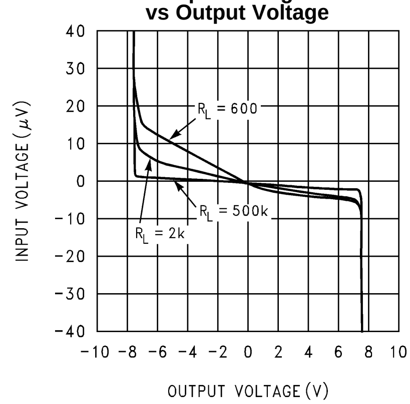


Figure 8.

Typical Performance Characteristics (continued)

V_S = ±7.5V, T_A = 25°C, Unless otherwise specified

Common Mode Rejection Ratio vs Frequency

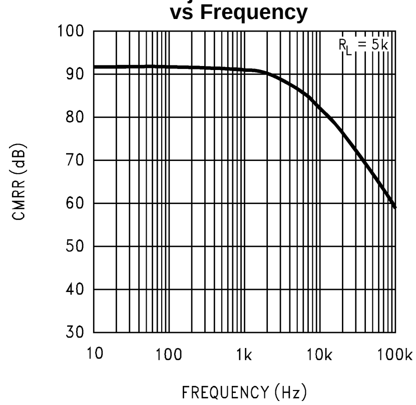


Figure 9.

Power Supply Rejection Ratio vs Frequency

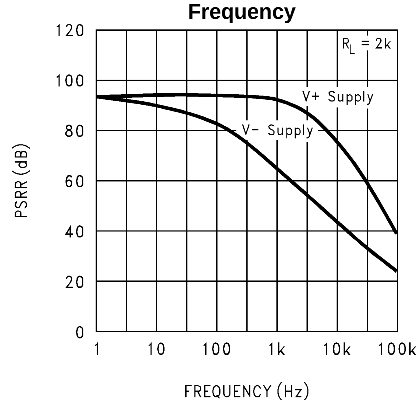


Figure 10.

Input Voltage Noise vs Frequency

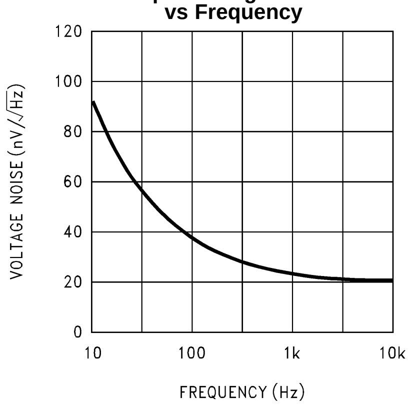


Figure 11.

Output Characteristics Sourcing Current

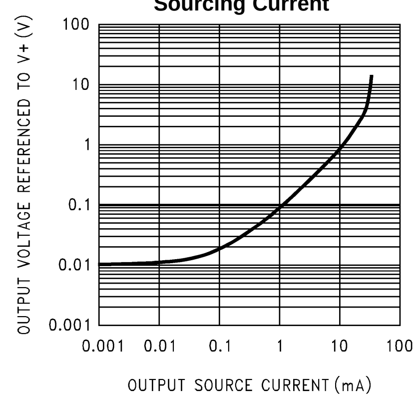


Figure 12.

Output Characteristics Sinking Current

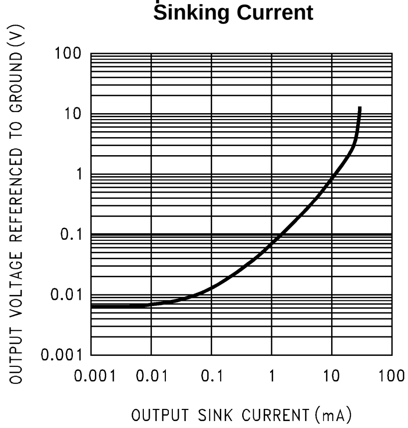


Figure 13.

Gain and Phase Response vs Temperature (−55°C to +125°C)

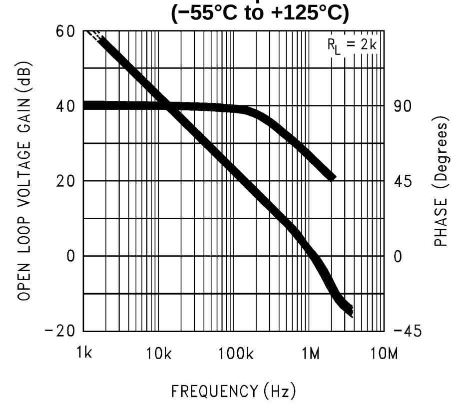


Figure 14.

Typical Performance Characteristics (continued)

V_S = ±7.5V, T_A = 25°C, Unless otherwise specified

Gain and Phase Response vs Capacitive Load with R_L = 600Ω

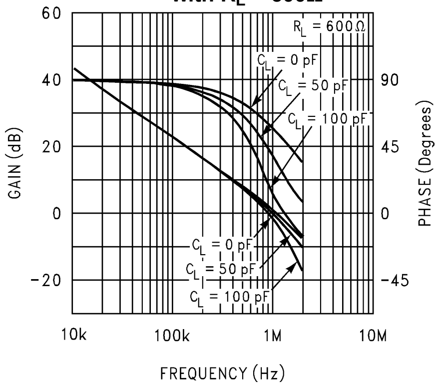


Figure 15.

Gain and Phase Response vs Capacitive Load with R_L = 500 kΩ

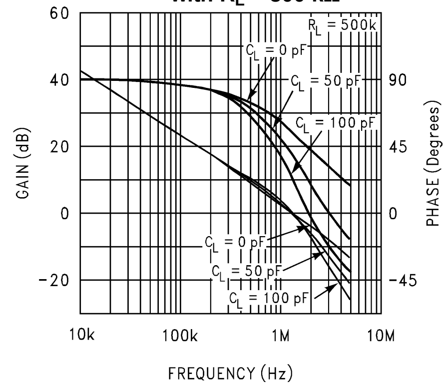


Figure 16.

Open Loop Frequency Response

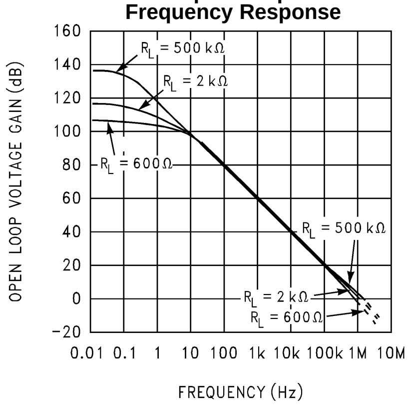


Figure 17.

Inverting Small Signal Pulse Response

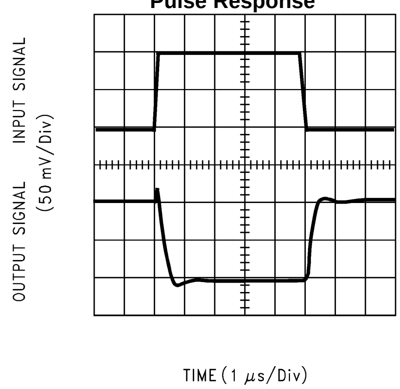


Figure 18.

Inverting Large Signal Pulse Response

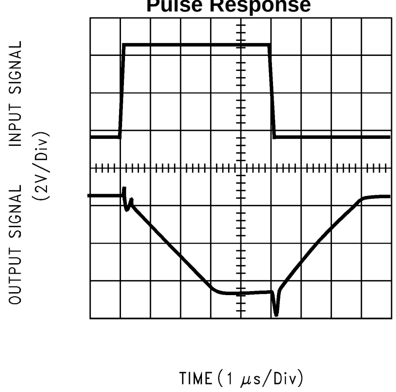


Figure 19.

Non-Inverting Small Signal Pulse Response

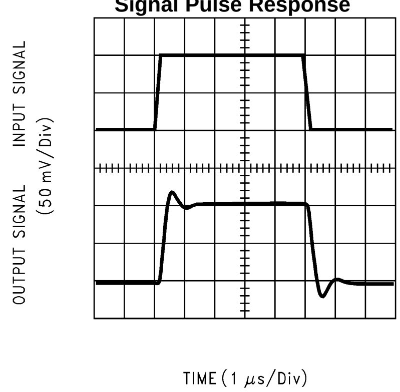


Figure 20.

Typical Performance Characteristics (continued)

$V_S = \pm 7.5V$, $T_A = 25°C$, Unless otherwise specified

Non-Inverting Large Signal Pulse Response

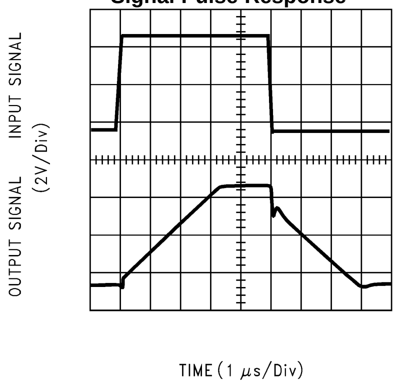


Figure 21.

Stability vs Capacitive Load, $R_L = 600\Omega$

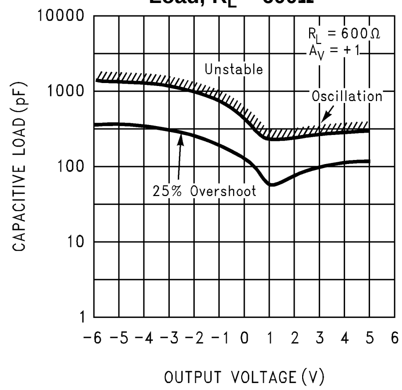


Figure 22.

Stability vs Capacitive Load $R_L = 1\ M\Omega$

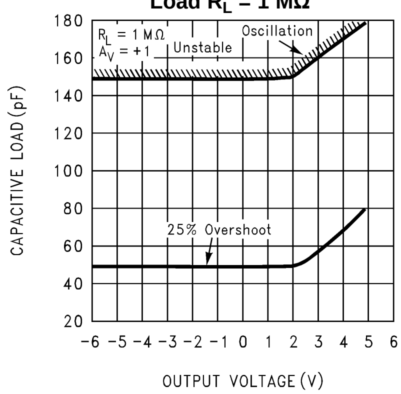


Figure 23.

APPLICATION INFORMATION

AMPLIFIER TOPOLOGY

The LMC6081 incorporates a novel op-amp design topology that enables it to maintain rail-to-rail output swing even when driving a large load. Instead of relying on a push-pull unity gain output buffer stage, the output stage is taken directly from the internal integrator, which provides both low output impedance and large gain. Special feed-forward compensation design techniques are incorporated to maintain stability over a wider range of operating conditions than traditional micropower op-amps. These features make the LMC6081 both easier to design with, and provide higher speed than products typically found in this ultra-low power class.

COMPENSATING FOR INPUT CAPACITANCE

It is quite common to use large values of feedback resistance for amplifiers with ultra-low input current, like the LMC6081.

Although the LMC6081 is highly stable over a wide range of operating conditions, certain precautions must be met to achieve the desired pulse response when a large feedback resistor is used. Large feedback resistors and even small values of input capacitance, due to transducers, photodiodes, and circuit board parasitics, reduce phase margins.

When high input impedances are demanded, guarding of the LMC6081 is suggested. Guarding input lines will not only reduce leakage, but lowers stray input capacitance as well. (See *Printed-Circuit-Board Layout for High Impedance Work).*

The effect of input capacitance can be compensated for by adding a capacitor, C_f, around the feedback resistors (as in Figure 24) such that:

$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_f} \tag{1}$$

or

$$R_1\, C_{IN} \leq R_2\, C_f \tag{2}$$

Since it is often difficult to know the exact value of C_{IN}, C_f can be experimentally adjusted so that the desired pulse response is achieved. Refer to the LMC660 and LMC662 for a more detailed discussion on compensating for input capacitance.

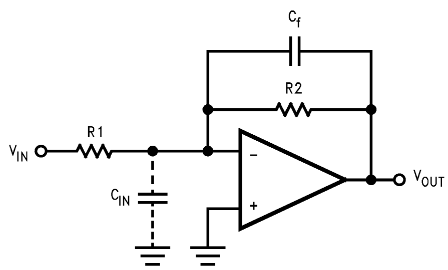


Figure 24. Cancelling the Effect of Input Capacitance

CAPACITIVE LOAD TOLERANCE

All rail-to-rail output swing operational amplifiers have voltage gain in the output stage. A compensation capacitor is normally included in this integrator stage. The frequency location of the dominant pole is affected by the resistive load on the amplifier. Capacitive load driving capability can be optimized by using an appropriate resistive load in parallel with the capacitive load (see typical curves).

Direct capacitive loading will reduce the phase margin of many op-amps. A pole in the feedback loop is created by the combination of the op-amp's output impedance and the capacitive load. This pole induces phase lag at the unity-gain crossover frequency of the amplifier resulting in either an oscillatory or underdamped pulse response. With a few external components, op amps can easily indirectly drive capacitive loads, as shown in Figure 25.

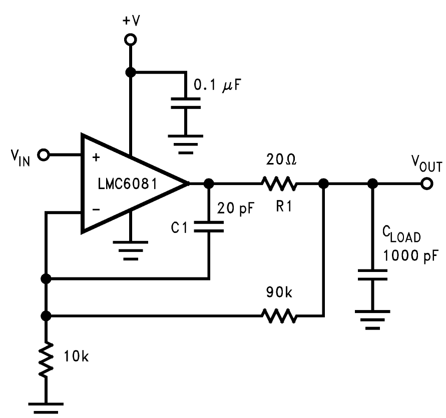


Figure 25. LMC6081 Noninverting Gain of 10 Amplifier, Compensated to Handle Capacitive Loads

In the circuit of Figure 25, R1 and C1 serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop.

Capacitive load driving capability is enhanced by using a pull up resistor to V^+ (Figure 26). Typically a pull up resistor conducting 500 μA or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see electrical characteristics).

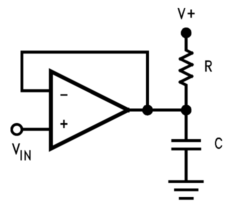


Figure 26. Compensating for Large Capacitive Loads with a Pull Up Resistor

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LMC6081, typically less than 10 fA, it is essential to have an excellent layout. Fortunately, the techniques of obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6081's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op-amp's inputs, as in Figure 27. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of the input. This would cause a 100 times degradation from the LMC6081's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11}\Omega$ would cause only 0.05 pA of leakage current. See Figure 28 for typical connections of guard rings for standard op-amp configurations.

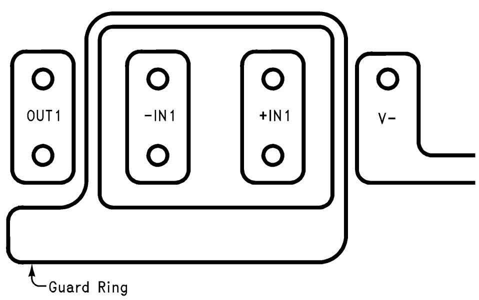


Figure 27. Example of Guard Ring in P.C. Board Layout

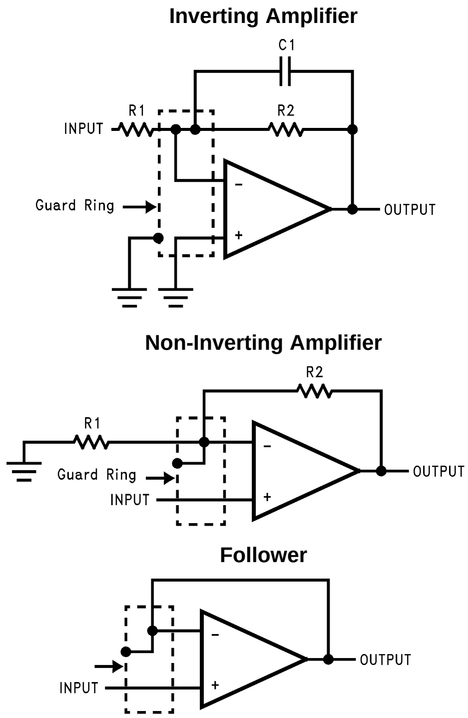
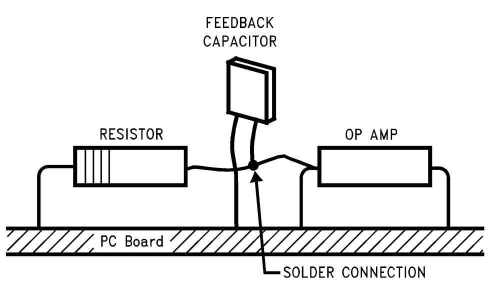


Figure 28. Typical Connections of Guard Rings

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See Figure 29.



(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board).

Figure 29. Air Wiring

Latchup

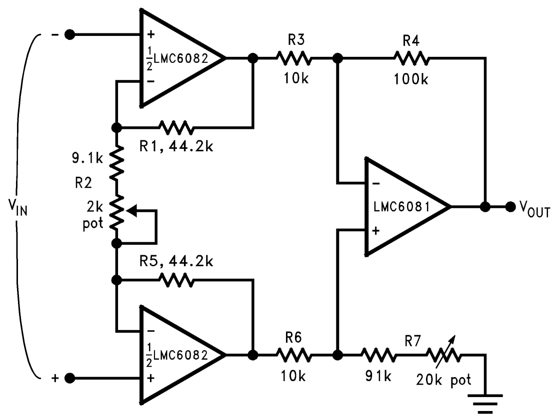
CMOS devices tend to be susceptible to latchup due to their internal parasitic SCR effects. The (I/O) input and output pins look similar to the gate of the SCR. There is a minimum current required to trigger the SCR gate lead. The LMC6061 and LMC6081 are designed to withstand 100 mA surge current on the I/O pins. Some resistive method should be used to isolate any capacitance from supplying excess current to the I/O pins. In addition, like an SCR, there is a minimum holding current for any latchup mode. Limiting current to the supply pins will also inhibit latchup susceptibility.

Typical Single-Supply Applications

($V^+ = 5.0\ V_{DC}$)

The extremely high input impedance, and low power consumption, of the LMC6081 make it ideal for applications that require battery-powered instrumentation amplifiers. Examples of these types of applications are hand-held pH probes, analytic medical instruments, magnetic field detectors, gas detectors, and silicon based pressure transducers.

Figure 30 shows an instrumentation amplifier that features high differential and common mode input resistance ($>10^{14}\Omega$), 0.01% gain accuracy at $A_V = 1000$, excellent CMRR with 1 kΩ imbalance in bridge source resistance. Input current is less than 100 fA and offset drift is less than 2.5 μV/°C. R_2 provides a simple means of adjusting gain over a wide range without degrading CMRR. R_7 is an initial trim used to maximize CMRR without using super precision matched resistors. For good CMRR over temperature, low drift resistors should be used.



If $R_1 = R_5$, $R_3 = R_6$, and $R_4 = R_7$; then

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_2 + 2R_1}{R_2} \times \frac{R_4}{R_3}$$

$A_V \approx 100$ for circuit shown ($R_2 = 9.822k$).

Figure 30. Instrumentation Amplifier

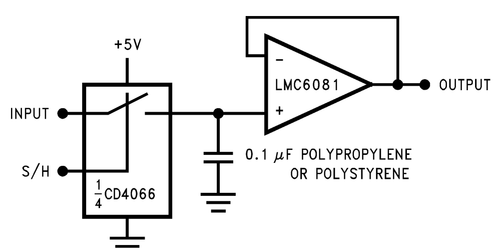


Figure 31. Low-Leakage Sample and Hold

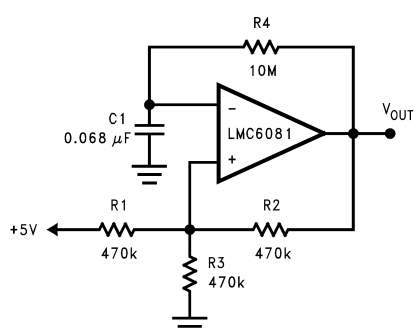


Figure 32. 1 Hz Square Wave Oscillator

REVISION HISTORY

Changes from Revision B (March 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	13

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMC6081-MDA	LIFEBUY	DIESALE	Y	0	270	RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125		
LMC6081AIM	LIFEBUY	SOIC	D	8	95	Non-RoHS & Green	Call TI	Level-1-235C-UNLIM	-40 to 85	LMC60 81AIM	
LMC6081AIM/NOPB	LIFEBUY	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LMC60 81AIM	
LMC6081AIMX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LMC60 81AIM	Samples
LMC6081IM/NOPB	LIFEBUY	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LMC60 81IM	
LMC6081IMX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LMC60 81IM	Samples
LMC6081IN/NOPB	LIFEBUY	PDIP	P	8	40	RoHS & Green	NIPDAU	Level-1-NA-UNLIM	-40 to 85	LMC6081 IN	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

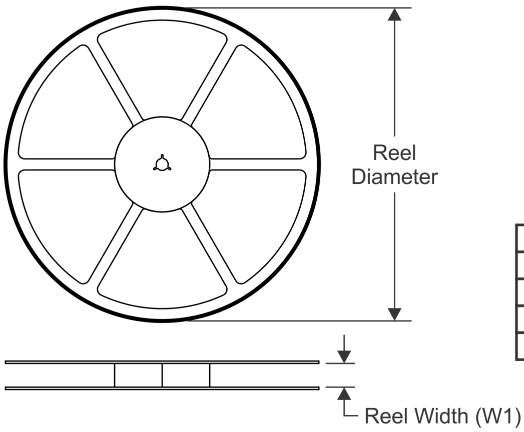
[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

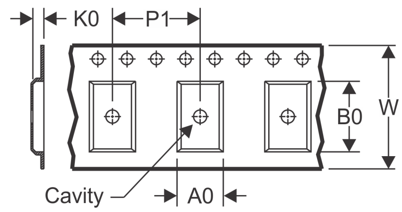
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

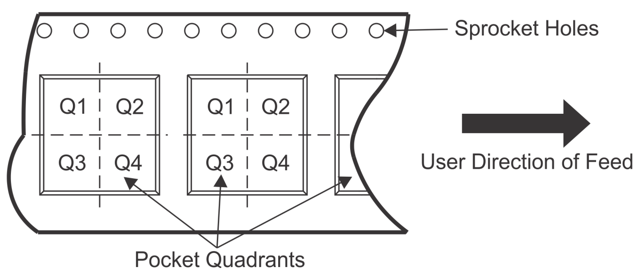


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

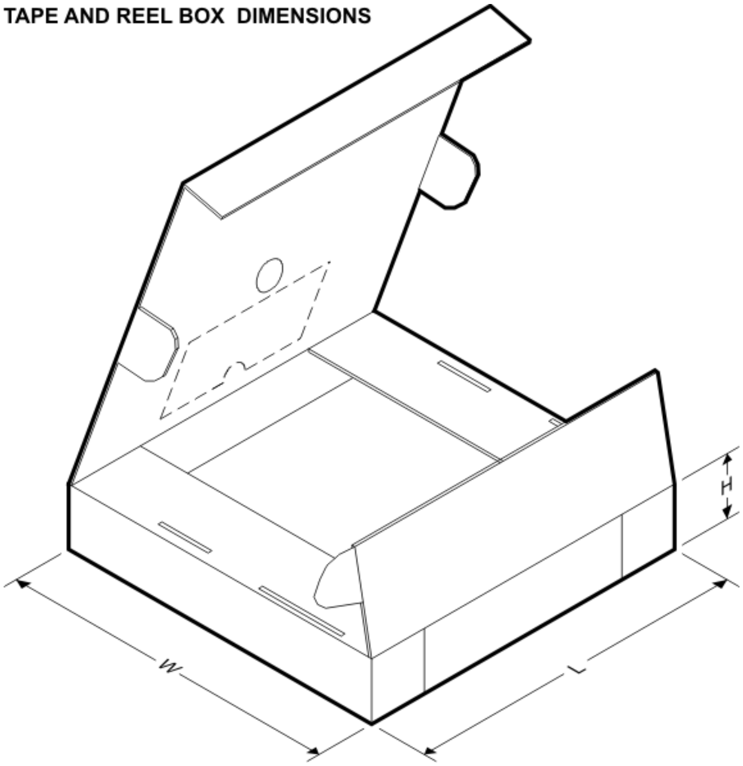
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMC6081AIMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMC6081IMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

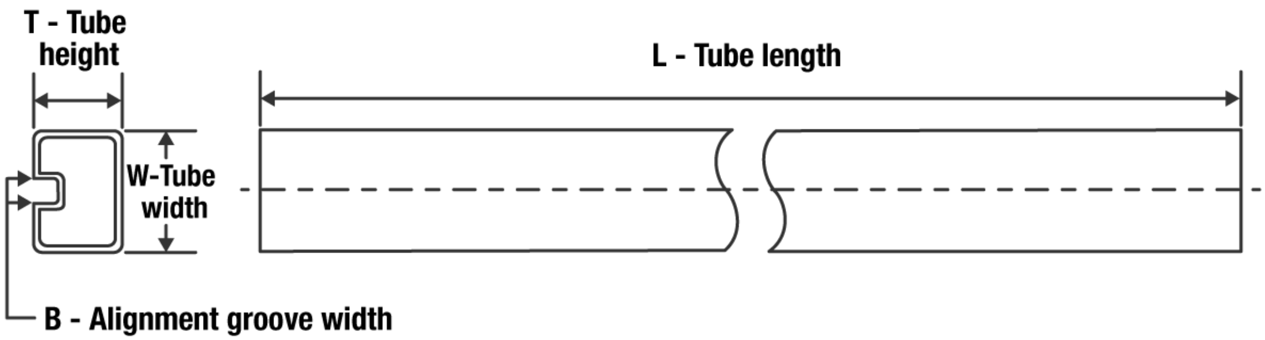
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMC6081AIMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMC6081IMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

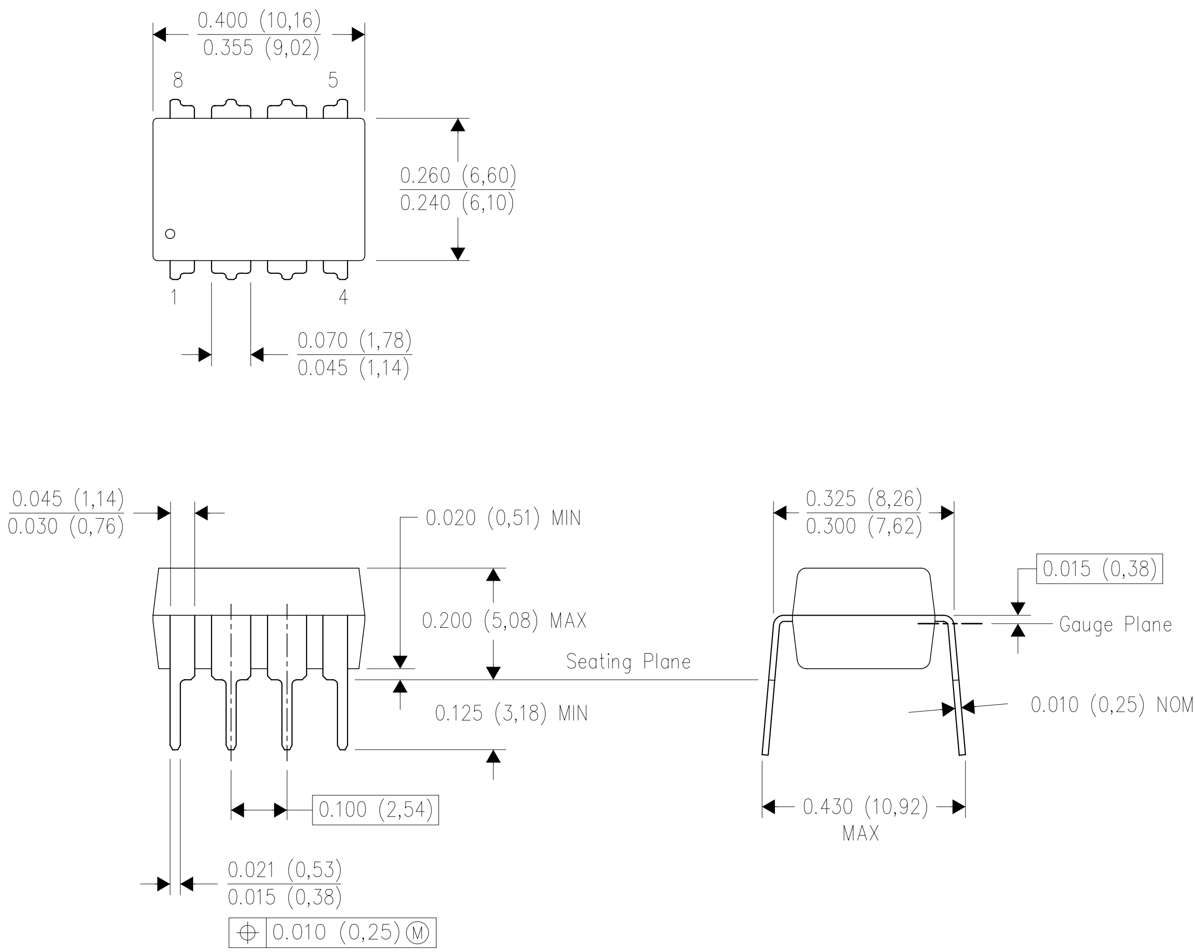
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LMC6081AIM	D	SOIC	8	95	495	8	4064	3.05
LMC6081AIM	D	SOIC	8	95	495	8	4064	3.05
LMC6081AIM/NOPB	D	SOIC	8	95	495	8	4064	3.05
LMC6081IM/NOPB	D	SOIC	8	95	495	8	4064	3.05
LMC6081IN/NOPB	P	PDIP	8	40	502	14	11938	4.32

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



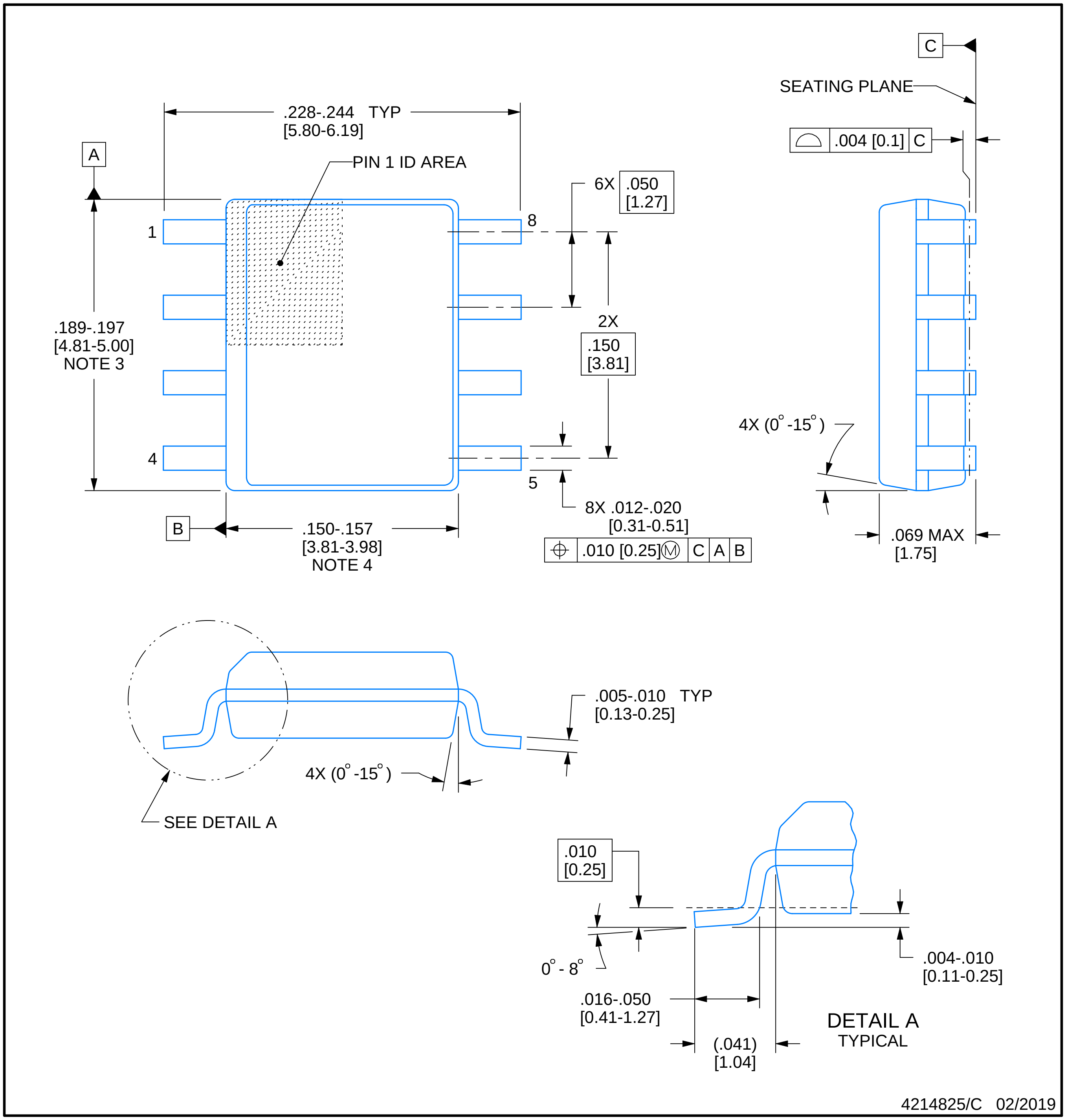
4040082/E 04/2010

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS–001 variation BA.

D0008A

SOIC - 1.75 mm max height

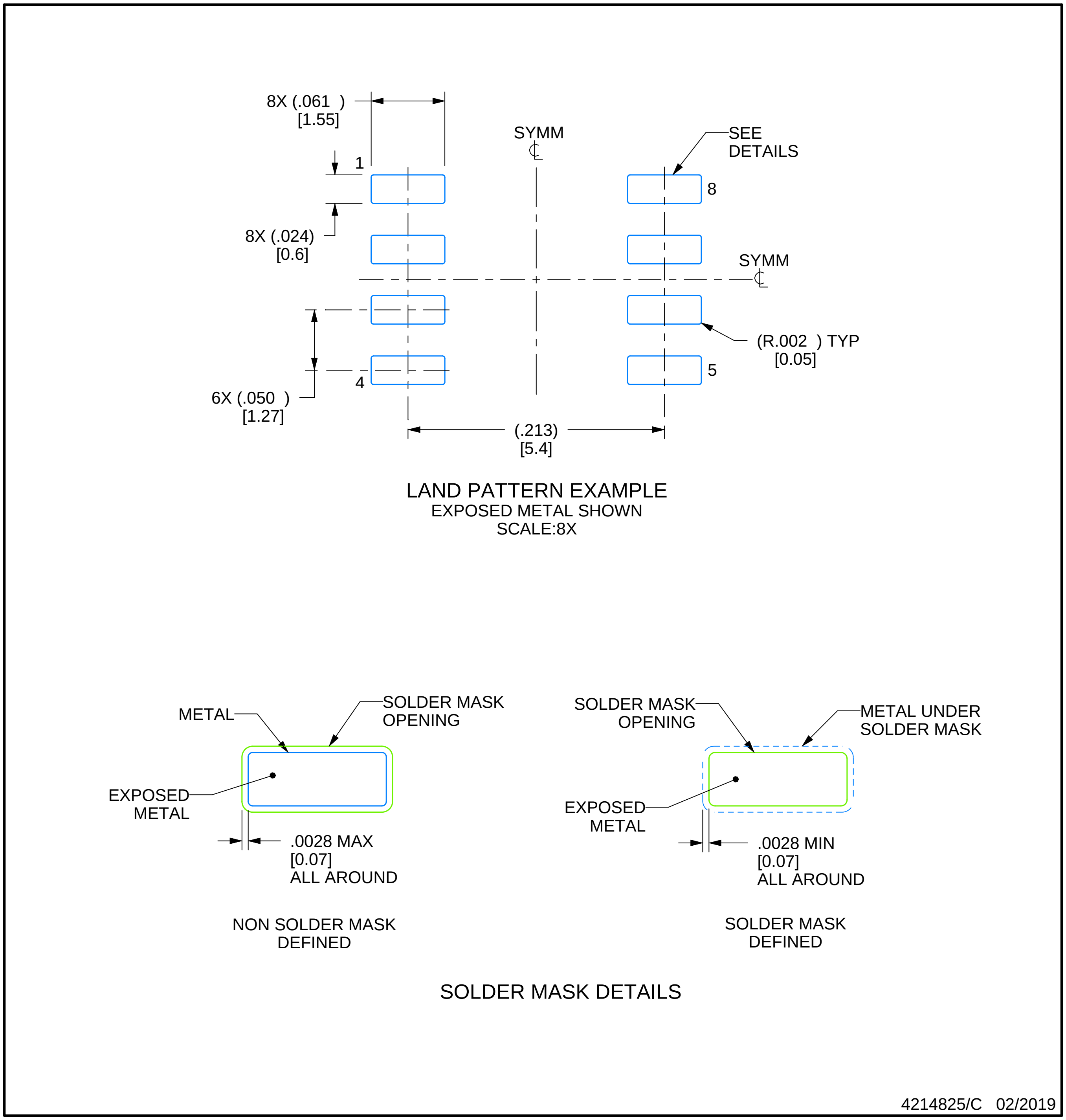
SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

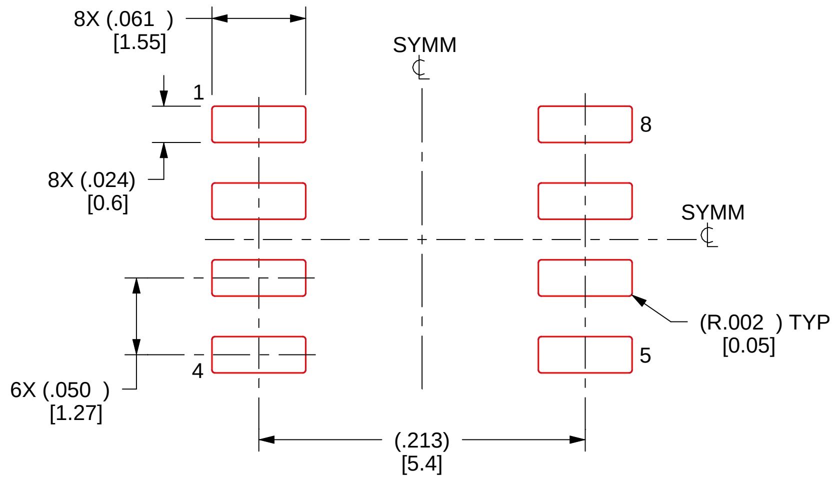
NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265