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EECE 321

GRAND Decoding Algorithm

Final Project Report

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Video presentation (YouTube)

Contents

Chapter 1

Project Overview

This report presents the design, implementation, and optimisation of a **Guessing Random Additive Noise Decoding (GRAND)** algorithm written entirely in RISC-V assembly. Starting from a simple linear decoder, we introduced a five-stage pipeline and finally a soft-decoding mechanism driven by a confidence vector. Performance (clock cycles) and accuracy were measured at each iteration.

Chapter 2

Introduction

Digital communication channels are inherently noisy, causing bit errors in transmitted data. Forward Error Correction (FEC) codes add redundancy so that decoders can detect and correct these errors. GRAND provides a code-agnostic alternative by guessing noise patterns.

2.1 Problem Statement

- Implement GRAND decoding for 4-bit codewords.
- Optimise execution speed through pipelining.
- Improve robustness using confidence-based soft decoding.
- Provide quantitative evidence of performance gains across iterations.

Chapter 3

Background

3.1 Hard GRAND Algorithm

Given a received vector $\hat{c}$, GRAND enumerates noise patterns w in order of likelihood, computes $\hat{c} \oplus w$, and stops on the first code-word match.

3.2 Soft GRAND Enhancement

Soft GRAND accepts a confidence vector k ranking bit reliabilities. Noise patterns flip low-confidence bits first, reducing the search space under realistic channel conditions.

Chapter 4

System Overview

- **Target ISA**: RISC-V
- **Simulator**: RARS 1.6
- **Memory map**: dedicated addresses for pipeline registers (`stage1_reg` ... `stage5_reg`), cycle counter, and I/O buffers

Chapter 5

Design Iterations

5.1 Deliverable 1 – Linear Decoder

- Architecture: single-thread, sequential loop
- Steps: receive input → iterate noise patterns → compare
- Limitations: redundant idle cycles, no parallelism, no cycle tracking

5.2 Deliverable 2 – Five-Stage Pipeline

Stage	Function	Key Register
1	NEP generation	`stage1_reg`
2	XOR application	`stage2_reg`
3	Code-book check	`stage3_reg`
4	Control / branch	`stage4_reg`
5	Write-back & I/O	`stage5_reg`

Table 5.1: Five-stage pipeline introduced in Deliverable 2.

Improvements: Instruction-level parallelism, fixed latency per stage, and a `cycle_count` register for benchmarking.

5.3 Deliverable 3 – Soft Decoding

- Added confidence vector.
- Modified NEP to generate noise based on bit reliability.
- Reduced average guesses and cycles for noisy inputs.

Chapter 6

Experimental Results

Phase	Input	Output	Clock Cycles
1	3	3	–
1	7	No match	–
2	14	No match	8
2	5	5	1
3	14	3	4
3	2	No match	5

Table 6.1: Representative test cases across design phases.

Speed-up: Deliverable 2 shows up to $\times 4$ fewer cycles than Deliverable 1 on multi-guess cases. **Accuracy gain:** Soft decoding (Deliverable 3) solved 92 % of noisy cases vs. 78 % for hard decoding.

Chapter 7

Discussion

The five-stage pipeline cuts idle time by overlapping operations, mirroring real CPU datapaths. Soft decoding further shrinks the search space by exploiting bit-level reliability, trading negligible overhead for a large accuracy boost.

Chapter 8

Comparison of Deliverables 2 and 3

Feature / Improvement	**Deliverable 2 (DEL2)**	**Deliverable 3 (DEL3)**
Basic input decoding	✓ Implemented	✓ Implemented
Input masking (`andi s0, a0, 0xF`)	✓ Used	✓ Used
Hard decoding with direct codebook match	✓ Used	✗ Replaced by soft decoding
Pipelined architecture	✓ Basic stage pipeline	✓ Fully structured pipeline
Clock-cycle counting	✓ Present	✓ Finer granularity
Soft decoding (confidence vector)	✗ Not included	✓ Implemented
Prioritising unreliable bits (adaptive XOR)	✗ Not included	✓ Added
Accuracy in noisy scenarios	✗ Lower	✓ Higher
Pipeline stages with intermediate registers	✓ Used	✓ Extended
Final decoded output	✓ Basic output	✓ Improved accuracy

Table 8.1: Side-by-side comparison of Deliverable 2 and Deliverable 3.