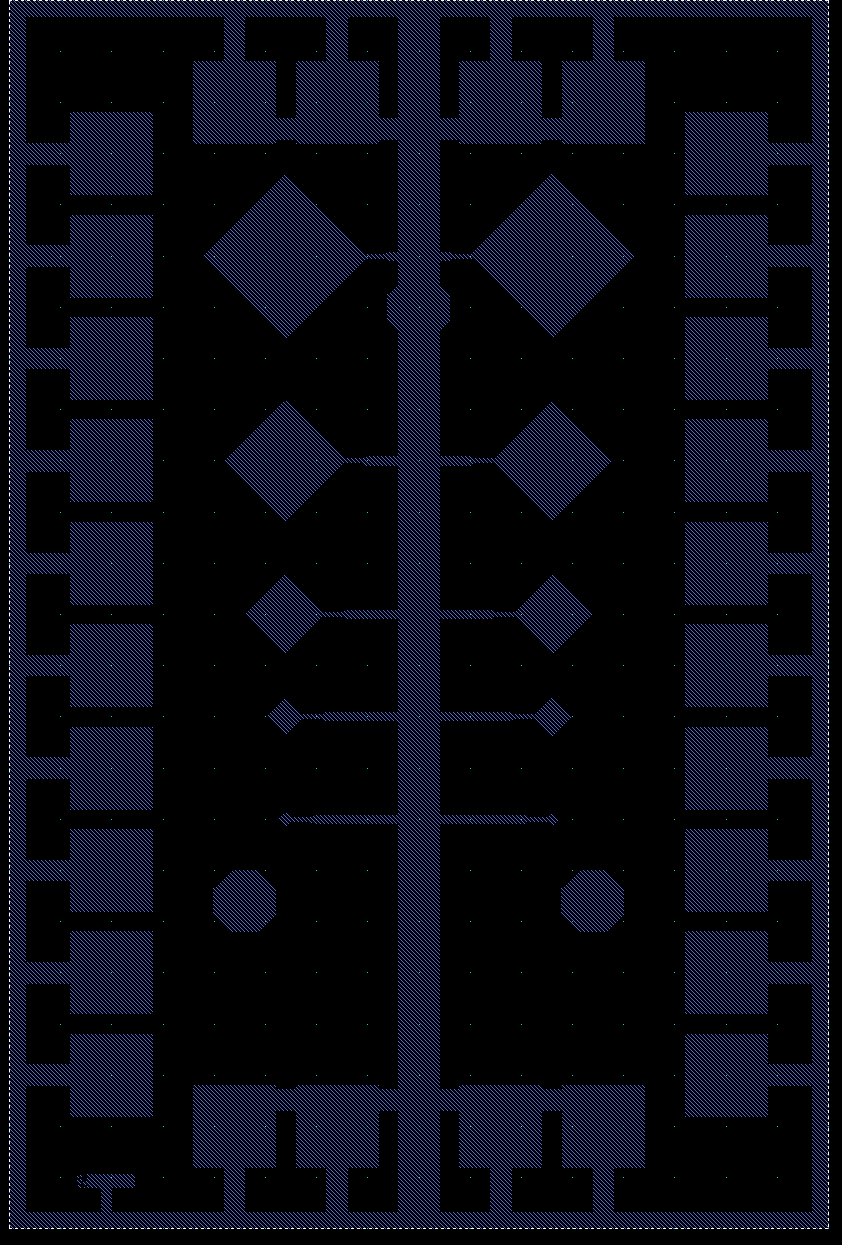
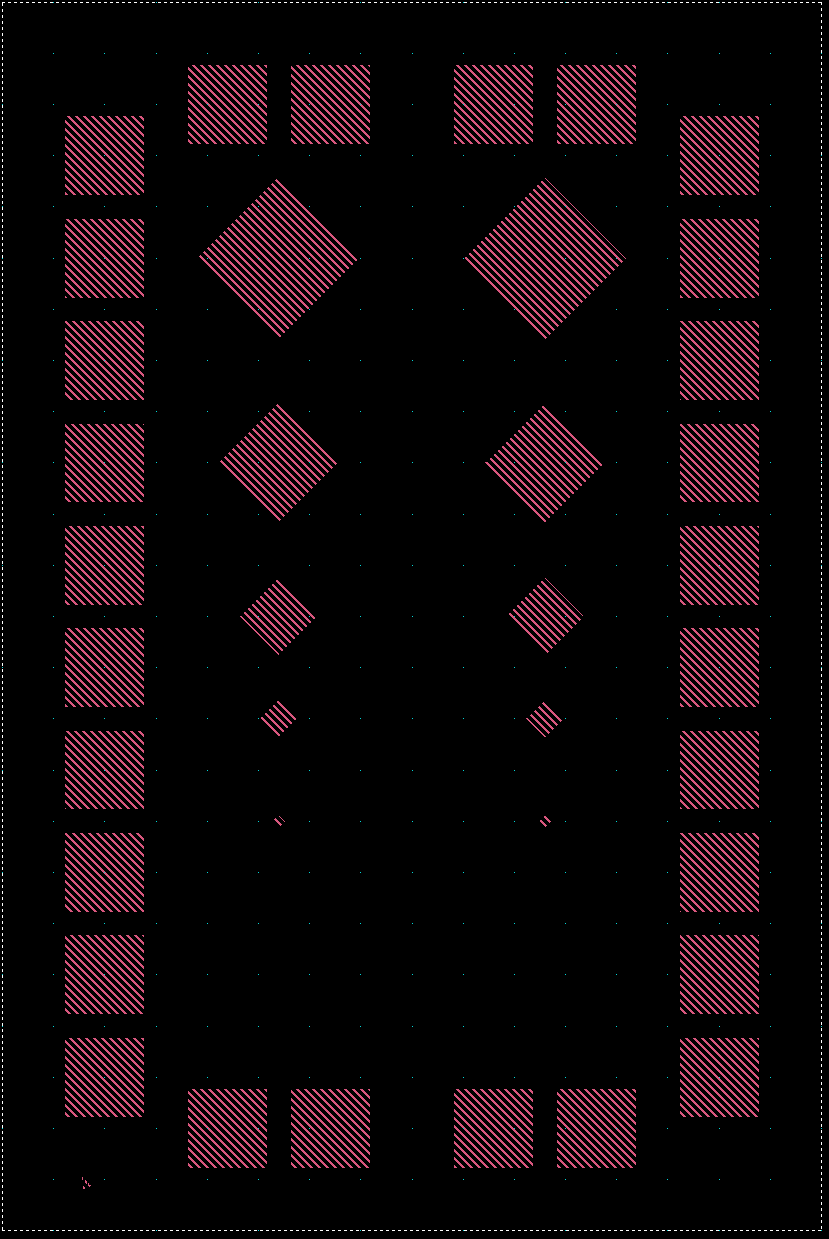
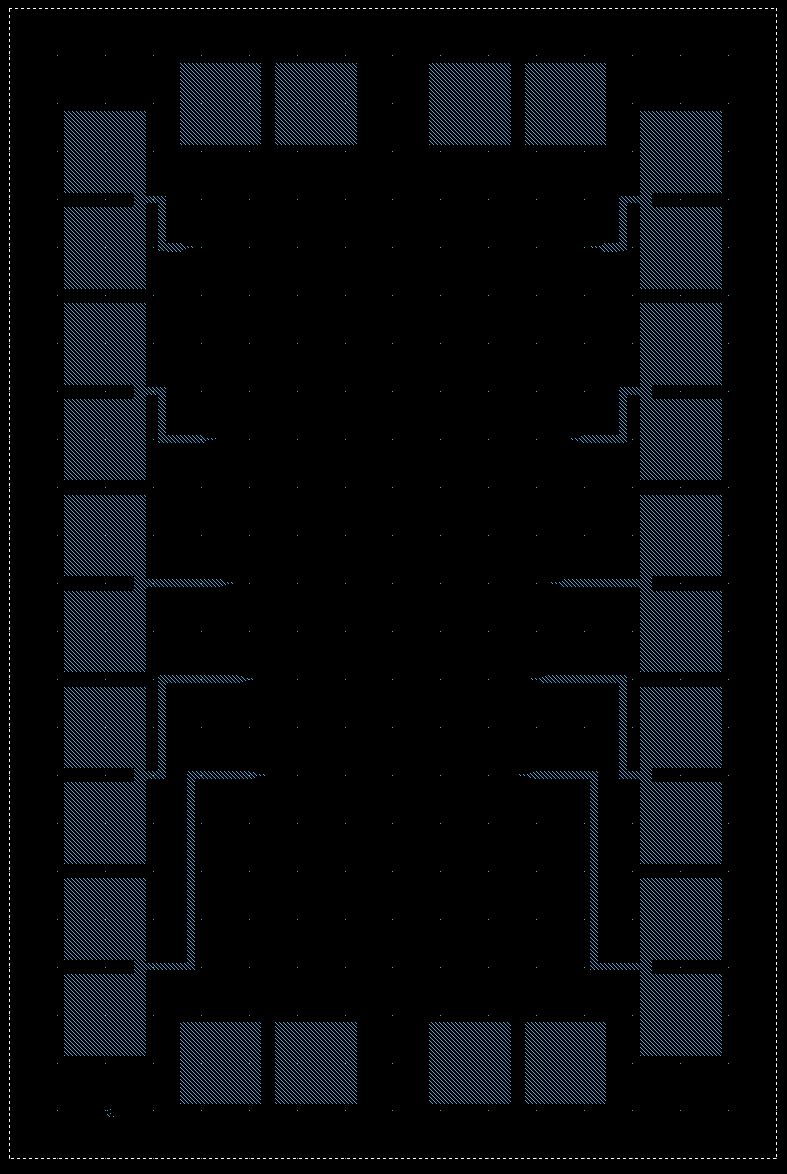
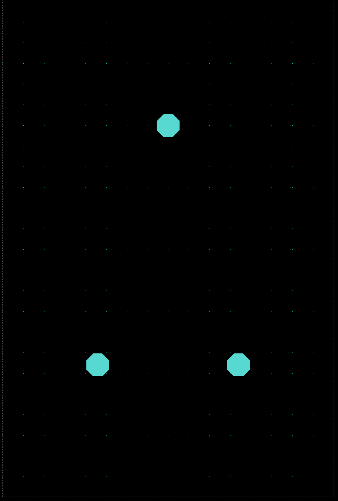
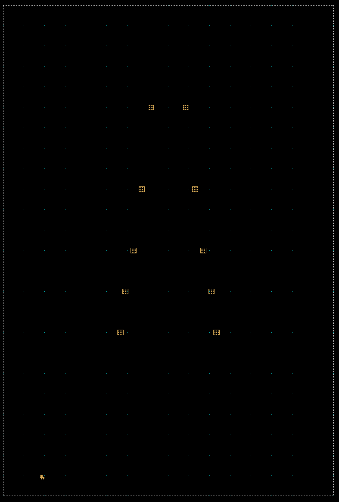
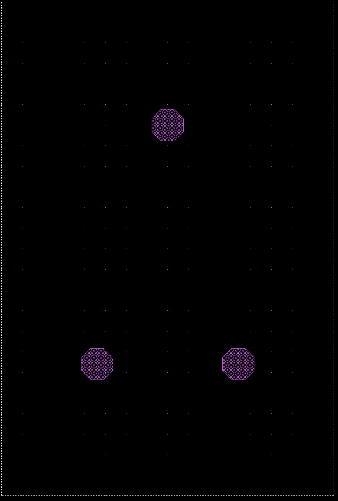
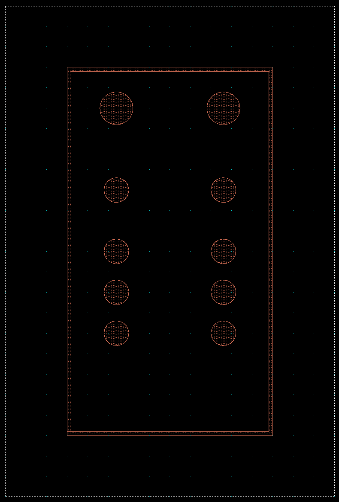
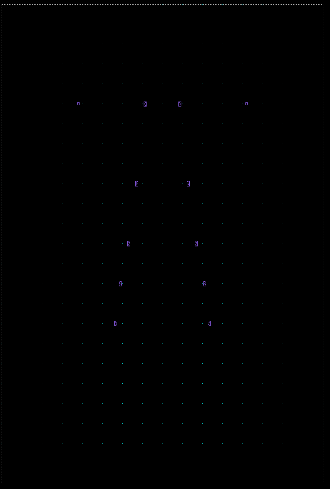
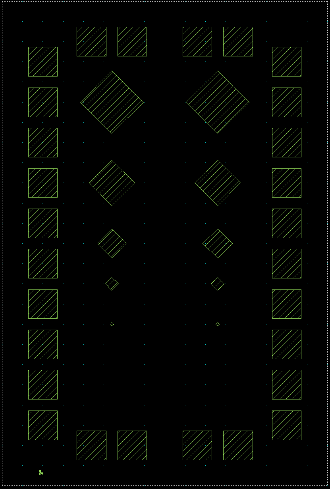
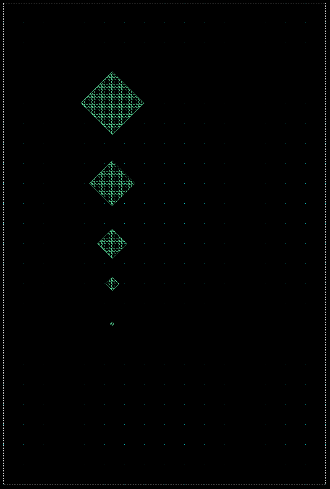
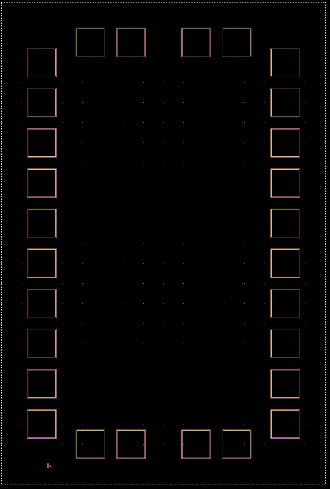
Selective Aluminum Etch Process (SAEP) – Spencer’s notes

Starting material: Si wafer, DSP, with thermal oxide (100 nm) and LPCVD nitride (500 nm).

1. Deposit Al trilayer, Al(265)/Al-Ox/Al(60) (thickness in nm).  
   1. 0300 – (Dark/+) – Defines device sizes
   2. Resist remains where mask was
   3. ***Subsequent Al deposition would be incorrect***

1. Pattern base electrode layer, wiring and pads with resist mask, and ion mill through top Al layer; strip resist.  
   1. 0400 – (Dark/+) – Slightly smaller than 0300
   2. ***What electrodes?***
2. Pattern top electrode layer with resist mask, ion mill down to base layer and to clear field areas, anodize to 50V; strip resist.  
   1. 0800 – (Dark/-) – Same size as 0300
   2. Resist removed where mask was
   3. ***Top layer Nb wires made: makes sense***
3. Pattern lift-off mask for Nb wiring and pads, deposit Nb, 600 nm, and lift off.  
   1. 1200 – (Clear/+) – Smaller than 1400
   2. ***Out of order? What are these?***

1. Pattern resist mask with windows over anodized Al base wiring where Nb plugs will be deposited, ion mill to remove anodized Al and most of underlying Al (depth TBD); strip resist.   
   1. 0900 – (Dark/-) – Wide, over ground wire but not devices
   2. ***Purpose unknown***
2. Pattern lift-off mask for Nb plugs, mill through exposed anodized Al and into Al, clear Al from step 5 etch, deposit Nb plugs, 300 nm, and lift off.   
   1. 1400 – (Dark/-) – Wider than 1200
3. Pattern lift-off mask for Au pads, deposit Au, 300 nm, and lift off.   
   1. 1000 – (Dark/-) – Definitely collimators
   2. ***Definitely the collimator layer***
4. Pattern lift-off mask for Pb absorbers, deposit Pb, thickness TBD, lift off.
   1. ***No 18 – 0A00?***
5. Spin coat wafer with SU-8, thickness TBD, and pattern collimator posts.
   1. ***Must be 1400/1200? Are those the posts?***
6. Bond wafer to backing wafer, face down, pattern backside resist mask, etch through wafer to release membranes; remove die from backing wafer and clean.
   1. ***New – make this.***
7. ??  
   1. 0E00/0F00 – () – 0E00 Same as 0500
   2. 0A00 – () –
   3. ***Lead mask? Dark/- would be my guess***
   4. 0C00 – (??) – Narrower than 0900
   5. ***Purpose unknown***
   6. 0500 – (??) – Slightly smaller than 0400
   7. ***Purpose unknown***

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **CAD Layer** | **GDS** | **Sequence** | **Digitized Data** | **Resist Polarity** | **Description** |
| Tri | 3 | 1 | Dark | Pos | Trilayer etch |
| Anod | 4 | 2 | Dark | Pos | Top electrode etch and anodization |
| Nb | 8 | 3 | Dark | Neg | Nb wiring |
| Pass | 12 | 4 | Clear | Pos | Plug etch |
| I2 | 9 | 5 | Dark | Neg | Nb plugs |
| Au | 14 | 6 | Dark | Neg | Au pads |
| Ta | 10 | 7 | Dark | Neg | Pb absorber |
| SU8 | 18 | 8 | Clear | Neg | SU8 posts |
| Col | 16 | - | Dark | Pos | Collimator |
| Key | 20 | - | Clear | Pos | Key etch for collimators |
| DE | 7 | 9 | Clear | Pos | Deep etch to release membranes |
| PVIA | 15 | - | Clear | Pos | Pad etch (not used) |