# Name: \_\_\_\_\_\_\_\_\_\_

# Netid: \_\_\_\_\_\_\_\_\_\_\_

1. Design Part 1. (40 pts)
   1. Design passes Post Implementation Timing simulation (16 pts)
   2. Post Implementation Timing simulation screenshot: (4 pts)
   3. Timing Analysis screenshot (4 pts)
   4. Logic Utilization Tables (4 pts) :
   5. Schematic screenshot (4 pts)
   6. Floorplan screenshot (LUT selected) (4 pts)
   7. Floorplan screenshot with routing (4 pts)
2. Correct Design part 2 (30 pts)
   1. Design passes Post Implementation Timing simulation (14 pts)
   2. Timing Analysis screenshot: (4 pts)
   3. Utilization tables – be sure to include the DSP table!: (4 pts)
   4. Schematic Screenshot (4 pts):
   5. Floorplan screenshot with routing displayed (4 pts):
3. Question (5 pts): From the timing analysis data for both designs, would you say that routing delay is a SIGNIFICANT or INSIGNIFICANT part of the delay?
4. Which design used fewer LUTs and why? (5 pts)
5. Question (10 pts)

For the following multiplication, write the hex values for the two operands encoded as 1.7 signed numbers, and for the result as 2.14 number.

-0.7421875 x 0.8671875 = -0.64361572265625

1. Question (10 pts)

What is the decimal result of the following multiplication if these hex numbers are signed 2.6 numbers?

0xA4 x 0x70 = ????