# Name: \_\_\_\_\_\_\_\_\_\_

# Netid: \_\_\_\_\_\_\_\_\_\_\_

1. Correct Design part 1 (40 pts)
2. Correct Design part 2 (25 pts)
3. Correct Design part 3 (25 pts) with TA checkoff, design resources (Slice Logic, Summary of Registers by Type)
4. (10 pts) Timing Analysis, part 3. Capture a screen shot from the timing analysis of the implemented design that gives the worst slack for Intra-clock paths for our 50 MHz clock (clk\_out1\_clk\_wiz). This design is supposed to run at 50 MHz. Could this design run at 100 MHz based on the slack in the timing report (explain your answer in order to get credit, you cannot just say ‘yes’ or ‘no’).