# Name: \_\_\_\_\_\_\_\_\_\_

# Netid: \_\_\_\_\_\_\_\_\_\_\_

1. Correct Design part 1 (90 pts)
2. Implementation tables – Slice Logic Table, Memory table (5 pts) – This is the first time your design has had Memory, so the Memory table will show that a block RAM tile is used.
3. Question (5 pts): For your design, assume the write counter value is "3", and the read counter value is "6". How many elements are in the FIFO?