ECE 310L: Microelectronic Circuits Lab

Lab 7: MOSFET Logic Circuits

Name:

Lab partner:

Objectives

(1) Experimentally verify the operation of NMOS, PMOS, and CMOS inverters.
(2) Design and verify simple logic circuits.

Background

A large number of circuits depend upon rapidly switching the current to a load to minimize the losses in the active elements, the transistors. These switching circuits range from DC-DC switch mode power converters to digital logic circuits that switch between a logic 1 and logic 0.

Rather than linearly varying the voltage applied to a load, many power conversion circuits will control the average amount of energy transferred to a load by rapidly switching the current supplied to the load on and off. A transistor is used as a switch to control the current to the load, producing an average output that is proportional to the on-time divided by a constant switching period. The transistor on-time is varied to control the amount of power delivered to the load. (This process is referred to as pulse-width modulation, or PWM.) The power loss in the transistor switch is minimal when it is full-on or full-off as long as the voltage drop across the transistor is low during the on-state and the current is low during the off-state.

Logic circuits also depend on switching an output between a high and low voltage (i.e. the supply voltage and ground) to produce the logic 1 and logic 0 states.

The metal-oxide silicon field effect transistor (MOSFET) does an excellent job acting as a switch. The FET displays a very low on-resistance, $R_{DS(on)}$ or R_{on}, in the on-state, and a very small leakage current in the off-state. CMOS (Complementary MOS) logic takes advantage of these low on resistances and uses both PMOS and NMOS transistors to produce logic levels very close to the supply voltage and ground.

This lab will study both NMOS and PMOS transistors as switches. We will also investigate how multiple switches can be used to implement simple Boolean functions (e.g. NOT, NAND, and NOR.).

NMOS Inverter

Logic inverter is one of the most basic logic circuit. An inverter circuit outputs a voltage representing the opposite logic-level to its input. In digital logic, an inverter circuit implements logical negation. In practice, actual devices have non-ideal electrical characteristics that must be carefully considered when designing inverters. In fact, the non-ideal transition region behavior of a MOSFET inverter makes it useful in analog electronics as a class A amplifier (e.g., as the output stage of an operational amplifier).

Inverters can be constructed using a single NMOS transistor or a single PMOS transistor coupled with a resistor. Figure 1 shows a simple open-drain logic inverter (or a low-side switch). Since this ‘resistive-drain’ approach uses only a single type of transistor, it can be fabricated at

low cost. When the gate voltage is below the NMOS threshold (logic low state), the transistor is OFF, the output voltage depends on the ratio of pull-up resistor R_p and the load. In the case of an open load as shown in Fig. 1, the output voltage will be V_{DD} = 5 V (logic high state). The transient from output low to high state is shown in left pane of Fig. 2. The transient time, also known as gate response time is determined by the time to charge C_L through the pull-up resistor, R_p, $t_r \approx R_p$ (C_{FET} + C_{probe} + C_L), where C_{FET} is the capacitance of the NMOS junction and C_{probe} is the capacitance of the probe during the measurement with an oscilloscope.

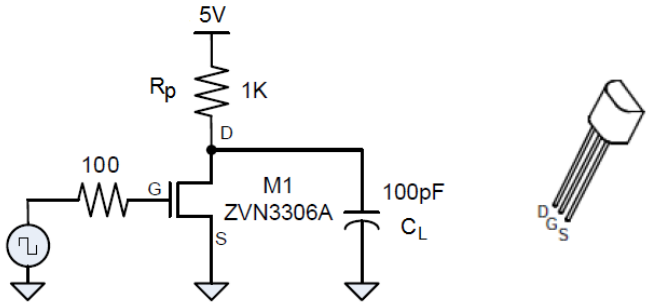


Figure 1. Open-drain logic inverter circuit (NOT gate) using a NMOS.

When the gate voltage is above the NMOS threshold, the transistor is ON, the output voltage can be calculated from a resistive voltage divider formed by the pull-up resistor R_p (1 KΩ in Fig. 2) and the on-resistance R_{on} of the MOSFET,

$$V_L = V_{DD}\frac{R_{on}}{R_{on}+R} \tag{1}$$

where R_{on} can be estimated theoretically by

$$R_{on} = \frac{V_{DS}}{I_D} = \frac{V_{DS}}{K_n'\frac{W}{L}\left(V_{GS}-V_{TN}-\frac{V_{DS}}{2}\right)} \tag{2}$$

In this lab, we will attempt to make an experimental estimation. Obviously, R_{on} must be smaller than R in order for V_L to be small. It is important to recognize that R_{on} represents a nonlinear resistor because the value of R_{on} is dependent on V_{DS}, the voltage across the resistor terminals. The logic gate output is in the low state.

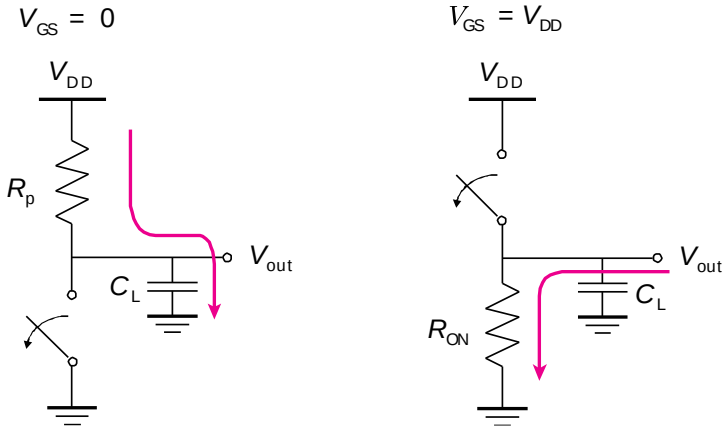


Figure 2. The switching dynamics of the NMOS inverter.

The transient from output high to low state is shown in right pane of Fig. 2. The gate response time is determined by the time to discharge C_L through the on-resistance of NMOST transistor, R_{on}, $t_f = R_{on}$ ($C_{FET} + C_{probe} + C_L$). By measuring the falling edge t_f, the on-resistance of the MOSFET can be estimated.

PMOS Inverter

An inverter can also be built with a PMOS transistor, as shown in Figure 3. This is also called a high-side switch, since the switching element is on the high side of the voltage rails.

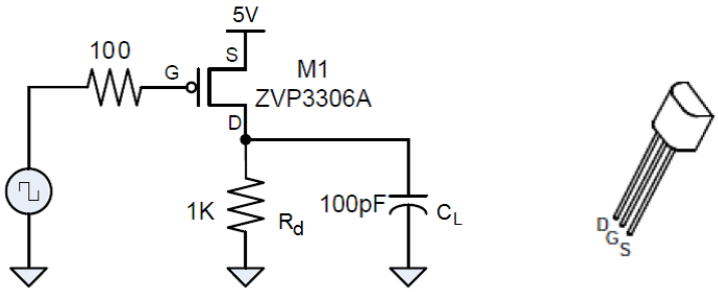


Figure 3. High-side switch inverter circuit (NOT gate) using a PMOS. Pay attention how the locations of S and D differ from NMOS in Fig. 2.

CMOS Inverter

Both of the previous circuits only have a single transistor which actively drives the output when the transistor is on. When the transistor is off, a pull-up (NMOS) or pull-down (PMOS) resistor causes the output to assume a high or low state, respectively. The relatively high resistance results in a much slower output transition than the low on-resistance of the transistor provides. To actively drive the output in both directions, we combine the NMOS and PMOS transistors to create a complementary MOS (or CMOS) inverter, as shown in Fig. 4.

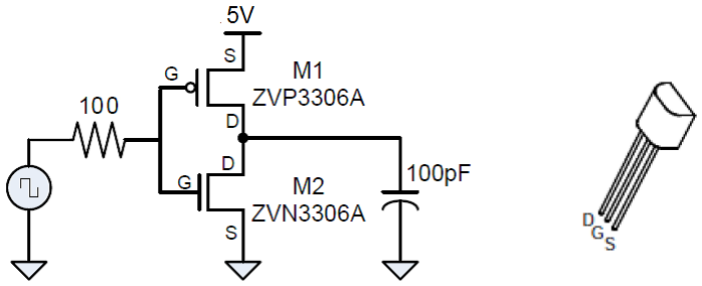


Figure 4. CMOS logic inverter circuit.

Boolean Logic Circuit

By adding more transistors as illustrated in Fig. 5, we can create Boolean functions rather than just inverters. These circuits form the basis for implementing digital logic.

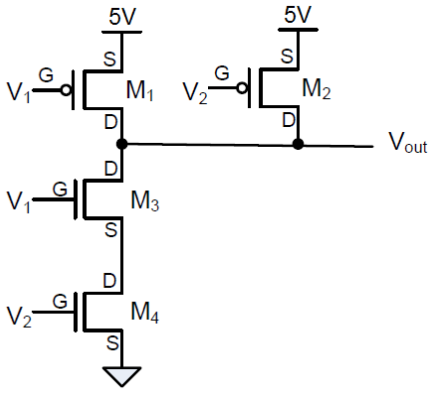
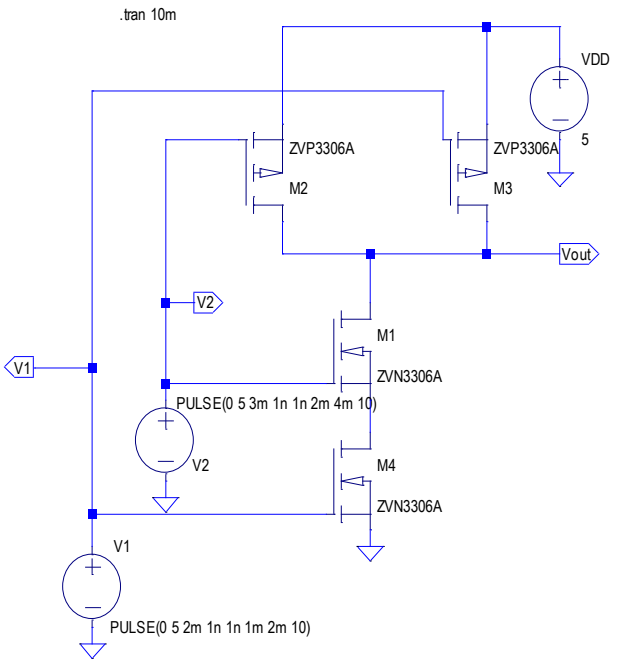


Figure 5. A 2-input Boolean circuit. The Boolean function will be identified in the lab assignment.

Figure 6 shows the LTspice model of the Boolean circuit shown in Fig. 5. Notice the orientation of the PMOS transistors. Since the source terminal is internally tied to the substrate, the drain and source are not interchangeable.

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.SUBCKT ZVP3306A 3 4 5
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M1 3 2 5 5 P3306M
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RL 3 5 1.2E8
C1 2 5 28E-12
C2 3 2 3E-12
D1 3 5 P3306D
*
.MODEL P3306M PMOS VTO=-2.875 RS=5.227 RD=7.524 IS=1E-15 KP=
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Figure 6.LTspice model of the 2-input Boolean circuit shown in Fig. 5.

LTspice internally includes a small number of NMOS and PMOS transistors. To introduce a new transistor, a sub-circuit is typically needed as shown in Fig. 6. A sub-circuit allows you to define a collection of elements as one element (e.g. a MOSFET and an Op-Amp) and to insert this description into the overall circuit. A sub-circuit is defined by a .SUBCKT control statement, followed by the circuit description. Both NMOS and PMOS transistors used in this lab can be found at www.diodes.com. Figure 6 shows the op codes for them.

To use these sub-circuits, left click the component while pressing the Ctrl key. A component attribute editor will show up as shown in Fig. 7. Change the Prefix to “X” so that LTspice will look for external SUBCKT control statements. Change the Value to the appropriate SUBCKT name, in this case, ZVP3306A.

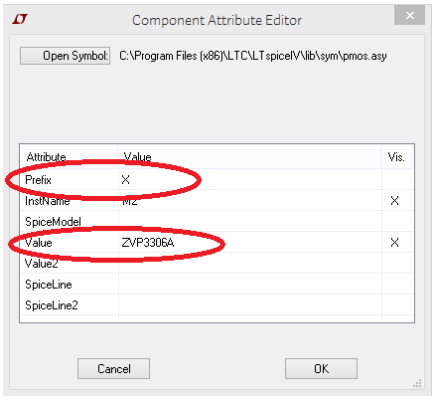

Figure 7. Component attribute editor for LTspice element

The logic function of a Boolean circuit is best modeled by a transient simulation. The inputs V_1 and V_2 are wave sequences that produce binary code (V_2 V_1) of 00, 01, 10, and 11 at 1, 2, 3, and 4 ms, respectively. V_2 is assumed as the most significant digit. The output waveform V_{OUT} indicates the logic function of the circuit.

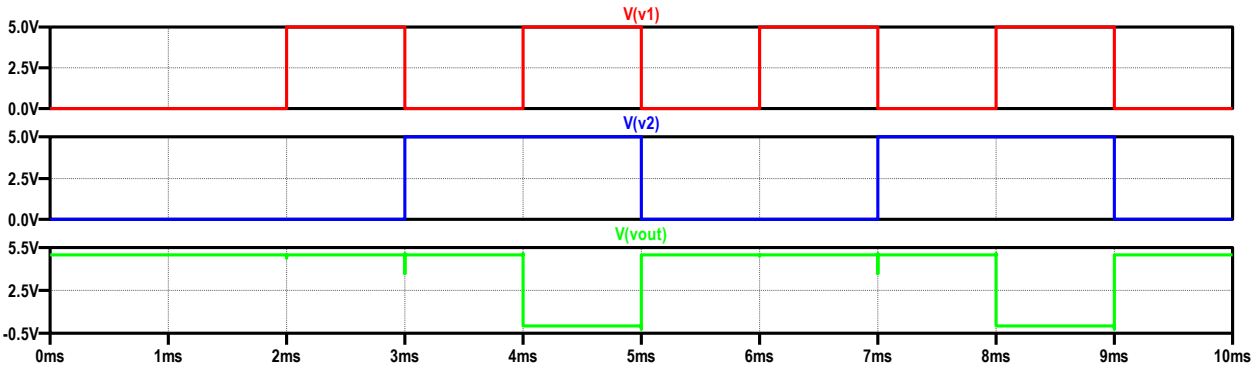

Figure 8. The waveform sequence of the Boolean circuit shown in Fig. 5 and 6.

A truth table can be produced from the waveform in Fig. 8, as shown in Table 1.

Table 1. Truth Table for the Boolean Circuit

V_1 \ V_2	0	1
0	1	1
1	1	0

Materials:

- DC Power supply, HP E3631A
- Oscilloscope, Agilent DSO5014A
- Signal generator, Agilent 33220A
- DMM, Agilent E3631A
- Solderless breadboad
- Hookup wires
- Resistors: 1 KΩ, 10 KΩ
- Transistors: ZVN3306A (2), ZVP3306A (2)
- Capacitor: 100 pF ceramic

Setup

Turn on power to the DMM, oscilloscope, power supply, and signal generator. Set the power supply +25V current limit to 50mA.

You will be constructing several circuits. Pay careful attention to the pin-out of the transistors to avoid damaging them. The NMOS and PMOS parts have the same pin out, as shown in Figure 1.

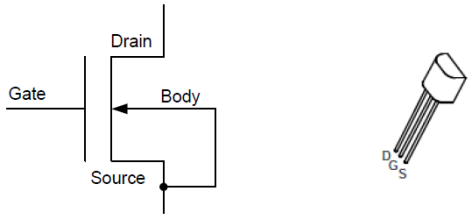

Figure 9. Pin layout for NMOS and PMOS used in the lab.

Since the source terminal is internally tied to the substrate, the drain and source are not interchangeable.

Pre-lab Assignments

Question 1. For the circuit shown in Fig. 1, draw the load line on the *I*−*V* characteristic of ZVN3306A shown in Fig. 10 where V_{GS} is varied from 0 V to 5 V at a step of 0.5 V (not all V_{GS} are labelled on the plots).

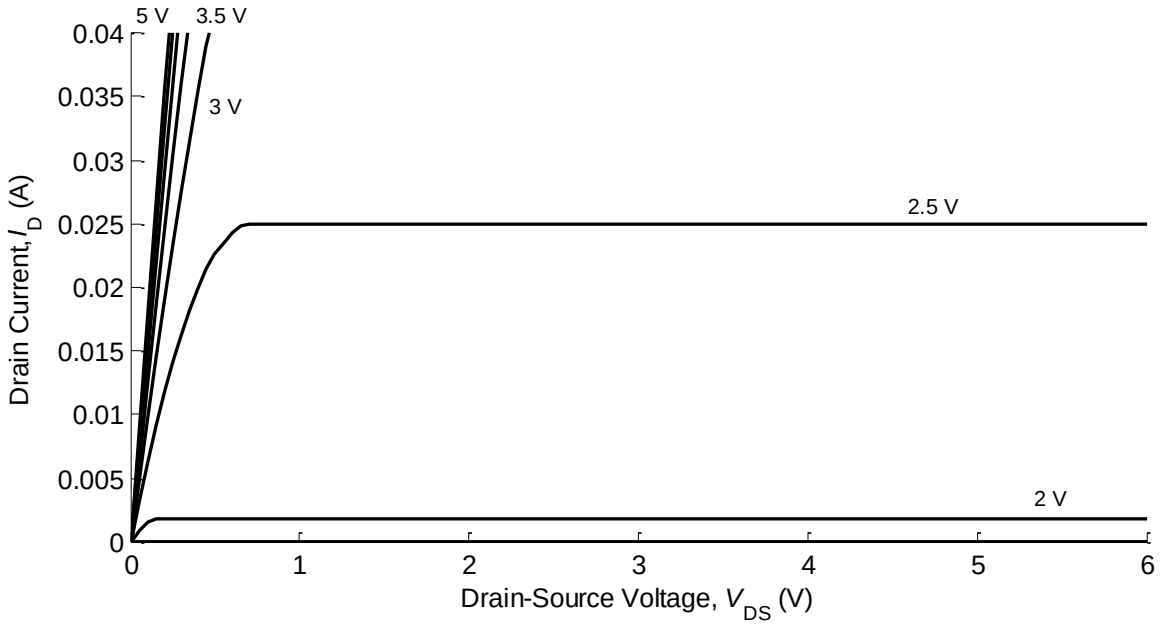

Figure 10. The *I*–*V* characteristic of ZVN3306A NMOS transistor.

Show the equation for the load line in the space given below. From the load line draw on Fig. 10, determine V_{DS} (V_{DS} is also the output voltage) when the transistor is ON with V_{GS} at 5 V.

Question 2. Given the on-resistance of a ZVN3306A NMOS transistor is 10 Ω at V_{GS} = 5 V and I_{DS} = 100 mA, what is the transient time of switching from 0 V to 5 V and from 5 V to 0 V for the inverter circuit shown in Fig. 2. Which is shorter?

Question 3. Show the charging and discharge path for the PMOS inverter circuit shown in Fig. 3. Which transient time is shorter, switching from 0 V to 5 V and from 5 V to 0 V? Explain.

Question 4. Design a CMOS 2-input NOR circuit. Draw a schematic diagram in the space below and simulate the circuit with LTspice.

Lab Assignments

1. Use the DMM to measure the values of all resistors. Use the measured resistor values in your calculations. Use the RLC meter to measure the capacitor.

Table 1. Measured Capacitance and Resistance

Expected Value	C = 100 pF	R_1 = 1 KΩ	R_2 = 100 Ω
Measured Value	pF	KΩ	Ω

2. Construct the NMOS inverter/low-side switch as shown in Fig. 1, except set the supply voltage in all circuits to 5 V instead of 3.3 V.
3. Set the signal generator to produce a 0−5 V square wave at 10 KHz.
4. Verify that the output is inverted compared to the input. Show the traces of input and output waveforms of at least two periods on the same plot below.

5. Zoom in to the rising edge of the output waveform. Show the traces of input and output waveforms in an appropriate timebase so that the rise time can be accurately measured. The times should be measured from 10% to 90% of the total voltage swing (5 V). Measure and record the rise time of the output in the space below. Verify that the rise

time matches the expected value given the capacitive load and the pull-up resistor. Note that rise/fall time from 10% to 90% is about 2.2 times the time constant.

6. Repeat step 5 to measure and record the fall time of the output. Calculate the on-resistance of the FET based on the fall time. Clearly show your calculation steps. Compare your calculated value to the datasheet value.

7. Reduce the amplitude of the input signal (keeping the lower value at 0 V) until the output stops switching. Record the value and how does it compare to the threshold voltage (V_{TN}) given in the datasheet.

8. Construct the PMOS inverter/high-side switch shown in Fig. 3. Repeat the measurements as were done in step 4-6, as appropriate for the PMOS high-side switch topology. Analyze the results and compare them with the NMOS inverter. Only show the traces around the rising and falling edges.

9. Reduce the amplitude of the input signal (keeping the lower value at 0V) until the output stops switching. Record the value, and compare to the threshold voltage (V_{TP}) given in the datasheet. Remember that V_{TP} is specified as the voltage from the gate to source voltage (5 V).

10. Construct the CMOS inverter shown in Fig. 4. Repeat the measurements as were done in step 4-6. Summarize your observation.

11. Construct the CMOS 2-input logic gate shown in Figure 5. Connect the inputs labeled V_1 together, and connect the inputs labeled V_2 together. Connect the inputs to all possible combinations of logic 0 (ground) and logic 1 (5 V), and record the output voltage and its corresponding logic value. Create a truth table and show the measurement results verifying the type of gate that was created.

12. Build the 2-input NOR circuit designed in the pre-lab assignment 1. Connect the inputs to all possible combinations of logic 0 (ground) and logic 1 (5 V), and record the output voltage and its corresponding logic value. Create a truth table and show the measurement results verify the type of gate that was created.