ECE 310L: Microelectronic Circuits Lab

Lab 6: Switch-Mode Power Supply

Name: Changyu Guo

Lab partner: Joe McCarver

Objectives

(1) Experimentally verify the operation of a buck switch-mode power supply.
(2) Understand the effects of duty cycle and load on the output voltage.

Background

Switch-mode power supplies (SMPS) use reactive elements (inductors and/or capacitors) and solid-state switches to create output voltages that can be greater than or less than the input voltage. If the output voltage is greater than the input voltage, we refer to the SMPS as a boost converter. If the output voltage is less than the input voltage, we refer to the SMPS as a buck converter. A buck converter is a voltage step down and current step up converter.

In lab 1, we have shown that a simple line regulator circuit (e.g., Zener diode circuit) has the ability of producing an output voltage lower than the input power supply. But such linear regulators waste energy as they operate by dissipating excess power as heat. Buck converter operates at a much higher efficiency (typical 95% or above), and have supplanted linear regulators in many applications. It is useful for tasks such as converting the main voltage in a computer (12 V in a desktop, 12-24 V in a laptop) down to the 0.8-1.8 volts needed by the processor.
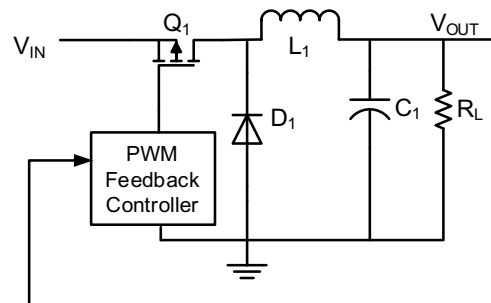

Figure 1. Schematic of a switch-mode power supply

A simplified buck converter is shown in Figure 1. The PMOS FET is operated as a high-side switch at a variable duty cycle. When the FET is on, current flows from the supply through the inductor to the output capacitor and load. During this phase of operation, the inductor develops a voltage drop that opposes (or bucks) the supply, hence the name buck converter. When the FET is then turned off, the inductor acts as a source and delivers current to the output capacitor and load through the diode. The switching frequency is chosen to ensure that the inductor current can only reach a desired peak value. The duty cycle applied to the PMOS transistor is

then varied by a feedback control system to produce a constant output voltage in the presence of changing load current.

The buck converter that you will build in the lab is shown in Figure 2. It will not have a feedback control system and will operate at a constant load. In this lab, you will vary the duty cycle and observe the effect on the output voltage. You will also vary the load with the duty cycle held constant.
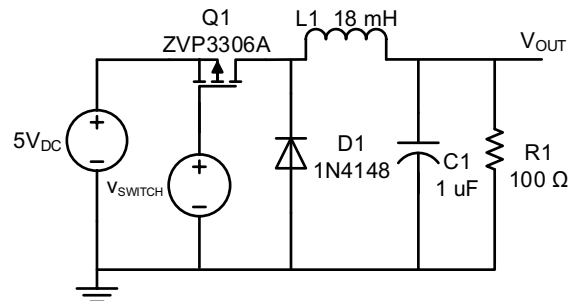

Figure 2. A constant load, open feedback swith-mode power supply

In this lab, we will also learn how to model MOSFET in LTSPICE. LTspice internally includes a small number of NMOS and PMOS transistors. To introduce a new transistor, a sub-circuit is typically needed. A sub-circuit allows you to define a collection of elements as one element (e.g. a MOSFET and an Op-Amp) and to insert this description into the overall circuit. A sub-circuit is defined by a .SUBCKT control statement, followed by the circuit description. Both NMOS and PMOS transistors used in this lab can be found at www.diodes.com. The following is the op codes for ZVP3306A.

```
*ZETEX ZVP3306A Spice Model v1.1 Last Revised 3/5/00
   *
   .SUBCKT ZVP3306A 3 4 5
   *              D G S
   M1 3 2 5 5 P3306M
   RG 4 2 252
   RL 3 5 1.2E8
   C1 2 5 28E-12
   C2 3 2 3E-12
   D1 3 5 P3306D
   *
   .MODEL P3306M PMOS VTO=-2.875 RS=5.227 RD=7.524 IS=1E-15 KP=.145
   +CBD=35E-12 PB=1 LAMBDA=6.67E-3
   .MODEL P3306D D IS=5E-12 RS=.768
   .ENDS ZVP3306A
   *
```

To use these sub-circuits, first pick a PMOS circuit component and place it on workspace. Left click the component while pressing the Ctrl key. A component attribute editor will show up as shown in Fig. 3. Change the Prefix to "X" so that LTspice will look for external SUBCKT control statements. Change the Value to the appropriate SUBCKT name, in this case, ZVP3306A. Please pay attention to the orientation of the PMOS transistors. Since the source terminal is internally tied to the substrate, the drain and source are not interchangeable.
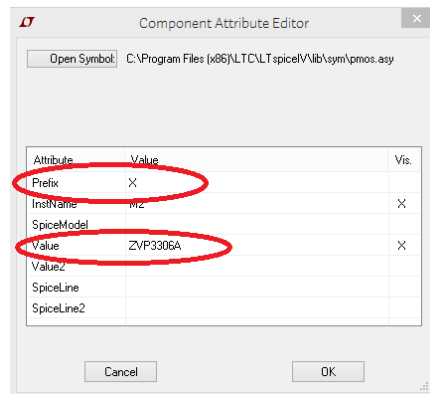
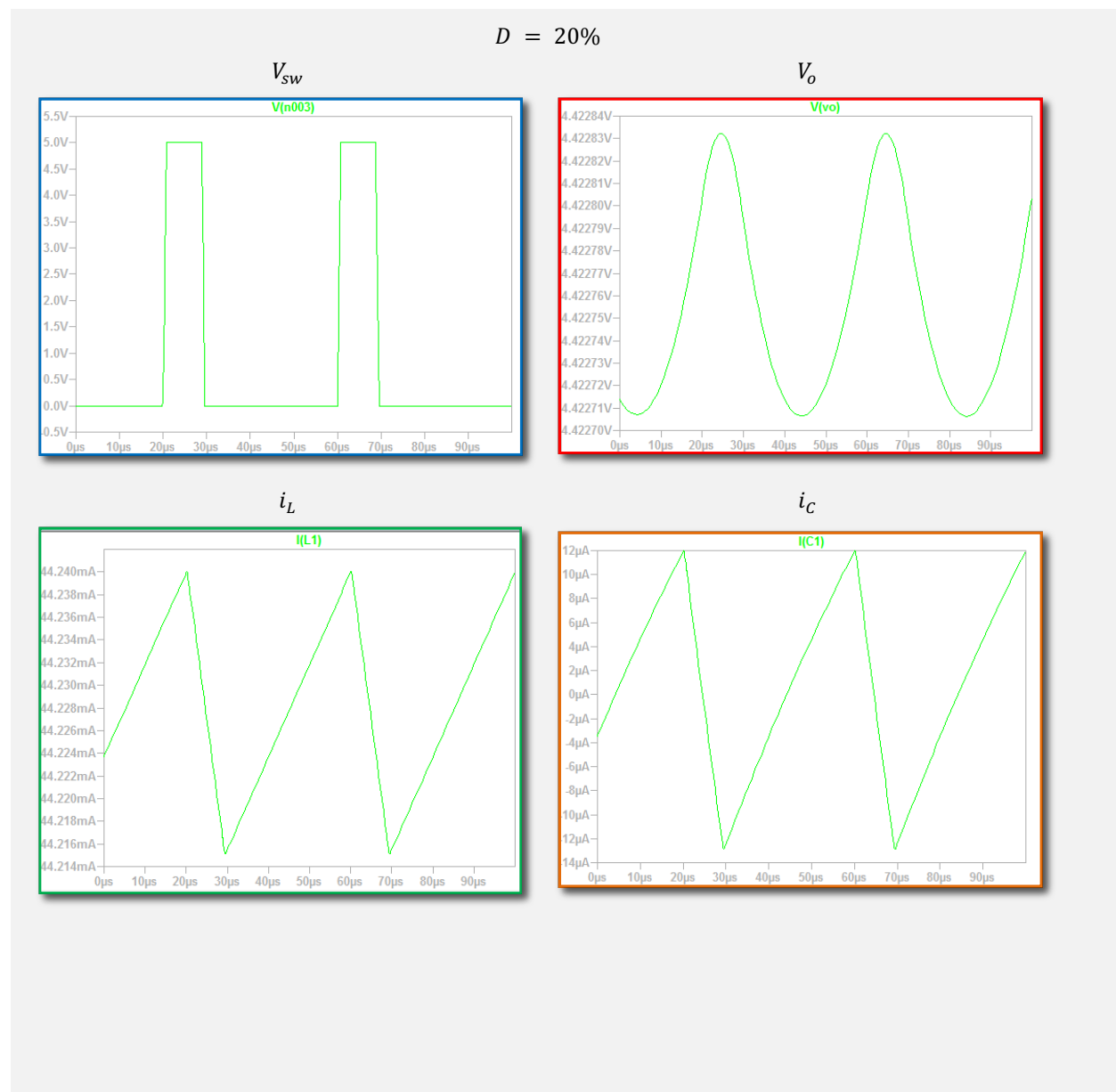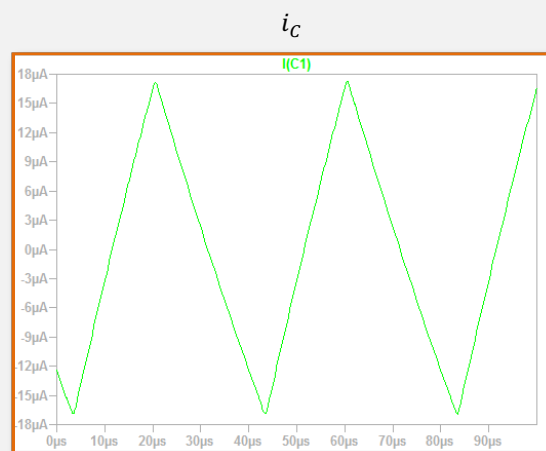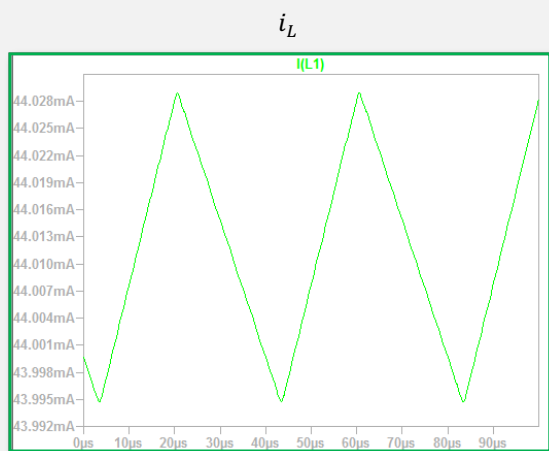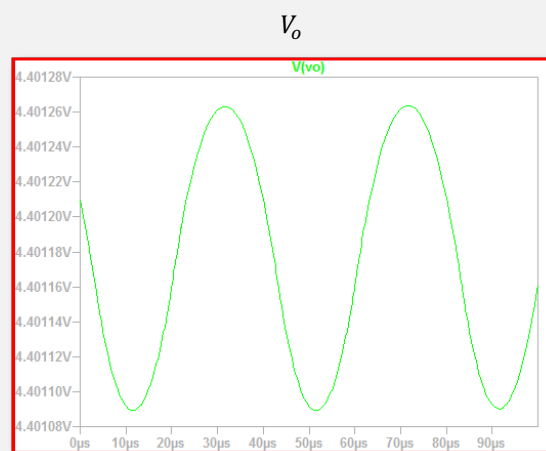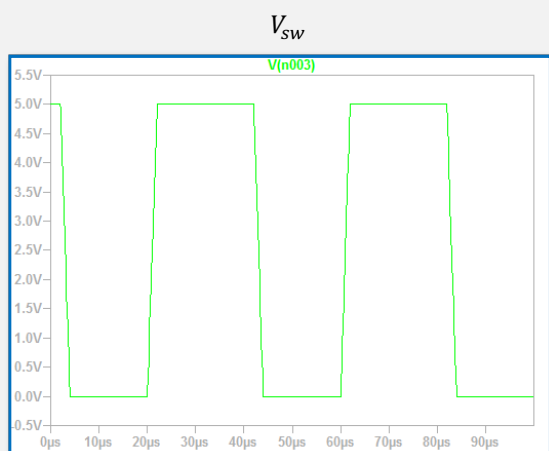Figure 3. Component attribute editor for LTspice element

Materials

- DC power supply, HP E3631A
- Oscilloscope, Agilent DSO5014A
- Signal Generator, Agilent 33220A
- DMM, Agilent E3631A
- Solderless breadboad
- Hookup wires
- Resistors: 100Ω (3)
- Capacitor: 1uF tantalum
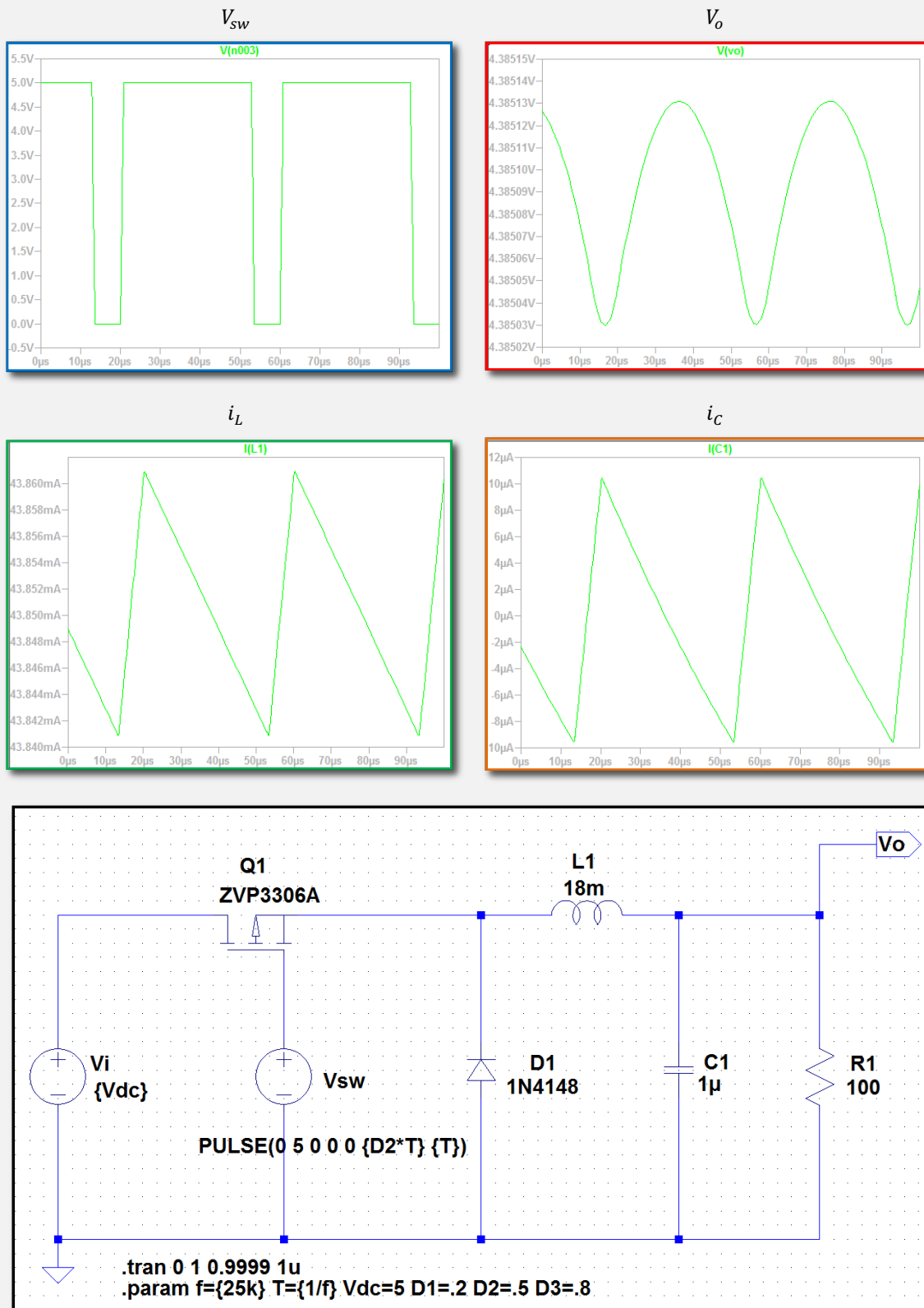- Inductor: 18mH
- Diode: 1N4148
- Transistors: ZVP3306A

Pre-lab Assignment

Question 1: Simulate the circuit in Fig. 2 in LT SPICE for v_{SWITCH} = 0–5V rectangular wave at 25 KHz. Set the v_{SWITCH} symmetry so as to cause the PMOS transistor to operate at duty cycles of 20%, 50%, and 80%. Remember that the PMOS transistor is on when v_{SWITCH} is 0V. Show your waveforms for each simulation run (20%, 50%, and 80%) showing v_{SWITCH}, i_L, i_C, v_{OUT} for just a couple cycles of v_{SWITCH} in <u>steady-state</u>. Note that it will take about 1 millisecond for the circuit to reach steady-state.

By default, an LT SPICE transient simulation will determine a DC operating point for the circuit and then run the transient simulation from that point. So, you will get a very different initial condition depending on whether you set v_{SWITCH} high or low to start. Be sure to select the "Skip initial operating point solution" option on the Transient tab of the Edit Simulation Command dialog.

$$D = 20\%$$

$$D = 50\%$$

V_{sw}

V_o

i_L

i_C

$$D = 80\%$$

V_{sw}

V(n003)

5.5V
5.0V
4.5V
4.0V
3.5V
3.0V
2.5V
2.0V
1.5V
1.0V
0.5V
0.0V
-0.5V
0µs 10µs 20µs 30µs 40µs 50µs 60µs 70µs 80µs 90µs

V_o

V(vo)

4.38515V
4.38514V
4.38513V
4.38512V
4.38511V
4.38510V
4.38509V
4.38508V
4.38507V
4.38506V
4.38505V
4.38504V
4.38503V
4.38502V
0µs 10µs 20µs 30µs 40µs 50µs 60µs 70µs 80µs 90µs

i_L

I(L1)

43.860mA
43.858mA
43.856mA
43.854mA
43.852mA
43.850mA
43.848mA
43.846mA
43.844mA
43.842mA
43.840mA
0µs 10µs 20µs 30µs 40µs 50µs 60µs 70µs 80µs 90µs

i_C

I(C1)

12µA
10µA
8µA
6µA
4µA
2µA
0µA
-2µA
-4µA
-6µA
-8µA
10µA
0µs 10µs 20µs 30µs 40µs 50µs 60µs 70µs 80µs 90µs

Vo

Q1
ZVP3306A

L1
18m

Vi
{Vdc}

Vsw

D1
1N4148

C1
1µ

R1
100

PULSE(0 5 0 0 0 {D2*T} {T})

.tran 0 1 0.9999 1u
.param f={25k} T={1/f} Vdc=5 D1=.2 D2=.5 D3=.8

Super Professional LTSpice Model used for Simulations

From the LT SPICE results, record the output voltage, V_{OUT}, and the peak-to-peak ripple voltage, V_{RIPPLE}, when the circuit reaches the steady state.

Table 1. The output voltage and peak-to-peak voltage ripple for Buck Converter as a function of duty cycle

Duty Cycle	20%	50%	80%
V_{OUT} (V)	4.42	4.40	4.385
V_{RIPPLE} (mV)	0.125	0.174	0.100

Question 2: On the figure below, draw the complete current path when v_{SWITCH} is at 0 V, assuming the converter is operating in steady-state. Label the current path in red with an arrow indicating the current direction. Explain. Is MOSFET on or off?
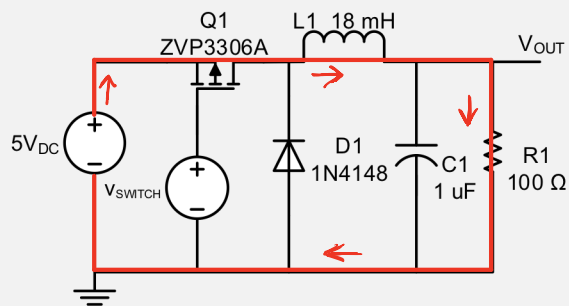

Figure S4. The current path for buck converter for v_{SWITCH} = 0 (FET is on). The current path is shown in **red** with an arrow indicating the direction.

A PMOS transistor conducts when the gate voltage is small, so at zero the transistor is conducting

Question 3: On the figure below, draw the complete current path when v_{SWITCH} is at 5 V, assuming the converter is operating in steady-state. Label the current path in blue with an arrow indicating the current direction. Explain. Is MOSFET on or off?
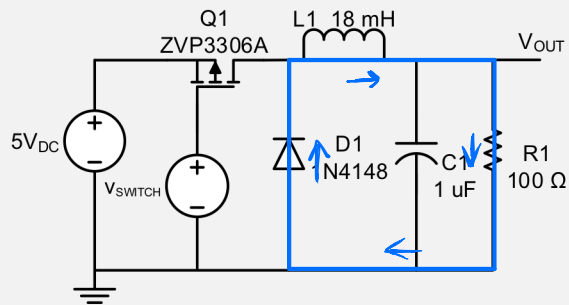

Figure S5. The current path for buck converter for v_{SWITCH} = 5 (FET is off). The current path is shown in **blue** with an arrow indicating the direction.

Conversely, it stops conducting when the gate voltage is raised

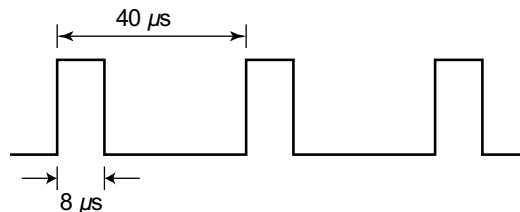Question 4: For the waveform showing in the Fig. 3 below,

Figure 3. Waveform of a rectangular wave

Find frequency and duty cycle of the waveform.

Ans. next pg

$$T = 40\ \mu s \rightarrow f = \frac{1}{T} = 25\ kHz$$

$$D = \frac{8\ \mu s}{40\ \mu s} = \frac{1}{5} = 0.2$$