# ECE 310L: Microelectronic Circuits Lab

**Lab 6: Switch-Mode Power Supply**

Name:

Lab partner:

## Objectives

(1) Experimentally verify the operation of a buck switch-mode power supply.
(2) Understand the effects of duty cycle and load on the output voltage.

## Background

Switch-mode power supplies (SMPS) use reactive elements (inductors and/or capacitors) and solid-state switches to create output voltages that can be greater than or less than the input voltage. If the output voltage is greater than the input voltage, we refer to the SMPS as a boost converter. If the output voltage is less than the input voltage, we refer to the SMPS as a buck converter. A buck converter is a voltage step down and current step up converter.

In lab 1, we have shown that a simple line regulator circuit (e.g., Zener diode circuit) has the ability of producing an output voltage lower than the input power supply. But such linear regulators waste energy as they operate by dissipating excess power as heat. Buck converter operates at a much higher efficiency (typical 95% or above), and have supplanted linear regulators in many applications. It is useful for tasks such as converting the main voltage in a computer (12 V in a desktop, 12-24 V in a laptop) down to the 0.8-1.8 volts needed by the processor.
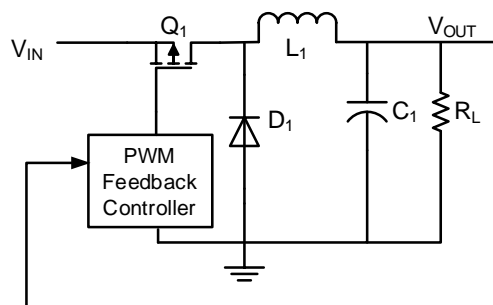


Figure 1. Schematic of a switch-mode power supply

A simplified buck converter is shown in Figure 1. The PMOS FET is operated as a high-side switch at a variable duty cycle. When the FET is on, current flows from the supply through the inductor to the output capacitor and load. During this phase of operation, the inductor develops a voltage drop that opposes (or bucks) the supply, hence the name buck converter. When the FET is then turned off, the inductor acts as a source and delivers current to the output capacitor and load through the diode. The switching frequency is chosen to ensure that the inductor current can only reach a desired peak value. The duty cycle applied to the PMOS transistor is

then varied by a feedback control system to produce a constant output voltage in the presence of changing load current.

The buck converter that you will build in the lab is shown in Figure 2. It will not have a feedback control system and will operate at a constant load. In this lab, you will vary the duty cycle and observe the effect on the output voltage. You will also vary the load with the duty cycle held constant.
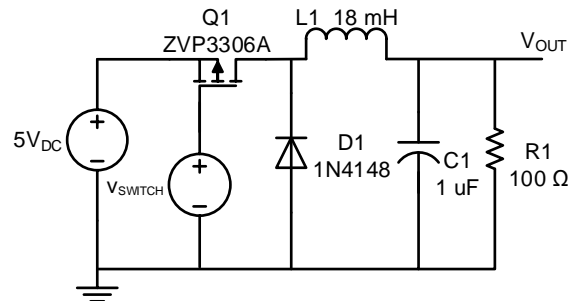


Figure 2. A constant load, open feedback swith-mode power supply

In this lab, we will also learn how to model MOSFET in LTSPICE. LTspice internally includes a small number of NMOS and PMOS transistors. To introduce a new transistor, a sub-circuit is typically needed. A sub-circuit allows you to define a collection of elements as one element (e.g. a MOSFET and an Op-Amp) and to insert this description into the overall circuit. A sub-circuit is defined by a .SUBCKT control statement, followed by the circuit description. Both NMOS and PMOS transistors used in this lab can be found at www.diodes.com. The following is the op codes for ZVP3306A.

```
*ZETEX ZVP3306A Spice Model v1.1 Last Revised 3/5/00
    *
    .SUBCKT ZVP3306A 3 4 5
    *                D G S
    M1 3 2 5 5 P3306M
    RG 4 2 252
    RL 3 5 1.2E8
    C1 2 5 28E-12
    C2 3 2 3E-12
    D1 3 5 P3306D
    *
    .MODEL P3306M PMOS VTO=-2.875 RS=5.227 RD=7.524 IS=1E-15 KP=.145
    +CBD=35E-12 PB=1 LAMBDA=6.67E-3
    .MODEL P3306D D IS=5E-12 RS=.768
    .ENDS ZVP3306A
    *
```

To use these sub-circuits, first pick a PMOS circuit component and place it on workspace. Left click the component while pressing the Ctrl key. A component attribute editor will show up as shown in Fig. 7. Change the Prefix to "X" so that LTspice will look for external SUBCKT control statements. Change the Value to the appropriate SUBCKT name, in this case, ZVP3306A. Please pay attention to the orientation of the PMOS transistors. Since the source terminal is internally tied to the substrate, the drain and source are not interchangeable.
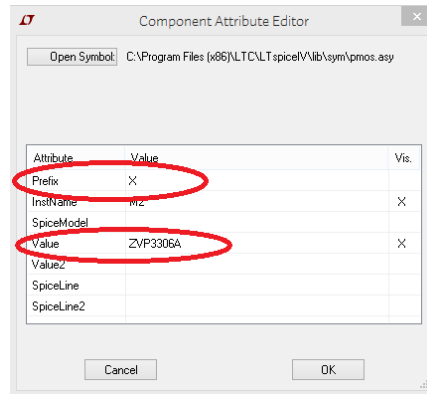
Figure 7. Component attribute editor for LTspice element

## Materials

- DC power supply, HP E3631A
- Oscilloscope, Agilent DSO5014A
- Signal Generator, Agilent 33220A
- DMM, Agilent E3631A
- Solderless breadboad
- Hookup wires
- Resistors: 100Ω (3)
- Capacitor: 1uF tantalum
- Inductor: 18mH
- Diode: 1N4148
- Transistors: ZVP3306A

## Pre-lab Assignment

Question 1: Simulate the circuit in Fig. 2 in LT SPICE for $v_{SWITCH}$ = 0–5V rectangular wave at 25 KHz. Set the $v_{SWITCH}$ symmetry so as to cause the PMOS transistor to operate at duty cycles of 20%, 50%, and 80%. Remember that the PMOS transistor is on when $v_{SWITCH}$ is 0V. Show your waveforms for each simulation run (20%, 50%, and 80%) showing $v_{SWITCH}$, $i_L$, $i_C$, $v_{OUT}$ for just a couple cycles of $v_{SWITCH}$ in <u>steady-state</u>. Note that it will take about 1 millisecond for the circuit to reach steady-state.

By default, an LT SPICE transient simulation will determine a DC operating point for the circuit and then run the transient simulation from that point. So, you will get a very different initial condition depending on whether you set $v_{SWITCH}$ high or low to start. Be sure to select the "Skip initial operating point solution" option on the Transient tab of the Edit Simulation Command dialog.
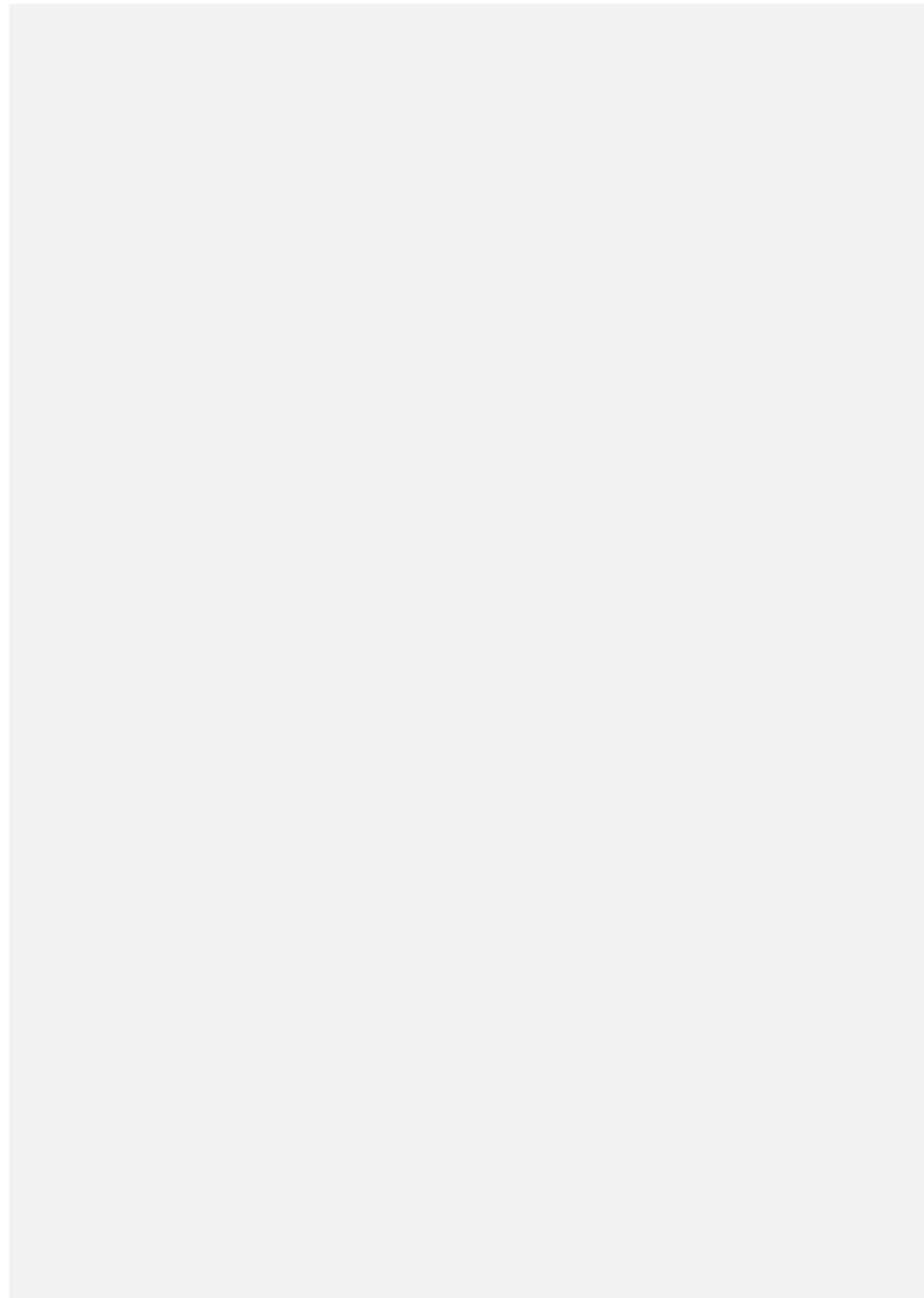
From the LT SPICE results, record the output voltage, $V_{OUT}$, and the peak-to-peak ripple voltage, $V_{RIPPLE}$, when the circuit reaches the steady state.

Table 1. The output voltage and peak-to-peak voltage ripple for
Buck Converter as a function of duty cycle

| Duty Cycle | 20% | 50% | 80% |
|---|---|---|---|
| $V_{OUT}$ (V) | | | |
| $V_{RIPPLE}$ (mV) | | | |

Question 2: On the figure below, draw the complete current path when $v_{SWITCH}$ is at 0 V, assuming the converter is operating in steady-state. Label the current path in red with an arrow indicating the current direction. Explain. Is MOSFET on or off?
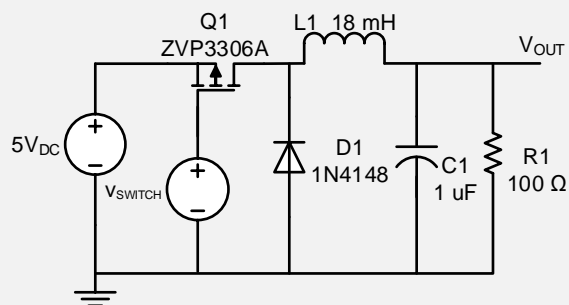


Figure S4. The current path for buck converter for $v_{SWITCH} = 0$
(FET is on). The current path is shown in red with an arrow
indicating the direction.

Question 3: On the figure below, draw the complete current path when $v_{SWITCH}$ is at 5 V, assuming the converter is operating in steady-state. Label the current path in blue with an arrow indicating the current direction. Explain. Is MOSFET on or off?
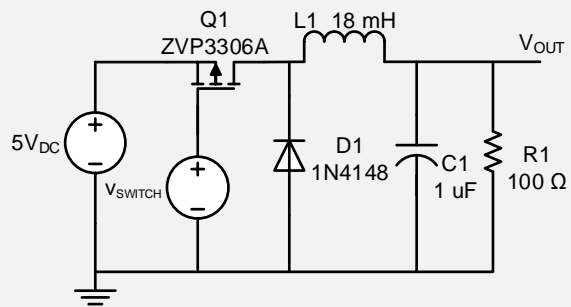
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Figure S5. The current path for buck converter for $v_{SWITCH} = 5$ (FET is off). The current path is shown in blue with an arrow indicating the direction.

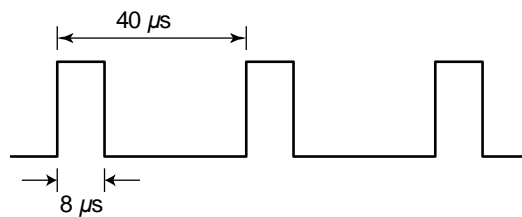Question 4: For the waveform showing in the Fig. 3 below,



Figure 3. Waveform of a rectangular wave

Find frequency and duty cycle of the waveform.

(2)

## Setup

Turn on power to the DMM, oscilloscope, power supply, and signal generator. Set the power supply +6V current limit to 100mA.

Pay careful attention to the transistor ZVP3306A pin-out as shown in Figure 3 to avoid damaging them.
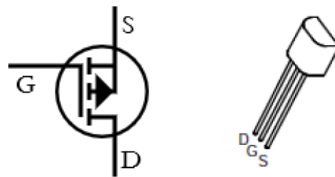


Figure 3. Pin layout of ZVP3306A *p*-channel enhancement mode MOSFET.

Tantalum capacitor is a type of electrolytic capacitor, typically consisting of a pellet of tantalum metal as the anode, covered by a layer of tantalum pentoxide as the dielectric, and surrounded by manganese dioxide as the cathode. The positive polarity of the capacitor is identified by the solder ball on one side of the lead. Sometimes, a "+" sign is also marked on the capacitor.



Figure 4. A tantalum capacitor. The side with solder ball shows the positive polarity of the capacitor.

## Lab Assignment:

1. Use the DMM to measure the values of the resistors. Use the LCR meter to measure the inductance and capacitance. Use the measured component values for the lab assignments.

Table 1: Measured Values for Components in the Buck Converter

| Expected Value | 100 Ω | 1 uF | 18 mH |
|---|---|---|---|
| Measured Value | | | |

2. Construct the circuit shown in Figure 2. Connect the oscilloscope to measure the averaged DC output voltage $v_{OUT}$ and the control signal $v_{SWITCH}$.
3. Set $v_{SWITCH}$ to 0 and verify that $v_{OUT}$ is approximately 5 V. Troubleshoot the circuit if $v_{OUT}$ is more than 0.5 V outside 5 V.
4. Set the signal generator to produce a 0−5 V rectangular wave output at 25 KHz at a 50% duty cycle. Record $v_{OUT}$ in the first column of Table 2. The rest of the columns will be filled out in the later steps.

Table 2: Measured Output for Different Load at 50% Duty Cycle

| Load Resistance, $R_L$ | 100Ω | 100Ω‖100Ω | 100Ω‖100Ω‖100Ω |
|---|---|---|---|
| Output Voltage, $v_{OUT}$ | | | |

5. Set the signal generator duty cycle to produce a switching duty cycle of 20%. Measure the averaged DC output voltage $v_{OUT}$ and the output voltage ripple $v_{RIPPLE}$. Capture the waveforms from oscilloscope in the space below and clearly shows the ripple waveform.

> Voltage ripple is usually very small. To reduce measurement noise, use AC coupling and acquisition averaging (access via Acquisition Mode).

6. Record the values of $v_{OUT}$ and $v_{RIPPLE}$. Repeat for switch duty cycles of 30%, 40%, 50%, 60%, 70%, and 80%. Plot the $v_{OUT}$ and $v_{RIPPLE}$ as a function of duty cycle using MATLAB function **errorbar(X, Y, E)** where **X** is duty cycle, **Y** is output voltage $v_{OUT}$, and **E** is half of voltage ripple $v_{RIPPLE}$.

> Read MATLAB documentation for more information regarding the `errorbar` function.
> Ensure that `Y` and `E` are expressed in the same unit.

7. Compare the observed behavior to the LT SPICE simulations (pre-lab assignment 1). Are there any significant differences? If so, what might account for them?

8. Return the signal generator to a 50% duty cycle. Add a 100Ω resistor in parallel with the load resistor $R_1$. Record the value of $v_{OUT}$ in Table 2.
9. Adjust the duty cycle to restore $v_{OUT}$ to the same value as 50% duty cycle with a single 100Ω resistor. Record the duty cycle value in Table 3.

Table 3:  Measured Duty Cycle for Different Load to Achieve the Same Output Voltage at 50% Duty Cycle with 100Ω Load

| Load Resistance, $R_L$ | 100Ω | 100Ω‖100Ω | 100Ω‖100Ω‖100Ω |
|---|---|---|---|
| Duty Cycle | 50 | | |

10. Record the values of $v_{OUT}$ and $v_{RIPPLE}$ for switch duty cycles of 20%, 30%, 40%, 50%, 60%, 70%, and 80%. Plot the $v_{OUT}$ and $v_{RIPPLE}$ as a function of duty cycle.

11. Return the signal generator to a 50% duty cycle. Add a second 100Ω resistor in parallel with the load. Record the value of $v_{OUT}$ in Table 2.
12. Adjust the duty cycle to restore $v_{OUT}$ to its previous value measured in step 5. Record the duty cycle value in Table 3.

13. From the results obtained in step 4 – 10, discuss what happened when the load was changed.

14. Now remove all load resistors. Describe what happens.

15. As design engineers, we need to do more than design a circuit that operates correctly. We also need to evaluate what could happen if components in our circuit were to fail.

For each of the below failures, indicate what the effects would be both within our circuit and to the circuit being powered.

$Q_1$ fails to a short from drain to source.
$Q_1$ fails to an open from drain to source.
$D_1$ fails to a short from cathode to anode.
$D_1$ fails to an open from cathode to anode.

## Discussion

Problem 1. At 50% duty cycle, what is load regulation for the buck converter circuit? Use the measurement from the three load resistances in Step 5–11 for this calculation.

Problem 2. From the LTSPICE model, determine the power efficiency for the buck converter circuit at 50% duty cycle with a single 100 Ω load.

Problem 3. In the feedback control system, we often need a sawtooth waveform as shown in the Figure 5 below.
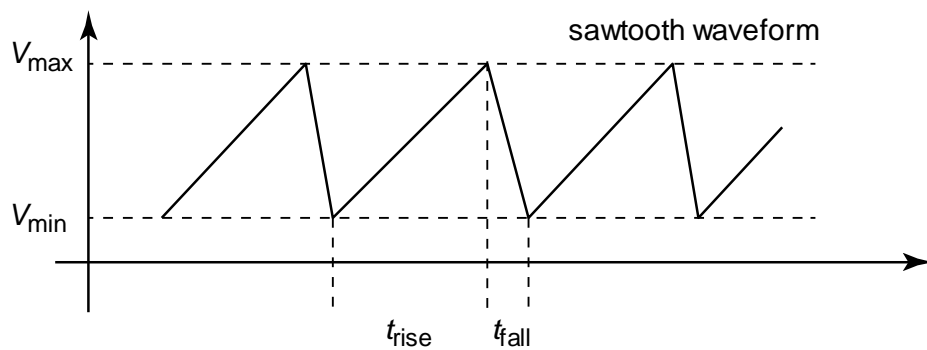


Figure 5. Sawtooth waveform

Assuming that you can have various PMOS FETs, NMOS FETs, diodes, capacitors, and resistors at your disposal, how would you generate an approximation of a sawtooth waveform with a rectangular waveform of a suitable period $T$, duty cycle, $V_{high}$, and $V_{low}$ as show in Fig. 6?
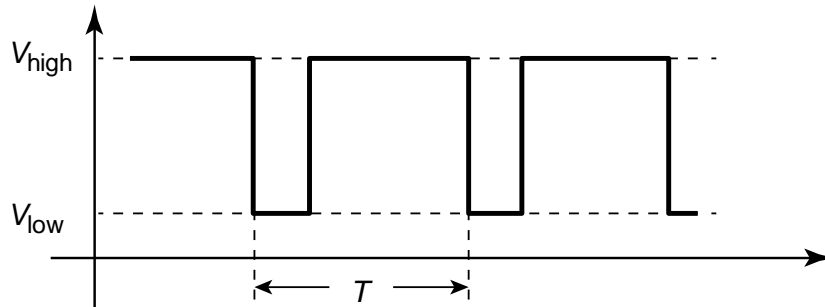


Figure 6. Rectangular waveform

Design a circuit and show in LTSPICE that the output resembles the waveform shown in Figure 5. Please overlay the rectangular waveform with the sawtooth waveform. Hint: When PMOS and NMOS reach saturation, current $I_{DS}$ is nearly constant. The voltage across a capacitor increases linearly when it is charged by a constant current.

If we would like to have a sawtooth waveform with $t_{rise} = 190$ µs, $t_{fall} = 10$ µs, $V_{min} < 0.5$ V, and $V_{max} > 3.6$ V, show your circuit design in LTSPICE.

Please clearly show the values of circuit components, rectangular waveforms, and output waveform.