ECE 310L: Microelectronic Circuits Lab

Lab 8: Source Follower

Name:

Lab partner:

Objectives:

- Construct NMOS source follower for output voltage buffering.
- Construct and verify the operation of an NMOS unity gain amplifier for small signal.

Background:

Some amplifiers are designed to act primarily as buffers, where they isolate circuits by providing high input impedance while providing a voltage gain of nearly one, or unity gain. As a result, it is also known as a *voltage follower* because the output voltage follows or tracks the input voltage. With a basic single-stage MOSFET topologies, voltage follower can be achieved by a *common-drain amplifier*, also known as a *source follower*. In this circuit, the gate terminal of the transistor serves as the input as shown in Figure 1. The source is the output, and the drain is common to both (input and output), hence the name of common-drain amplifier.
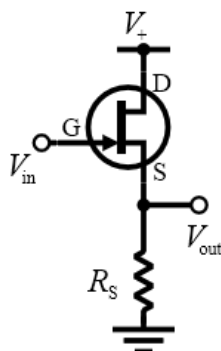

Figure 1. Source follower circuit with JFET

In this lab, we will demonstrate two applications of source follower: (1) as a voltage buffer for switched mode power supply and (2) as a power amplifier for small signal.

Buffered Buck Converter

In Lab 6: Switch-Mode Power Supply, we demonstrated that buck converter has the ability to convert the main voltage to any voltage lower than the main voltage at a much higher efficiency (typical 95% or above) than a linear regulator. For example, in a computer (12 V in a desktop, 12-24 V in a laptop) down to the 0.8-1.8 volts needed by the CPUs. However, the output of the circuit in Lab 6 shows a strong dependency on load resistance which is called poor load regulation. In the following pre-lab question 1, you will be asked to model a buck converter and calculate the load regulation of the circuit. You will observe that the circuit has a load regulation higher than 20%.

In practice, 20% load regulation is hardly acceptable. We would like the power supply to provide a constant voltage regardless of the load. A typical power supply has a load regulation of 5% or

better. To improve load regulation, a voltage buffer amplifier can be used to transfer a voltage from the buck converter, having a high output impedance level, to a second circuit with a low input impedance level. The buffer amplifier prevents the second circuit from loading the first circuit unacceptably and interfering with its desired operation.

Figure 2 shows a source follower formed with a simple MOS current source using M_2. The current source offers high resistance when operated in the saturation region. The voltage applied at gate of M_2 that is V_B makes sure that M_2 operates in saturation all the time. The amount of DC voltage level shift between output V_{out} and input V_{in} is affected by V_B. In pre-lab question 2, we will form a simple buffered buck converter by connecting the output of a buck converter in series with the source follower. You will be asked to calculate the load regulation again and find out how much it is improved with buffer amplifier.
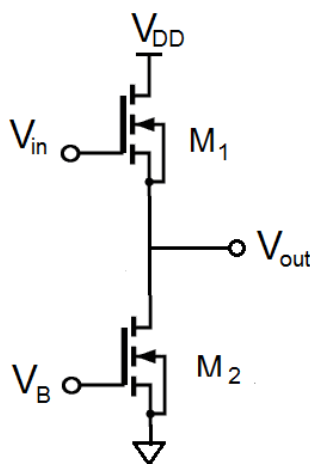

Figure 2. Constant current buffer amplifier

It's important to note that the circuit in Figure 2 would not be used in the real world since the current is dependent upon the gain and threshold voltage of M_2 which varies greatly between transistors and with temperature. To minimize those effects, a resistor is typically added in series with the source of M_2 to ground to add some negative feedback. However, we will not explore this option in this lab.

Small-Signal Unity Gain Amplifier

Another application of source follower is to isolate sensors from readout electronics, for example, to separate a thermocouple or thermistor from an ADC. They can be used for driving ADCs as ADCs can draw current in large bursts when they sample their input, and this can be disruptive to whatever circuitry might be sourcing the signal.

Also imagine a microcontroller can supply 1 mA but you need at least 10 or 20 mA to drive something (e.g. LED, relay, etc). Most voltage followers can supply more current than microcontroller I/O pins. Although the voltage gain of a voltage buffer amplifier may be (approximately) unity, it usually provides considerable current gain and thus power gain.

The common-drain NMOS amplifier shown in Figure 3 is one such amplifier for small signal. The resistive network R_1–R_3 is designed to place the MOSFET at an optimal working point. In prelab question 4, you will be asked to find out what if MOSFET is not biased optimally. The name source follower indicates the output is taken from the source and is in phase with input, i.e. V_S

"follows" V_G. The term common drain comes from the idea that the drain is connected directly to V_{DD} with no load resistance and in the AC analysis the supply rail, V_{DD}, is a ground reference. The voltage gain (A_V) of the source follower is inherently less than one and is generally in the range 0.8 – 0.9. The current gain can be much higher than one, though, allowing the source follower to buffer between a high-impedance source and a low-impedance load.
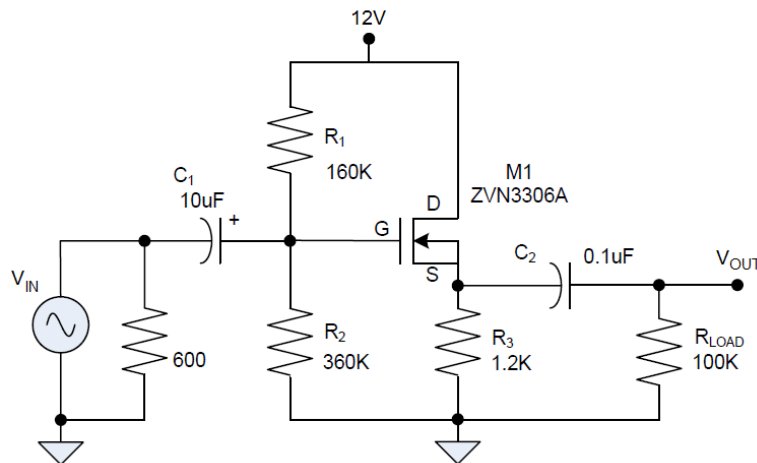

Figure 3. N-channel MOSFET source follower circuit

The input coupling capacitors are very large, so their poles will be near 0. The low frequency response of the system will thus be determined by C_2. The RC time constant will set the cut-off frequency so in this design the significant time constant will be C_2 and the equivalent resistance seen by C_2.

In the NMOS amplifier the time constant will be determined by the output capacitor, C_2, which is in series with the load resistor and the parallel combination of the source resistor and the impedance seen in the NMOS source, $1/g_m$.

$$g_m = \frac{2I_D}{V_{GS} - V_{TN}}$$

$$\tau = \left(\left(1.2k \parallel \frac{1}{g_m}\right) + 100k\right)100nF$$

Pre-Lab Assignment:

Question 1: Simulate the circuit in Figure 4 in LTSPICE for V_{SWITCH} = 0–12V rectangular wave at 25 KHz. Find the duty so that V_{OUT} is 6V (within ±2%).
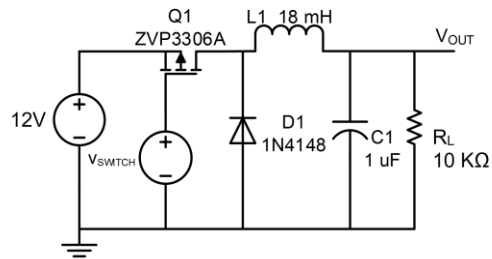

Figure 4. An open feedback swith-mode power supply

In the textbox below, show the LTSPICE circuit model and the output waveform <u>after</u> V_{OUT} reaches steady state.

Keep the duty cycle and change the load resistance R_L to 6 KΩ and 2 KΩ, find out the output voltage V_{OUT} and ripple voltage. Calculate load regulation of the circuit and fill in the table below.

Table 1: Buck Converter Circuit

Load resistance, R_L	Calculated values			
	Duty Cycle	Output Voltage (V)	Ripple Voltage (mV)	Load Regulation (%)
10 KΩ				
6 KΩ				
2 KΩ				

Question 2: A simple buffered buck converter is shown in Figure 5. Simulate the circuit in LTSPICE for V_{SWITCH} = 0–12V rectangular wave at 25 KHz. Find the duty so that V_{OUT} is 6V (within ±2%).
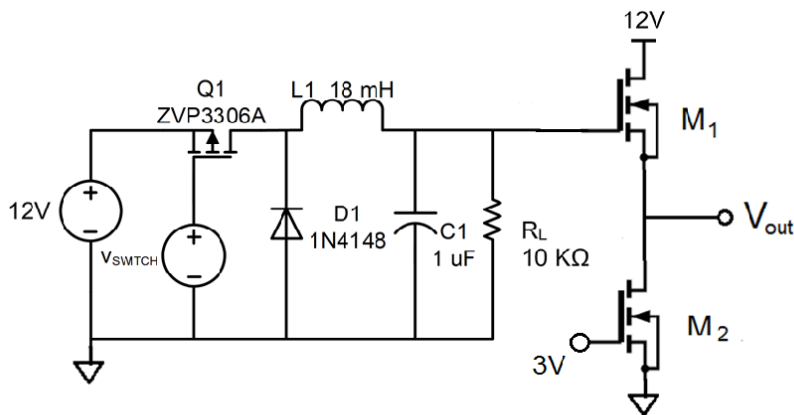

Figure 5. Buffered buck converter

In the textbox below, show the LTSPICE circuit model and the output waveform <u>after</u> V_{OUT} reaches steady state.
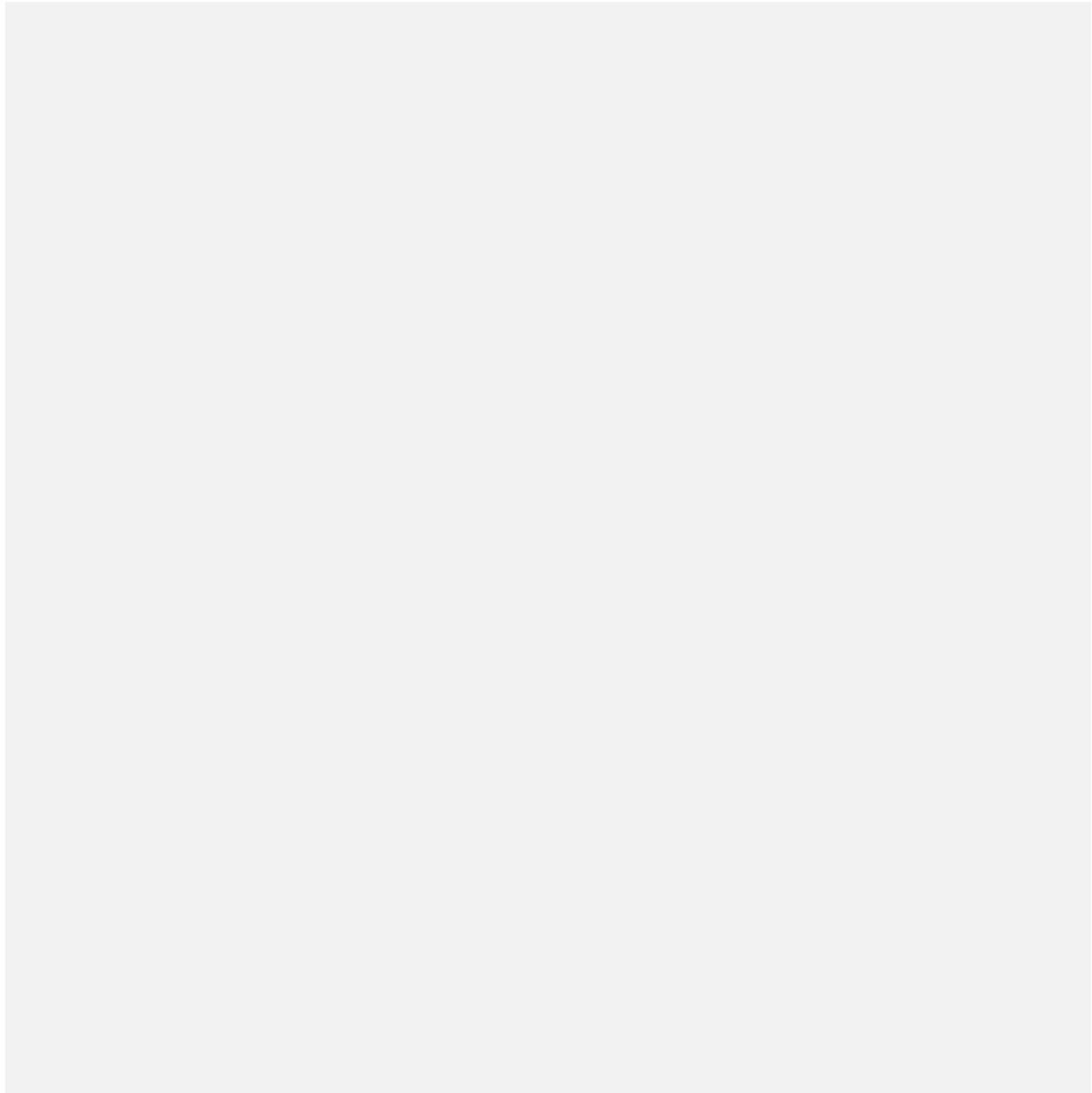
Table 2: Buffered Buck Converter Circuit

Load resistance	Calculated values			
	Duty Cycle	Output Voltage (V)	Ripple Voltage (mV)	Load Regulation (%)
10 KΩ				
6 KΩ				
2 KΩ				

Question 3: Use LTSPICE to calculate the frequency response of the circuit shown in Figure 3 in the frequency range of 10 Hz to 100 KHz. Use the SPICE model of ZVN3306A and V_{IN} = 1 V

in LTSPICE. Show both amplitude and phase in the Bode plot. Determine the frequency of 3 dB point.
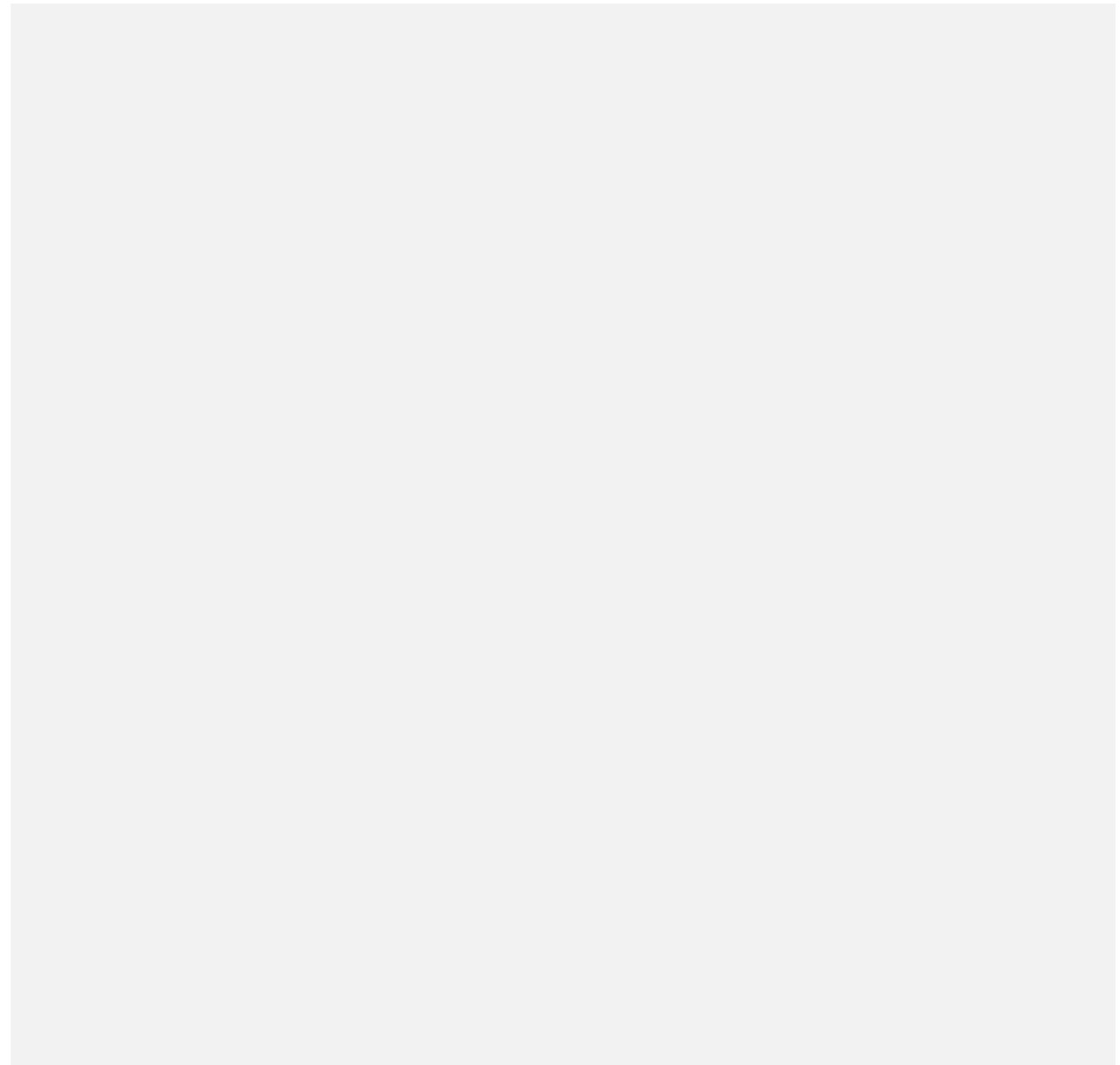
Question 4: In addition to frequency response, another important design consideration for an amplifier is clipping. Clipping is a form of waveform distortion that occurs when the amplifying circuit is overdriven and attempts to deliver an output voltage beyond its maximum capability. For an audio amplifier, clipping leads to sound distortion and should be avoided in most cases.

Many factors can contribute to clipping such as power drawn exceeding supply capability, poorly designed bias point for the transistors, and current saturation. In this lab, we will examine how bias point affects the clipping of an amplifier. The NMOS source follower circuit shown in Figure 3 is modeled with LTSPICE in transient mode, as shown in Figure 6. The source V_{IN} is a sinusoidal wave with a frequency of 1 KHz and an amplitude of 12 Vp-p.
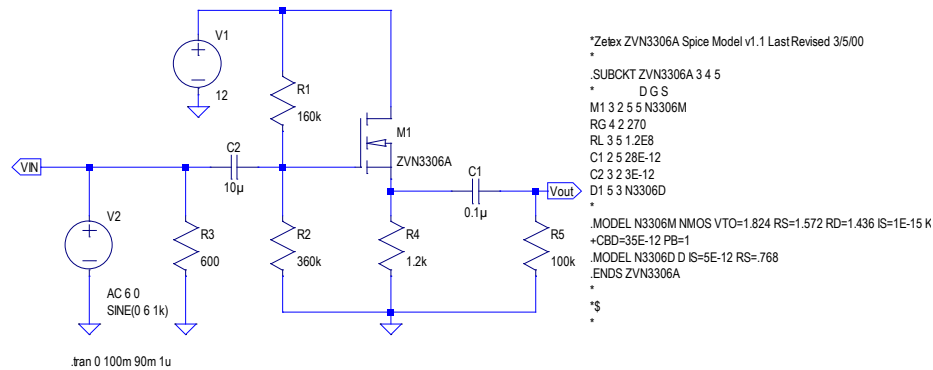
Figure 6. LTSpice transient model of a NMOS source follower

Figure 7 shows the output voltage V_{OUT} as a function of time as well as V_{IN}. The transient calculation is performed for 100 ms (100 periods to ensure that the circuit reaches a steady state) but only the last 10 ms is shown in the figure. It is clear that the V_{OUT} is slightly clipped at the peak (near +6 V). With a power supply voltage of 12 V, this clipping is expected. The peak-to-peak voltage is, at the minimum, limited to the power supply voltage less a small amount due to the saturation voltage ($R_{DS(on)}$ for FET or $V_{CE}(sat)$ for BJT).
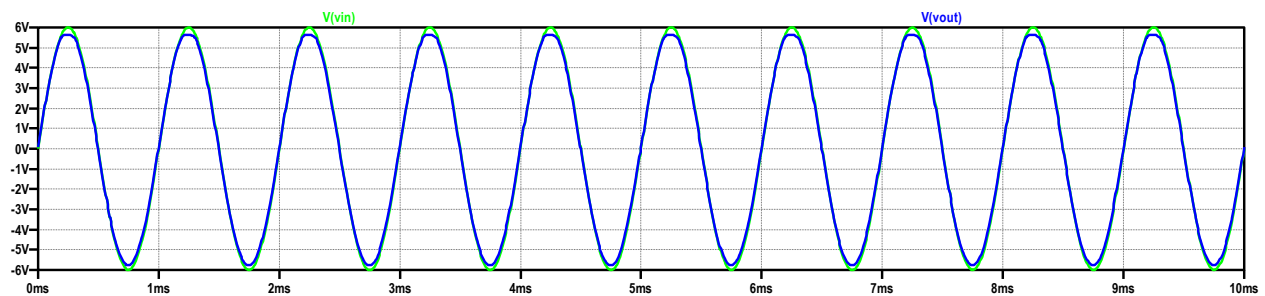

Figure 7. The input and output waveforms of NMOS source follower.
A small voltage clipping can be observed for the output.

The voltage clipping can also be analyzed in the frequency domain. In LTSPICE, right click on Fig. 7 and choose FFT. Clipping produces harmonics at higher frequencies than the unclipped signal, as shown in Fig. 8 These high frequency energy can be very harmful as they has the potential to damage a loudspeaker's tweeter via overheating.
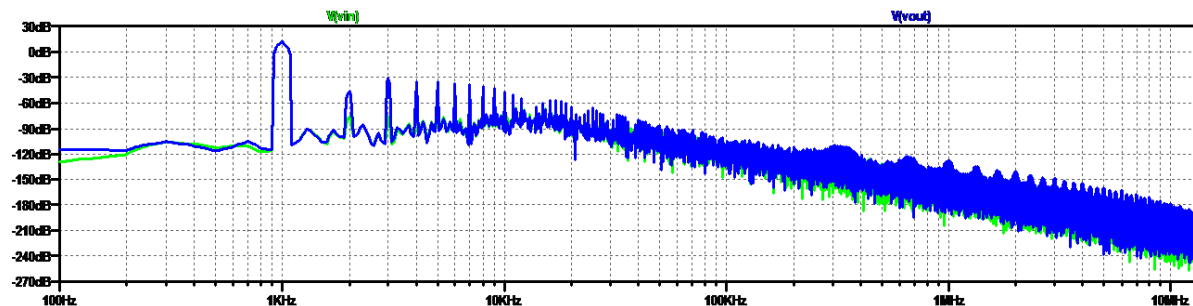

Figure 8. The FFT spectra of the input and output waveform. It is clear that the output produces higher harmonics components (at 2 KHz, 3 KHz, etc.) than the input voltage.

The peak-to-peak output can be further reduced if the output stage does not have a quiescent DC output voltage set to half the supply voltage. For the amplifier circuit shown in Figure 3, the Q-point for V_{DS} shall be around 6 V to achieve the maximal unclipped peak-to-peak output.

If R_2 is replaced by a 100 KΩ, show the V_{OUT} as a function of time for V_{IN} = 12 Vp-p. What is the maximal peak-to-peak output without clipping?