ECE 310L: Microelectronic Circuits Lab

Lab 5: *I−V* Relation of MOSFET

Name:

Lab partner:

Objectives

Experimentally verify the operations of NMOS and PMOS transistor in the cut-off, triode, and saturation regions.

Materials

- DC Power supply, HP E3631A
- Oscilloscope, Agilent DSO5014A
- Signal generator, Agilent 33220A
- DMM, Agilent E3631A
- Solderless breadboad
- Hookup Wire
- Resistors: 10 Ω
- Transistors: ZVN3306A, ZVP3306A

Background

A field effect transistor (FET) is a voltage controlled device where its current carrying ability is changed by applying an electronic field. A commonly used type of FET is the metal-oxide semiconductor FET (MOSFET). MOSFET are widely used in integrated circuits. MOSFET work by inducing a conducting channel between two contacts called the source (S) and the drain (D) by applying a voltage on the oxide-insulated gate electrode (G). There are two main types of MOSFET called NMOS and PMOS depending on the type of carriers flowing through the channel. Figure 1 shows the circuit symbols for different types of MOSFETs.

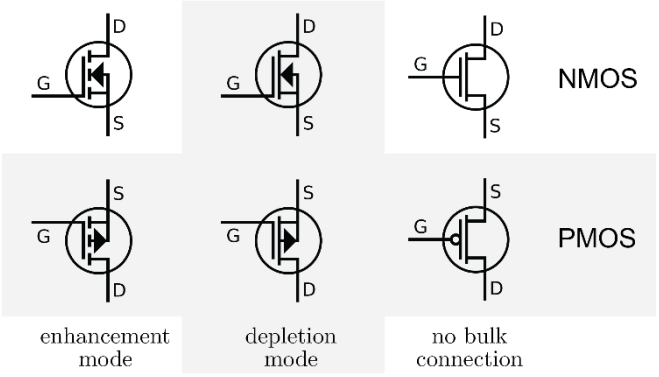

Figure 1. Comparison of MOSFET symbols for enhancement-mode, depletion-mode, and no bulk connection transistors

A NMOS transistor is made up of n-type source and drain and a p-type substrate. When a positive voltage is applied to the gate that is higher than the threshold V_{TN} ($V_{GS} > V_{TN}$), holes in

the body (p-type substrate) are driven away from the gate. This allows forming an n-type channel between the source and the drain and a current is carried by electrons from source to the drain through an induced n-type channel. Logic gates and other digital devices implemented using NMOSs are said to have NMOS logic. There are three modes of operation in a NMOS called the cut-off, triode and saturation, as shown in Fig. 2. Pay attention to the direction of current I_{DS} and voltage V_{GS} in the figure. NMOS logic is easy to design and manufacture. But circuits with NMOS logic gates dissipate static power when the circuit is idling, since DC current flows through the logic gate when the output is low.

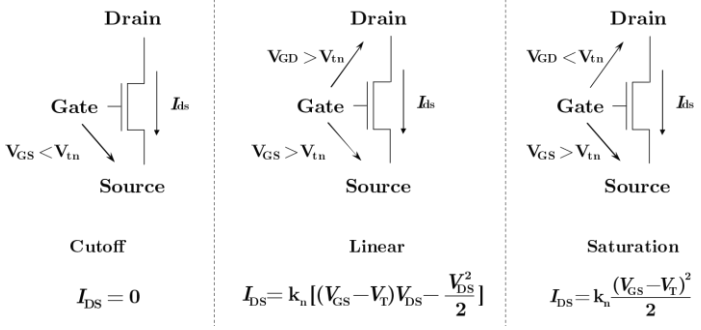

Figure 2. Operation modes – cutoff, linear (triode), and saturation of NMOS

A PMOS transistor is made up of p-type source and drain and an n-type substrate. When a negative voltage is applied between the gate and source that is lower than the threshold V_{TP} ($V_{GS} < V_{TP}$), a p-type channel is formed between the source and the drain with opposite polarities. A current is carried by holes from source to the drain through an induced p-type channel. A high voltage on the gate will cause a PMOS not to conduct, while a low voltage on the gate will cause it to conduct. Logic gates and other digital devices implemented using PMOS are said have PMOS logic. There are three modes of operation in a PMOS called the cut-off, triode and saturation, as shown in Fig. 3. Pay attention to the direction of current I_{DS} and voltage V_{GS} in the figure. PMOS technology is low cost and has a good noise immunity.

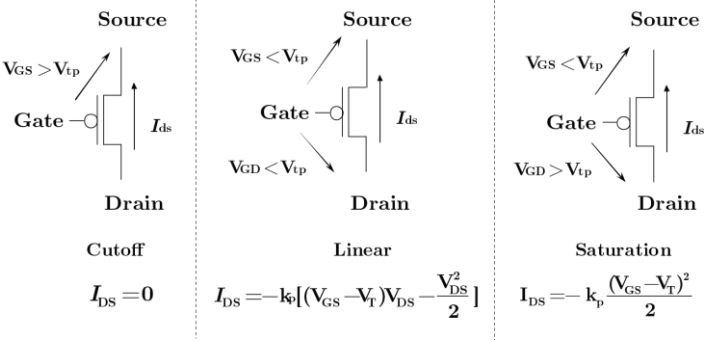

Figure 3. Operation modes – cutoff, linear (triode), and saturation of PMOS

The main difference between NMOS and PMOS is the type of carrier conducting current. In a NMOS, carriers are electrons, while in a PMOS, carriers are holes. NMOS is built with n-type source and drain and a p-type substrate, while PMOS is built with p-type source and drain and a

n-type substrate. When a high voltage is applied to the gate, NMOS will conduct, while PMOS will not. Furthermore, when a low voltage is applied in the gate, NMOS will not conduct and PMOS will conduct. NMOS are considered to be faster than PMOS, since the carriers in NMOS, which are electrons, travel about twice as fast as holes, which are the carriers in PMOS. But PMOS devices are more immune to noise than NMOS devices. Given the same functionalities, NMOS ICs is generally smaller than PMOS ICs, since the NMOS has one-half of the impedance provided by a PMOS for the same geometry and operating conditions.

In addition to the distinction of carriers, FETs is distinguished by two major operating modes – depletion mode and enhancement mode, corresponding to whether the transistor is in an ON state or an OFF state at zero gate–source voltage. In a depletion-mode MOSFET, the device is normally ON at zero V_{GS}. Such devices are used as load “resistors” in logic circuits. For N-type depletion-load devices, the threshold voltage might be about −3 V, so it could be turned off by pulling the gate 3 V negative. Enhancement-mode MOSFETs are commonly used as a switching elements. These devices are OFF at zero V_{GS}, and can be turned on by pulling the gate voltage in the direction of the drain voltage; that is, toward the V_{DD} supply rail, which is positive for NMOS logic and negative for PMOS logic.

In this lab, we experimentally characterize NMOS and PMOS transistors operating in three distinct regions – cut-off, triode (linear), and saturation (pinch-off). In cut-off, the FET is essentially non-conducting and no drain current will flow. In the triode region, the FET acts as a nearly constant resistance (R_{DS}) whose value is controlled by V_{GS}. In saturation, I_D remains nearly constant as V_D varies.

Pre-Lab Assignments

Question 1. Review the datasheets for the NMOS ZVN3306A and PMOS ZVP3306A transistors. Bring the datasheet with you during the lab period to verify your measurements.

Question 2. The *I–V* characteristic of an NMOS transistor can be measured with the circuit shown in Fig. 4. The V_{GS} source will be provided by the 6V DC power supply, while the V_{DD} source will be provided by the signal generator. R_1 is a current sensing resistor. The peak amplitude of V_{DD} and the voltage across R_1 yield *I–V* characteristic of Q_1 for the given V_{GS}. A family of *I–V* curves can be obtained by V_{GS}.

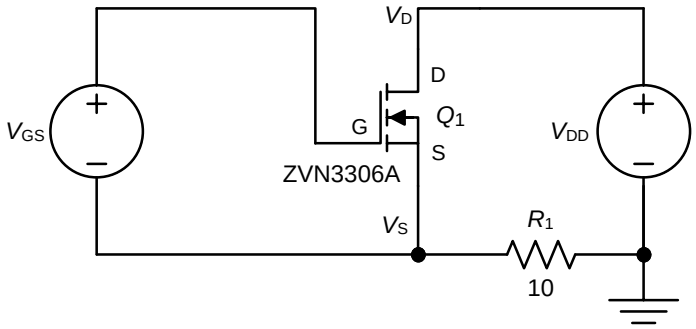

Figure 4. Circuit for measuring the *I–V* characteristic of a NMOS transistor.

In the space below, show the circuit for measuring the *I–V* characteristic of an enhancement-mode PMOS transistor. Explain.

Question 3. The output characteristic of a MOSFET are shown in Fig. 5.

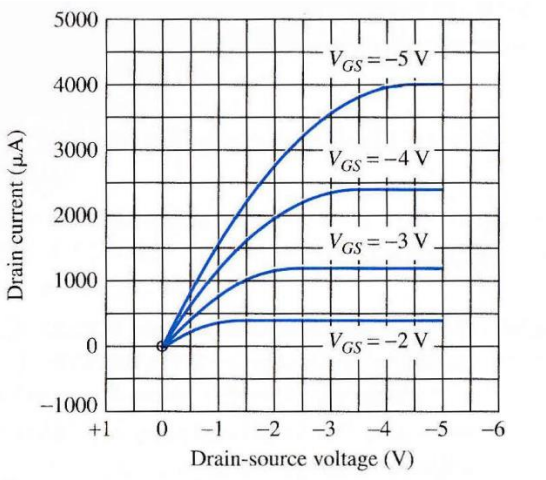

Figure 5. Family of *I*−*V* curves for a MOSFET.

Answer the following questions regarding the transistor.

(1) Is this a PMOS or a NMOS transistor?
(2) Is this an enhancement-mode or depletion-mode transistor?
(3) What are the values of k and V_T for this transistor?

Setup

Turn on power to the DMM, oscilloscope, power supply, and signal generator. Set the power supply +6 V output's current limit to 50 mA.

You will be constructing two circuits. Pay careful attention to the pin-out of the transistors to avoid damaging them. The NMOS and PMOS parts have the same pin out, as shown in Figure 6.

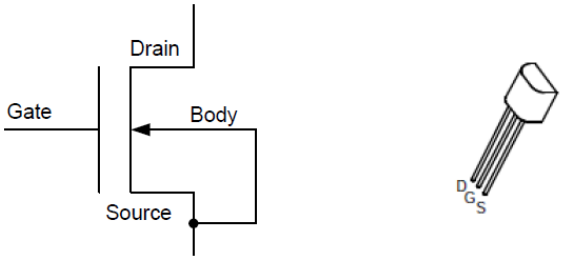

Figure 6. Pin layout of NMOS ZVN3306A and PMOS ZVP3306A transistors.

The first circuit will be built to evaluate the behavior of an NMOS transistor, as shown in Fig. 4. The V_{GS} source will be provided by the 6V DC power supply, while the V_{DD} source will be provided by the signal generator.

You will measure V_D and V_S during this experiment. From these measurements you will be able to calculate the drain current I_{DS} (V_S/R_1) and V_{DS} ($V_D - V_S$). Note that you cannot count on the signal generator's displayed output voltage to be equal to V_{DS}.

A similar circuit will be used for the PMOS transistor as described by the solution of pre-lab question 2.

In order to obtain the waveforms and raw data from the oscilloscope, a USB thumb drive smaller than 16 GB and formatted in FAT32 is needed. USB thumb drive is not provided.

Lab Assignment:

1. Use the DMM to measure the value of the 10 Ω resistor. Use the measured resistor value in your calculations.

> **Keep your hookup wires as short as possible between components to minimize oscillations in output.**

2. Construct the circuit shown in Fig. 4. Connect the oscilloscope to measure V_D and V_S. Use the SYNC output of the signal generator to provide a stable trigger source to the oscilloscope. Connect the SYNC output to TRIG IN port at the back of the oscilloscope. In the textbox below, draw how oscilloscope probes are connected to the circuit.

3. Set the signal generator to produce a rectangular pulse at 100 Hz with a pulse-width of 1ms and pulse amplitude 0−10 V. Set the pulse rise/fall times (edges) to 100 ns. Set the V_{GS} source to 0 V.
4. Slowly increase the V_{GS} source until you see current begin to flow (V_S will go positive). Record the value, and compare to the threshold voltage (V_{TN}) given in the datasheet.

> **Measurements made at low gate bias is very noisy. That is expected.**

In Table 1 depicts the specified manufacturer $V_{GS(th)}$ limits and observed $V_{GS(th)}$s for the ZVN3306A NMOS and ZVP3306A PMOS.

Table 1: Specified manufacturer $V_{GS(th)}$ limits and observed $V_{GS(th)}$s for the ZVN3306A NMOS and ZVP3306A PMOS.

MOSFET	Manufacturer Specified $V_{GS(th)}$ maximum (V)	Manufacturer Specified $V_{GS(th)}$ minimum (V)	Observed $V_{GS(th)}$ (V)
ZVN3306A ZVP3306A			

5. Increase the V_{GS} by 0.5 V (i.e. set it to V_{TN} + 0.5 V). Then, slowly reduce the V_{DD} source amplitude (keeping its lower level at 0 V), recording the peak values of V_D and V_S. The signal generator produces a rectangular pulse at a relatively low duty cycle to minimize heating of the transistor. This technique is commonly used to characterize devices at higher current and/or power levels than they can sustain in steady-state. Record enough data points so that you will be able to reconstruct an accurate curve – you will find that as V_{DD} is reduced you will need to do so in smaller increments (as you go from the saturation region to the triode region). You will want to create a data table or put this information directly into a spreadsheet.

Set the V_{GS} source to V_{TN} + 1.0V, and repeat step 5. Repeat for V_{TN} + 1.5, and V_{TN} + 2.0V. Plot the I_{DS}-V_{DS} relation of ZVN3306A for a family of V_{GS} starting at V_{TN} + 1.0V.

Before proceeding, carefully read step 6.

6. The family of *I*−*V* curves of a MOSFET device can also be measured directly with oscilloscope by using a scanning voltage approach introduced in Lab 3. Change the signal generator to produce a sawtooth pulse at 100 Hz with a peak amplitude of 10 V. Connect V_D to channel 1 and V_S to channel 2. Change oscilloscope to X-Y mode and the display on the oscilloscope is the *I*−*V* curve for the given V_{GS}. Increase V_{GS} at 0.5 V interval to finish all *I*−*V* curves.

   > **The waveform shown in the X-Y mode are not always properly saved in when the oscilloscope is in the X-Y mode. To avoid potential data corruption issues, change the oscilloscope back to sampling mode before exporting data to the thumb drive. Data points for channel 1 and 2 are for X and Y axes, respectively.**

7. Compare the results for step 5 and 6 on a single graph. Remember to convert the voltage on the sense resistor to I_{DS}. Annotate your graph to show the apparent pinch-off locus, and label the cut-off, triode, and saturation regions.

Replace the transistor with the ZVP3306A, a PMOS transistor. Use the circuit that you answered in prelab Question 2 and follow the similar steps 3−8 to measure I_{DS}-V_{DS} relation of ZVP3306A. You can use either approach to perform the measurement.

> **Threshold voltage varies between NMOS and PMOS transistors. The measured saturation current could therefore be smaller and larger than the results from SPICE models.**

8. In the textbox below, draw how oscilloscope probes are connected to the circuit.

9. Plot the I_{DS}-V_{DS} relation of ZVP3306A for a family of V_{GS} measured in Step 8. Annotate your graph to show the apparent pinch-off locus, and label the cut-off, triode, and saturation regions.

Discussion

Question 1. How do your graphs compare to the manufacturer's data?

Question 2. Within the triode region, is $R_{DS(on)}$ relatively constant? Support your answer with calculations based on your data.

Question 3. How do the I_{DS}–V_{DS} curves for the saturation region of the NMOS transistor compare to those of the PMOS transistor? Compare the curves at similar values for (V_{GS} - $V_{TN}$and |V_{GS} - V_{TP}|.

Question 4. Estimate a value for the channel-length modulation parameter λ based on your data.

References

[1] “N-Channel Enhancement Mode Vertical DMOS FET ZVN3306A” pp. 1-3., March 94
Available: http://pdf.datasheetcatalog.com/datasheet/zetexsemiconductors/zvn3306a.pdf

[2] “P-Channel Enhancement Mode Vertical DMOS FET ZVP3306A” pp. 1-3., March 94
Available: http://pdf.datasheetcatalog.com/datasheet/zetexsemiconductors/zvp3306a.pdf