ECE 310L: Microelectronic Circuits Lab

Lab 5: *I–V* Relation of MOSFET

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Group 13

Objectives

Experimentally verify the operations of NMOS and PMOS transistor in the cut-off, triode, and saturation regions.

Materials

- DC Power supply, HP E3631A
- Oscilloscope, Agilent DSO5014A
- Signal generator, Agilent 33220A
- DMM, Agilent E3631A
- Solderless breadboad
- Hookup Wire
- Resistors: 10 Ω
- Transistors: ZVN3306A, ZVP3306A

Background

A field effect transistor (FET) is a voltage controlled device where its current carrying ability is changed by applying an electronic field. A commonly used type of FET is the metal-oxide semiconductor FET (MOSFET). MOSFET are widely used in integrated circuits. MOSFET work by inducing a conducting channel between two contacts called the source (S) and the drain (D) by applying a voltage on the oxide-insulated gate electrode (G). There are two main types of MOSFET called NMOS and PMOS depending on the type of carriers flowing through the channel. Figure 1 shows the circuit symbols for different types of MOSFETs.

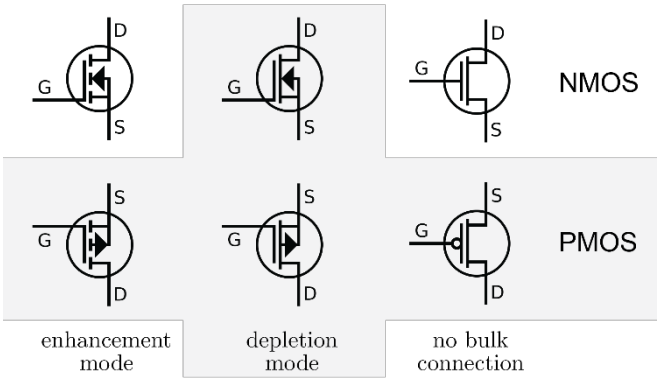


Figure 1. Comparison of MOSFET symbols for enhancement-mode, depletion-mode, and no bulk connection transistors

A NMOS transistor is made up of n-type source and drain and a p-type substrate. When a positive voltage is applied to the gate that is higher than the threshold V_{TN} ($V_{GS} > V_{TN}$), holes in

the body (p-type substrate) are driven away from the gate. This allows forming an n-type channel between the source and the drain and a current is carried by electrons from source to the drain through an induced n-type channel. Logic gates and other digital devices implemented using NMOSs are said to have NMOS logic. There are three modes of operation in a NMOS called the cut-off, triode and saturation, as shown in Fig. 2. Pay attention to the direction of current I_{DS} and voltage V_{GS} in the figure. NMOS logic is easy to design and manufacture. But circuits with NMOS logic gates dissipate static power when the circuit is idling, since DC current flows through the logic gate when the output is low.

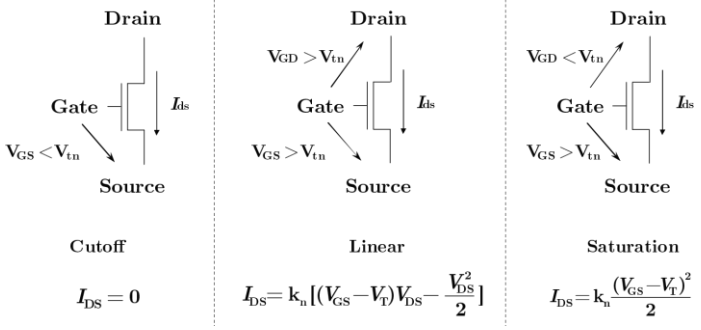


Figure 2. Operation modes – cutoff, linear (triode), and saturation of NMOS

A PMOS transistor is made up of p-type source and drain and an n-type substrate. When a negative voltage is applied between the gate and source that is lower than the threshold V_{TP} ($V_{GS} < V_{TP}$), a p-type channel is formed between the source and the drain with opposite polarities. A current is carried by holes from source to the drain through an induced p-type channel. A high voltage on the gate will cause a PMOS not to conduct, while a low voltage on the gate will cause it to conduct. Logic gates and other digital devices implemented using PMOS are said have PMOS logic. There are three modes of operation in a PMOS called the cut-off, triode and saturation, as shown in Fig. 3. Pay attention to the direction of current I_{DS} and voltage V_{GS} in the figure. PMOS technology is low cost and has a good noise immunity.

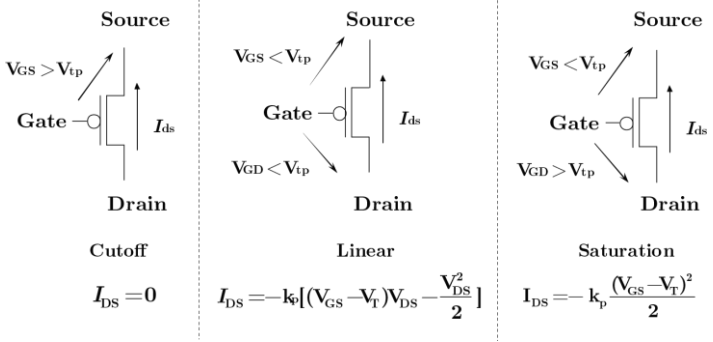


Figure 3. Operation modes – cutoff, linear (triode), and saturation of PMOS

The main difference between NMOS and PMOS is the type of carrier conducting current. In a NMOS, carriers are electrons, while in a PMOS, carriers are holes. NMOS is built with n-type source and drain and a p-type substrate, while PMOS is built with p-type source and drain and a

n-type substrate. When a high voltage is applied to the gate, NMOS will conduct, while PMOS will not. Furthermore, when a low voltage is applied in the gate, NMOS will not conduct and PMOS will conduct. NMOS are considered to be faster than PMOS, since the carriers in NMOS, which are electrons, travel about twice as fast as holes, which are the carriers in PMOS. But PMOS devices are more immune to noise than NMOS devices. Given the same functionalities, NMOS ICs is generally smaller than PMOS ICs, since the NMOS has one-half of the impedance provided by a PMOS for the same geometry and operating conditions.

In addition to the distinction of carriers, FETs is distinguished by two major operating modes – depletion mode and enhancement mode, corresponding to whether the transistor is in an ON state or an OFF state at zero gate–source voltage. In a depletion-mode MOSFET, the device is normally ON at zero V_{GS}. Such devices are used as load “resistors” in logic circuits. For N-type depletion-load devices, the threshold voltage might be about −3 V, so it could be turned off by pulling the gate 3 V negative. Enhancement-mode MOSFETs are commonly used as a switching elements. These devices are OFF at zero V_{GS}, and can be turned on by pulling the gate voltage in the direction of the drain voltage; that is, toward the V_{DD} supply rail, which is positive for NMOS logic and negative for PMOS logic.

In this lab, we experimentally characterize NMOS and PMOS transistors operating in three distinct regions – cut-off, triode (linear), and saturation (pinch-off). In cut-off, the FET is essentially non-conducting and no drain current will flow. In the triode region, the FET acts as a nearly constant resistance (R_{DS}) whose value is controlled by V_{GS}. In saturation, I_D remains nearly constant as V_D varies.

Pre-Lab Assignments

Question 1. Review the datasheets for the NMOS ZVN3306A and PMOS ZVP3306A transistors. Bring the datasheet with you during the lab period to verify your measurements.

Question 2. The *I–V* characteristic of an NMOS transistor can be measured with the circuit shown in Fig. 4. The V_{GS} source will be provided by the 6V DC power supply, while the V_{DD} source will be provided by the signal generator. R_1 is a current sensing resistor. The peak amplitude of V_{DD} and the voltage across R_1 yield *I–V* characteristic of Q_1 for the given V_{GS}. A family of *I–V* curves can be obtained by V_{GS}.

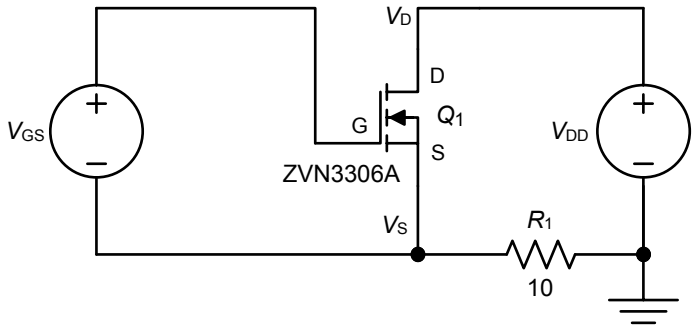
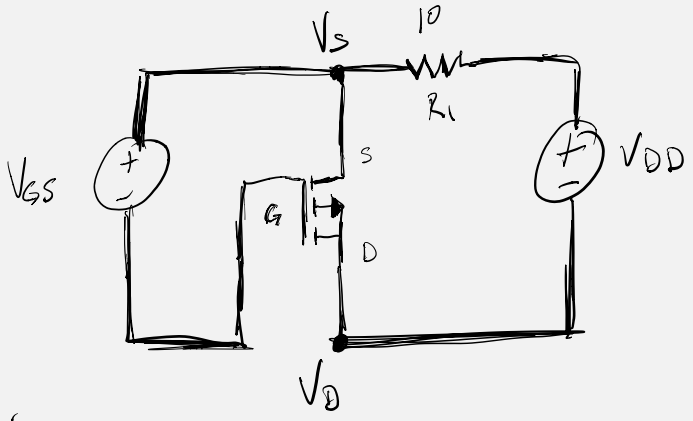


Figure 4. Circuit for measuring the *I–V* characteristic of a NMOS transistor.

In the space below, show the circuit for measuring the *I–V* characteristic of an enhancement-mode PMOS transistor. Explain.



inverted

from above → PMOS has inverted polarity

Question 3. The output characteristic of a MOSFET are shown in Fig. 5.

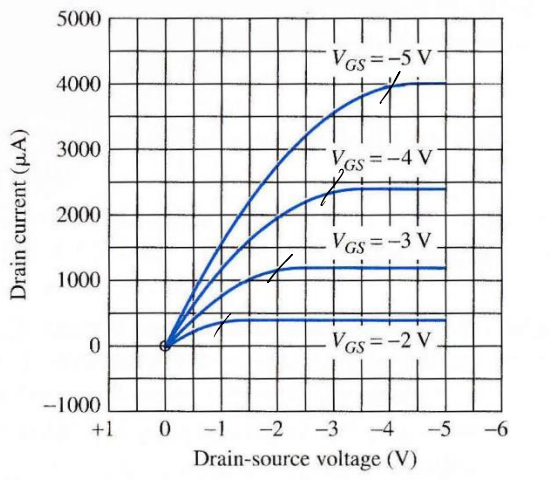


Figure 5. Family of *I*−*V* curves for a MOSFET.

Answer the following questions regarding the transistor.

(1) Is this a PMOS or a NMOS transistor?
(2) Is this an enhancement-mode or depletion-mode transistor?
(3) What are the values of k and V_T for this transistor?

1) PMOS

2) depletion Mode

3) V_{T_2} - 1V → k - 0.4mA/V²

V_{T_3} - 2V → k - 0.55mA/V²

V_{T_4} - 3V → k - 0.8mA/V²

V_{T_5} - 4V → k - 1mA/V²