

17 – 19 April 2023 · Antwerp, Belgium

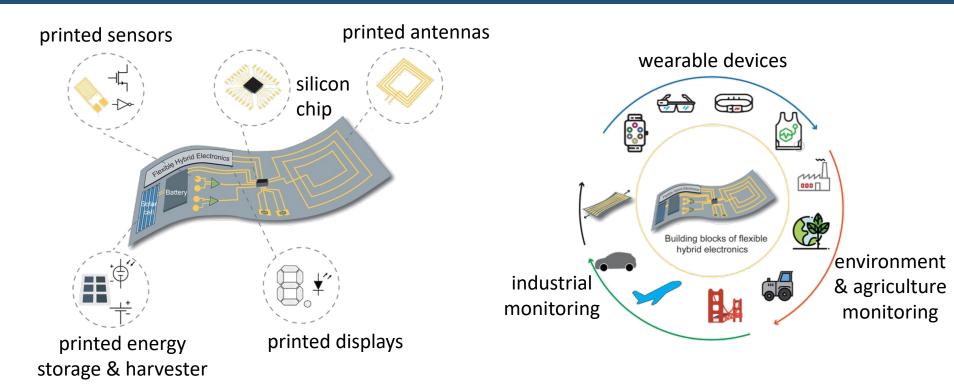
The European Event for Electronic System Design & Test

Split Additive Manufacturing for Printed Neuromorphic Circuits

Haibin Zhao, Michael Hefenbrock, Michael Beigl, Mehdi B. Tahoori
Karlsruhe Institute of Technology (KIT)

- Printed Neuromorphic Circuits
- Split Additive Manufacturing
- Experiment
- Conclusion

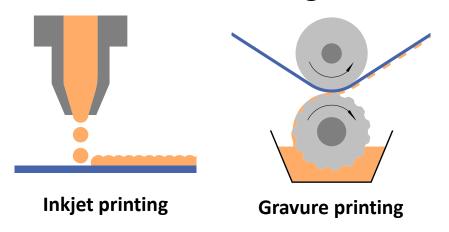
Printed Electronics – Overview



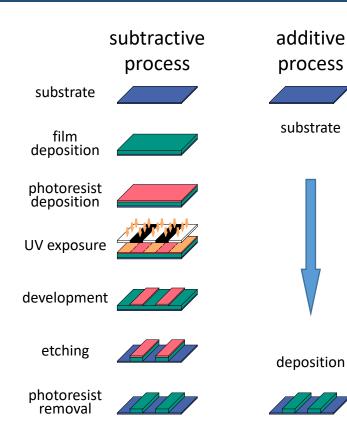
Source: Khan Y, et al. "A New Frontier of Printed Electronics: Flexible Hybrid Electronics". Advanced Materials, 2020

Printed Electronics – Manufacturing

Additive Manufacturing

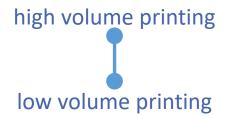


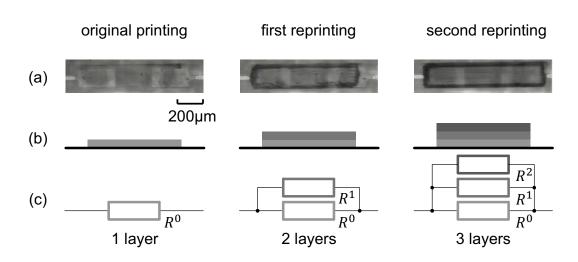
	Low volume process	High volume process
printing speed	-	+
customization	+	-



Printed Electronics – Reprinting

- Additive Manufacturing
 - Reprinting
 - Post processing
 - Repair
 - Split manufacturing

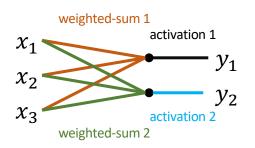




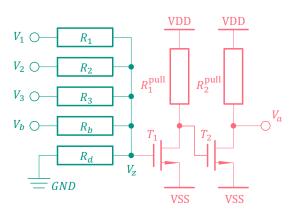
- Printed Neuromorphic Circuits
- Split Additive Manufacturing
- Experiment
- Conclusion

Printed Neuromorphic Circuit – Motivation

- Conventional digital NNs are infeasible for PE
 - Large feature size
 - Low integration density
 - Low device count



Campananta	Number of transistors		
Components	4-bit digital NN	Analog NN	
Input converter	185	-	
Weighted-sum	265	≤ 4	
Activation	10	2	



Analog neuromorphic circuits were developed

Printed Neuromorphic Circuit – Primitives

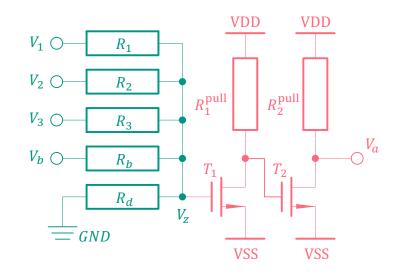
Resistor crossbar for weighted-sum

$$V_Z=\frac{g_1}{G}V_1+\frac{g_2}{G}V_2+\frac{g_3}{G}V_3+\frac{g_b}{G}V_b$$
 where $g_i=\frac{1}{R_i}$, G is the sum of g_i , $V_b\equiv 1V$.

Tanh-like activation circuit

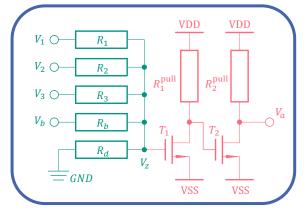
$$V_{\text{out}} = \text{ptanh}(V_{\text{in}})$$

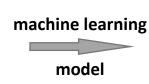
= $\eta_1 + \eta_2 \cdot \text{tanh}((V_{\text{in}} - \eta_3) \cdot \eta_4)$



Printed Neuromorphic Circuit - Design

Printed Neuromorphic Circuit

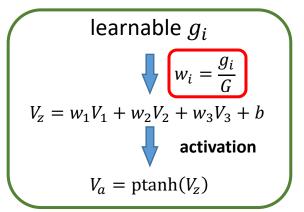




THE STATE OF THE S



Printed Neural Network





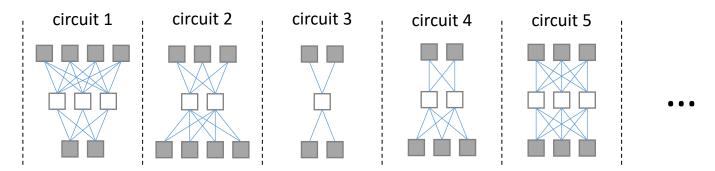
well-trained g_i

- Printed Neuromorphic Circuits
- Split Additive Manufacturing
- Experiment
- Conclusion

Split Additive Manufacturing – Motivation

Scenario

Numerous different circuits for different tasks



- Problem: despite the large printing batch, only low volume printing technologies can be adopted -> time consuming
- Idea: combine high and low volume manufacturing
 - High volume common part of circuits
 - Low volume point-of-use correction

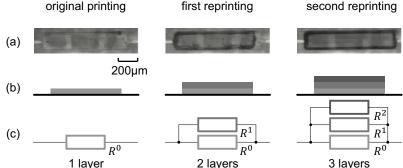
Split Additive Manufacturing – Idea

- Combination of high and low volume printing
 - Recall resistor reprinting

$$\frac{1}{R} = \sum_{l} \frac{1}{R_l} \rightarrow g = \sum_{l} g_l$$

ullet Split each learnable conductance g into

$$g = g^C + g^I$$



first reprinting

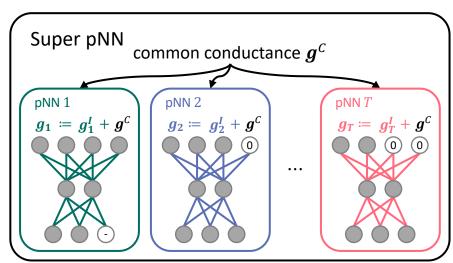
- g^{C} : common part shared across all circuits high volume process
- g^{I} : point-of-use individual part for each circuit low volume process

second reprinting

Split Additive Manufacturing – Idea

Super pNN

- A model contains multiple pNNs for different tasks with
 - One learnable parameter $oldsymbol{g}^{\mathcal{C}}$ high volume printing
 - Multiple independent learnable parameters g_t^I for each task
 - Resulted conductance $g = g^I + g^{\mathcal{C}}$



Split Additive Manufacturing – Idea

Training objective of the super pNN

$$\mathcal{L} = loss + \alpha \cdot cost$$

- loss: cross entropy loss (classification accuracy)
- α : trade-off between accuracy and cost
- Estimated cost: $C = ||\boldsymbol{g}^I||_1 = \sum_i |g_i^I|$
 - Template cost can be ignored due to large number of circuits
 - Material cost stay constant regardless of printing technology
 - Production efficiency

- Printed Neuromorphic Circuits
- Split Additive Manufacturing
- Experiment
- Conclusion

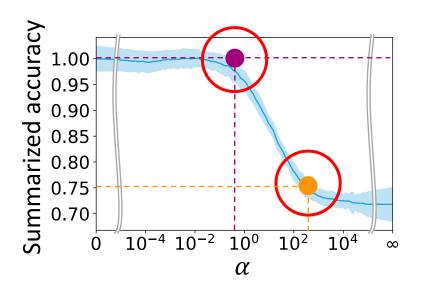
Experiment – Setup

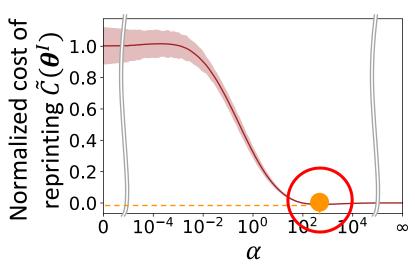
- Super pNN contains 30 benchmark datasets
- $\alpha \in [10^{-5}, 10^{5}]$ (trade-off between accuracy and cost)
- Baseline
 - Baseline1: $\alpha = 0$ (independent learning of all pNNs)
 - Baseline2: $\alpha \to \infty$ (same pNN for all tasks)
- Evaluation metric
 - Accuracy
 - Normalized accuracy (by baseline1)
 - Summarized accuracy
 - Cost: normalized cost (by baseline1)

```
\mathcal{L} = loss + \alpha \cdot cost
```

Experiment – Result

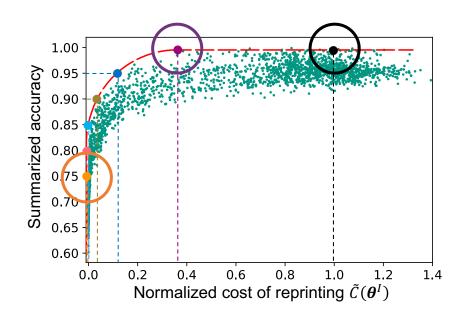
- α vs. accuracy
- α vs. cost

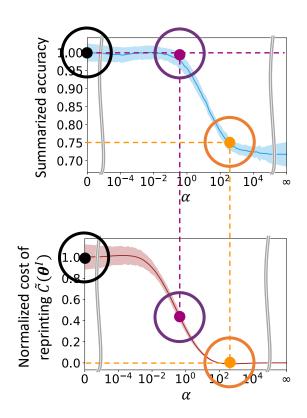




Experiment – Result

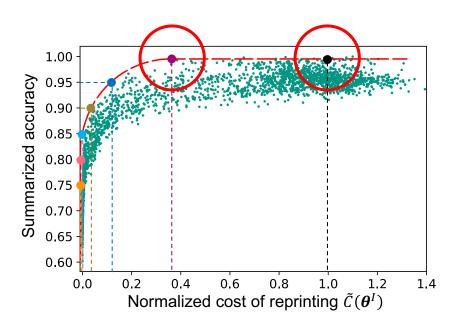
Pareto front - cost vs. accuracy





Experiment – Result

Pareto front - cost vs. accuracy



	Accuracy	Cost	
independent	100%	100%	
	100%	38.6%	
split additive manufacturing	95%	15.7%	
	90%	5.7%	
	85%	2.9%	
	80%	1.4%	
common	75%	0%	

- Printed Neuromorphic Circuits
- Split Additive Manufacturing
- Experiment
- Conclusion

Conclusion

- Printed electronics provides complementary advantages
 - Compared to traditional silicon-based VLSI technologies
- Low device count, large feature sizes, large latencies
 - Constraints for printed circuits
- Printed analog neuromorphic circuits
 - Analog computing to reduce device count
- Split additive manufacturing
 - Combining
 - High volume printing -> reduces cost
 - Low volume printing -> guarantees accuracy
 - Even suitable for
 - Different circuits
 - Small batch for each circuit
 - Bridges the gap between high and low volume processes

Split Additive Manufacturing for Printed Neuromorphic Circuits

Thank you for your attention

Haibin Zhao, Michael Hefenbrock, Michael Beigl, Mehdi B. Tahoori

Karlsruhe Institute of Technology (KIT)