Circuit Routing in Electronics Design Automation

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Abstract. The constant evolution of semiconductor technology has increased the design complexity of integrated circuits and printed circuit boards. As such, the manual design of modern printed circuit boards has been extremely time-consuming, expensive and with a high rate of difficulty. As a result, a large amount of research has been dedicated to studying typical circuit routing algorithms and the corresponding circuit routing tasks. There are several most common routing tasks: escape routing, length-matching routing, bus assignment, and layer minimization, on which this paper is focused. Moreover, we proposed an optimal mixture of classic and recent algorithms for completing each task. In addition, we described an algorithm that combines machine and human intelligence to optimize the circuit routing design automation.

Keywords: electronic design automation, printed circuit board, integrated circuit, circuit routing algorithms

1 Introduction

According to Moore's Law[11], the number of transistors on an integrated circuit(IC) would double every 18 months. As a result, modern IC and Printed Circuit Board(PCB) designs consist of millions of transistors, packages with multiple chips and thousands of pins. This increase results in a constant challenge to the reliability and scalability of the circuit design flow. Therefore, new challenges cannot be effectively handled by using traditional IC routing approaches in high-speed PCB designs. Moreover, the manual design of modern PCBs has been extremely time-consuming, expensive and with a high rate of difficulty. Electronic Design Automation(EDA) is an industry that operates with software support for engineers and uses algorithms in order to automate the process of ICs and PCBs design creation. EDA tools and algorithms are required to achieve more efficiency and are essential when designing high-end PCB boards and ICs. This paper focuses on studying typical circuit routing algorithms that are part of these software tools. The rest of the chapter is organized as follows: firstly, a short overview of PCB, followed by a brief presentation of routing and routing tasks. Lastly, the organization of this paper is going to be shown.

1.1 Overview of Printed Circuit Board

A printed circuit board consists of a layer of copper foil laminated to the substrate of a thin insulating board. Several isolated conductive paths are positioned on the surface of the board. Their function is to interconnect an assembly of electrical and electronic components that represent a physical implementation of a complex schematic circuit drawing. As part of an electronic device, the components of a PCB are composed of flip-flop circuits and logic gates. Thus, a modern PCB incorporates a set of packages such as memories, multi-chip and I/O modules. The footprints of such packages are arrays of pins. Non-crossing wires should be used to connect these pin arrays. In order to accommodate all the wire connections, it is required to use multiple layers to prevent the appearance of design rule violations and to satisfy all the routing tasks, as shown in Fig. 1. Based on the number of layers, PCB is categorised into three types: single-sided board, double-sided board and multi-layer board.

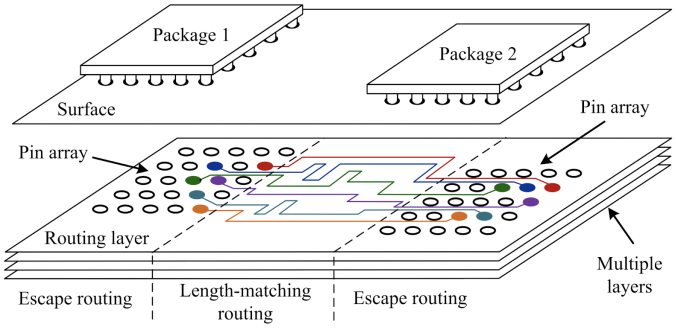

Fig. 1. An illustration of a PCB routing[29].

The first versions of PCBs comprised one layer, traditionally called single-sided boards. The routing wires are positioned only on one side of the layer. This type of design created a multitude of constraints, such as the crossing conflict between two wire segments situated on the same board area. In addition, the increase of the large net count and high pin density make routing extremely time-consuming and complex. As such, the use of this type of layering has considerably decreased.

The double-sided board consists of copper on both sides, each being isolated from the opposite. Therefore, the vias holes are required to connect the wires between different layers. There are generally four types of via holes: through, buried, blind, and micro-vias, as shown in Fig.2. The double-sided board is a two-layer board, which is why only through vias are needed to connect the wire segments of different layers. There are many advantages of using such a layout compared with the single-side board, such as a bigger routing area and the

possibility of routing the wires between different layers. In addition, some of the single-sided board problems, e.g. the crossing wires and the routing resource limitation, can be solved. Thus, this type of layering is the most popular amongst PCB designers because it is easy to produce and use.

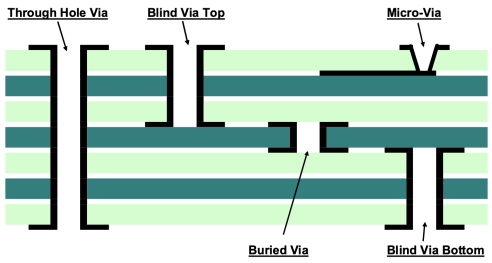

Fig. 2. Types of Via used in PCB design[5].

The multi-layer board is an amalgamation of single and double-sided boards. Its main advantage is the increase of the routing area. All types of vias can be integrated to connect the wire segments on different layers. In addition, it allows a larger amount of packages and pins.

However, the introduction of vias in the process of routing, as well as a large number of wire segments, can lead to serious signal integrity issues. Therefore, integrating vias in the middle of the routing should be minimised. As such, the routing has to be done using various algorithms.

1.2 PCB routing and common routing tasks

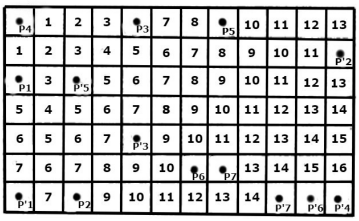

Fig. 3. Systematical search of the adjacent cells between P_4-P_4' based on Lee's Algorithm[6].

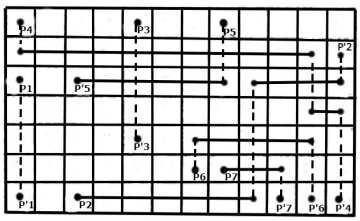

Fig. 4. The result after routing the wires based on Lee's Algorithm[6] starting with P_1-P_1'.

The purpose of PCB routing is to properly connect the electrical and electronic components while adhering to design rules. Lee's algorithm[6] is one

of the most basic algorithms used to satisfy this set of rules. This algorithm works by systematically searching for a path between two points that must be routed. In this method, as illustrated in Fig.3, each wire point is shown as a square, with one of the points being a starting point while the other represents the target point. Then a basic path is found by connecting the start and the finish using the adjacent empty cells while avoiding the obstacles. After reaching the target point, a retracting procedure is initiated to identify the path with the minimum number of turns from the target point to the starting point, similar to Fig. 4.

This fundamental algorithm has the advantage that it can always provide a systematic way to connect two points. However, the early routing process is done without considering the pins that need to be routed in the future. As such, there is a possibility that the later wires cannot be successfully routed because the early routing prevents finding the most suitable solution. This method also requires via holes to be used when obstacles are impossible to avoid, which, as mentioned in the earlier section, are unsuitable for efficient PCB routing.

Lee's algorithm has been used as a base for different kinds of routing algorithms. However, due to the growth of circuit routing, the design rules and constraints are getting more strict and varied. As such, there are a few well-defined and commonly studied tasks for PCB routing: escape routing, length-matching routing, bus assignment and layer minimisation. The described algorithm refers to area routing, which also includes length-matching routing.

Escape routing involves routing from inside the pin arrays to the peripherals of the arrays inside the components, as demonstrated in Fig.1. In other words, it aims to help a group of pins "to escape" the pin array. The length-matching routing task is a special case of the area routing problem. Since the area routing connects the previously escaped routes of two or more components without any constraints, the length-matching routing is to connect the escaped routes between pin arrays of different components while satisfying stringent length constraints, which can be seen in Fig.1. As such, the length-matching routing can also be called area routing with length-matching constraints.

Escape routing and length-matching routing have different tasks. The escape routing dominates the total number of layers. The major goal is to escape a set of pins using as few layers as possible while preparing a suitable base for pin placement on the periphery of the examined components to provide a planar topology for the later length-matching routing. On the other hand, the primary objective of the length-matching routing is to route the pin pairs to accommodate the length constraints while maintaining the planar topology inherited from escape routing.

The bus assignment and layer minimisation tasks indicate that all the given buses in a modern PCB can be assigned to a minimal group of routing layers. The main idea in a bus-driven design is to route the buses using as few layers as possible while avoiding design rule violations. Similarly to how pins are routed, different algorithms are employed to find relevant results.

1.3 Organisation of the Paper

The rest of the paper is organized as follows: Section 2 presents the escape routing task in detail. In section 3, the length-matching routing task is thoroughly discussed. Then, section 4 proposes a comprehensive study of the bus assignment and layer minimization tasks. Afterwards, AI-assisted routing is discussed in section 5. Finally, section 6 offers a conclusion to the paper.

2 Escape Routing

Generally, escape routing can be classified into net-oriented and bus-oriented escape routing. A net specifies how a node is physically represented on a PCB and determines how part pins are connected. On the other hand, a bus represents a multi-wire connection composed of multiple nets with the same signal. In net-oriented routing, the nets inside two escape buses may be mixed up and routed in the same layer. In the bus-oriented routing, on the other hand, the nets inside a single escape bus are not expected to be mixed up with any foreign net and are routed together. However, in this section, only the escape routing on the net level will be researched in detail. The bus-oriented escape routing will be studied in chapter 4 when exploring the bus routing task. Escape routing at the net level is categorised into unordered escape routing(UER), ordered escape routing(OER) and simultaneous escape routing(SER).

2.1 Unordered Escape Routing

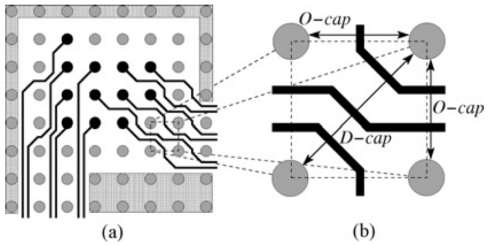

Fig. 5. (a) Example of the escape routing task and (b) enlarged view of a tile[41].

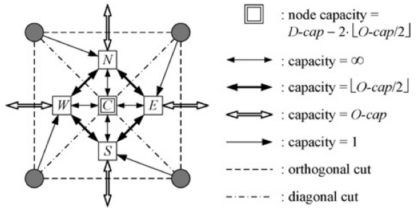

Fig. 6. Network Flow Model inside tile[41].

Unordered escape involves identifying a legal routing path from a pin to an escape point for each net without any constraint on the pin ordering along the boundary. It refers to only one pin array.

There are two general approaches: the non-flow model and the network-flow model. The non-flow model is used to solve a full grid escape problem, a typical

package problem. The PCB grid resembles the layout's intersecting horizontal and vertical lines. Coordinates for component placement and routing are formed on the PCB where the grid lines cross. In the full grid escape problem, all the pins in the grid are expected to be escaped in one or multiple layers. For example, Yu and Dai[23], [22] worked on a monotonic routing style to route all pins in a pin array on one layer. On the other hand, this model does not apply to problems in which a set of specified pins is expected to be escaped on the same layer. In this case, the network-flow model is the most widely chosen approach. Therefore, it is pervasively used to model this task in[9], [8], [32], [31], [42], [4], [41].

The network-flow model can be solved by introducing the orthogonal and diagonal wiring capacity. The number of wires between orthogonally and diagonally adjacent pins in the array pin is limited based on modern design rules. According to Yan and Wong's work[41], such constraints are called orthogonal(O-cap) and diagonal capacity(D-cap), as can be seen in Fig.5. As shown in (b), a tile of the pin array is a square formed by four adjacent pins. In this case, the number of wires passing through the tile's four sides is limited by O-cap. Meanwhile, the number of wires passing through the tile's two diagonals is limited by D-cap. The example from Fig.5 shows the case in which O-cap = 2 and D-cap = 3.

The network-flow model views each routing path as a unit flow from the pin to the periphery of the package. Since no order is specified, a flow solution always corresponds to some non-crossing routing. The diagonal capacity is essential for 45° routing in most components and PCBs. It is not considered in any of the previously mentioned network-flow models. In the traditional network-flow model employed by[9], [8], [31], and [4], each pin is designated by a pin node and each tile is designated by a tile node. Consequently, from the pin nodes to their adjacent tile nodes, and also between horizontal and vertical nodes, edges are added.

The network-flow model[9], [8] limits the number of wires inside a tile. This may lead to a suboptimal solution since tile capacity does not correctly reflect diagonal capacity. On the other hand, the networks of [31] and [4] may violate the design rule result because they ignore the diagonal capacity. The reference [42] is based on the triangulation of the pins, which captures only one of the two diagonals in a tile. Accordingly, its model may correspondingly include capacity violations on the other diagonal. The model [32] solely gives an upper-bound assessment of the number of routable nets. In conclusion, none of the mentioned network flow models can model the diagonal capacity correctly.

Consequently, Yan and Wong[41] offered a network-flow design that could precisely grasp the diagonal and orthogonal capacity. They can control the flow in accurate detail inside each tile by adding nodes and edges, thus capturing the diagonal capacity, as shown in Fig.6. Their other contribution is to consider missing pins in their model.

2.2 Ordered Escape Routing

Similarly to UER, OER considers only one pin array and entails restricting the escape order of the nets along each component's boundary. As such, successfully completing this task entails using a different methodology.

Because the flow does not maintain the ordering information, the network-flow models cannot be applied to the ordered escape task. Contrary to UER, OER involves an artificial arrangement or restriction of the escape order. As a result, it is more suitable for modern PCB designs.

There are multiple kinds of research on the subject of ordered escape routing. This section will start with the traditional and most studied algorithms for this type of task: boolean satisfiability (SAT)-based algorithms and integer linear programming(ILP) algorithms.

SAT-based algorithms were intensively used to attempt to resolve the OER tasks. In 2008, Luo and Wang[18] presented an algorithm where the OER task is offered as an SAT task and used an existing SAT solver to complete it. They proposed a partition technique to decompose large, challenging tasks into more minor and manageable ones. It reduces but does not eliminate the time complexity problem when the escape route's grid size increases. Due to its efficiency, they later proposed to rip up and reroute a small region where other heuristic-based routers are not able to finish the routing. They developed the algorithm to handle cyclic ordering and pin clustering in later research[19]. However, a quicker algorithm based on hierarchical bubble sorting was suggested by Yan in [38].

ILP is another approach for solving OER tasks. Fang et al.[7] presented an algorithm with the OER problem as an ILP task and used an existing ILP solver to solve the task optimally. Consequently, it reaches a rapid routing time. Unfortunately, since they assume non-monotonic routing only when their routing graph has a cycle, their ILP formulation does not ensure optimality. In 2016, Jiao and Dong[10] published a Min-cost Multi-commodity Flow (MMCF) algorithm. It was the first algorithm that optimized the total wire length of OER using an existing ILP solver. Nevertheless, the model may lead to increased time complexity due to multiple redundancy variables and constraints when solving it with an ILP solver.

Recently, Liao and Dong[16] proposed a compact algorithm driven by linear constraints to find and reduce some impractical solutions. A set of new variables were presented to create an injective map in which each solution of an OER task can be defined by just one model solution. Then, they offered a heuristic algorithm that decreases the search region size for each item in the base network flow model. On the one hand, it further decreases the number of variables and constraints. On the other hand, it decreases computational complexity. Then, based on the heuristic algorithm's results, a partitioning strategy is devised. As a result, the CPU time can be shrunk. The experiments demonstrate that this approach can reduce the ILP variables(constraints) by approximately 79.43%(74.05%) and can reach 100 times speed up without losing optimality in comparison to the earlier method from [10].

Another approach to completing the OER task was simplifying the task by adding restrictions on the routing. For sequential OER, Kubo and Takahashi[15], [14] proposed to add a monotonic routing constraint. They implemented a monotonic via assignment technique to ensure the feasibility of monotonic OER for two-layer ball grid array packages.

2.3 Simultaneous Escape Routing

Simultaneous escape routing requires simultaneously escaping the circuit pins inside two pin arrays. The SER task is relatively less studied because it involves only PCB routing compared to UER and OER, which additionally are applied to other electronic components. However, SER provides an optimal solution for the escape routing of two connected components and the corresponding crossings concurrently. The UER and OER do not present a hopeful solution because escape ordering, preferring escape routing, may complicate area routing and the other way around.

Ozdal and Wong can be regarded as the pioneers of the SER task. In their works[26], [27], they designed 16 routing patterns for each pin and then selected one of the patterns per pin to minimize the mismatched net ordering along the two boundaries. The patterns were then chosen according to the longest path with the forbidden pairs problem. Moreover, they proposed a precise polynomial-time algorithm for simpler problems which is guaranteed to find the maximal planar routing solution on one layer. They used a randomized algorithm approach for routing with better scalability in the case of complex problems.

In a later study[28], they proposed a more generalised algorithm. They used a congestion driver router to generate the routing pattern and took performance constraints such as adjacence, length-matching constraints and differential pair routers. The congestion driver router plays a huge role in the efficiency of the entire algorithm. On the one hand, the algorithm supplies the promised solution for smaller circuits. On the other hand, the optimal solution can not be achieved in larger circuits with the complex shape of escape routing by challenging escape problems.

Luo et al.[20] solve the problem of dense PCBs. Their boundary routing solution consists of building a routing boundary for all the pins inside a pin grid and allowing the routing path to track the boundary as much as possible when routing a net. Then the resulting routed net is excluded by shrinking the routing boundary. Even if this approach is very effective for complex layouts, it can provoke pin blockage when a specific zone is eliminated and boundaries are shrunk.

In a later work, Ali et al.[3] presented an alternative method using an optimization modelling technique to solve the SER task. A network flow approach is utilized to map the SER and area routing tasks as network routing. As a result, two distinct algorithms are proposed: link-based routing, which uses ILP and nodes-based routing, which uses non-ILP to discover the optimal routes. They decreased the time complexity and performed 100% routability. However, the models are efficient in routing over small grids but inefficient when run over

larger grids. Recently, they extended their previous study[2] to solve the larger grid problem and optimize the algorithm. Here, they use only ILP algorithms while connecting the local and global routing algorithms to reach end-to-end routing. In conclusion, this algorithm is superior to the earlier algorithms by performing 99.9% routability and is autonomous of grid topology and component pin arrangement.

In another recent work, Lin et al.[17] proposed an alternative approach which includes a comprehensive PCB routing process, including SER, post-SER improvement, and gridless area routing. The suggested SAT-based concurrent hierarchical SER and MAX-SAT–based post-SER improvement can conclude layer assignment and develop a consistent escape order per layer among all components of the PCB. In addition, the number of required vias is minimized, and a robust basis for fulfilling group length-matching constraints for a provided PCB design is delivered. The suggested adaptable snaking unit can help expand the wire length of a net with length slack to an acceptable rank. The experiments show promising results by routing seven commercial PCB layouts, where any commercial PCB tools can solve none.

3 Length-Matching Routing

The high clock frequencies on modern PCBs are a big topic in circuit routing. Due to the strict length rules of the nets, the general routing process can be categorised into escape routing and area routing. In the last section, the escape routing was studied in detail, which is why it is not further explained. Consequently, area routing is to finish the links between the boundaries. The task of length-matching routing is to carefully detour the wires to meet the length bounds while maintaining the planar topology inherited from escape routing, as was already demonstrated in Fig.1.

Generally, the length-matching constraint is divided into min-max length bounds and bounded length difference. The minimum and maximum length bounds for each net are offered in the case of the min-max length bounds. At the same time, the length of the routing cannot exceed the limits of the boundary. In the case of the bounded length difference, it is anticipated that the length of a set of nets to be equal. To put it differently, a given bound acts as a regulation for the difference between the length of a group of nets.

The minimum length bound can be satisfied when the short wires are extended. However, deliberately increasing wire length is commonly avoided in circuit routing, making length-matching routing a unique task in PCB routing.

The snaking of wires is the most used technique to increase the wire length. However, its big disadvantage is the possible blockage of other wires by snaking a wire, which is the main reason that limits the usage of greedy approaches. The greedy algorithms need a global view of balancing the requirements of wires, which, as said earlier by snaking, is not usually possible.

Ozdal and Wong[24] proposed an approach without a greedy resource allocation for wire extension. A Lagrangian relaxation approach was used to

distribute routing resources based on each wire length and available length slack. In order to determine the minimum cost path to reach the desired length in the PCB layout, they proposed a directed acyclic graph with a specific number of vertices. Despite promising results, this approach has two potential problems. Firstly, a long runtime appeared because of the increasing number of router iterations required to perform the actual routing when the problems were too complex. Secondly, each net's routing must be monotonic in one direction, restricting the approach's application.

Yan and Wong[40] solve these problems by proposing a length-matching approach without limitation on the routing topology while eliminating their router's monotonic restriction on the routing. In their approach, the length-matching routing is regarded as an area assignment issue. This issue was then converted into a mathematical programming problem by applying a bounded-sliceline grid (BSG) structure described in detail in Ref.[25]. Due to this conversion, the area assignment issue could be indirectly solved through an optimal iterative approach. One of the main advantages of this approach is the possibility of making general topology manageable. Another huge benefit is that the router is gridless. Furthermore, the problem of routing's grid size dependence is eliminated compared to previous approaches. After comparing it with the Lagrange relaxation router[24], a significant speedup was identified. Unfortunately, this approach can meet trouble when the layout is agglomerated with many obstacles. In this case, the generation of an optimal topology is not an easy task.

In a later paper[36], the problem with obstacles from [40] was solved by substituting the BSG with linking the neighbour areas in the Hanan grid. This substitution generates an alternative partition of the routing area. Then, a max-flow algorithm is used on the partition-generated adjacent graph to determine the routing topology. Eventually, the routing resources are applied to detour/untangle the nets to complete the length restriction through heuristics. Their router delivered promising outputs after a sequence of simulations.

4 Bus Assignment and Layer Minimisation

The complexity of the length-matching or timing-matching restrictions delivers a more complicated bus routing in high-speed PCB designs. Moreover, the minimization process of used layers in a PCB layout plays a huge role in the cost of manufacture.

Generally speaking, the assignment process of buses, in order to minimize the layers in PCB design, can be categorized into the bus assignment inside components and the bus assignment outside components.

The bus assignment inside components is also known as bus-oriented escape routing. As such, the buses inside a component can be escaped onto the component's available boundaries to minimize the number of layers. Moreover, the bus-oriented escape routing can be summarised as a rectangle arrangement issue. Fig.7 gives a general overview of the projection-based escape routing.

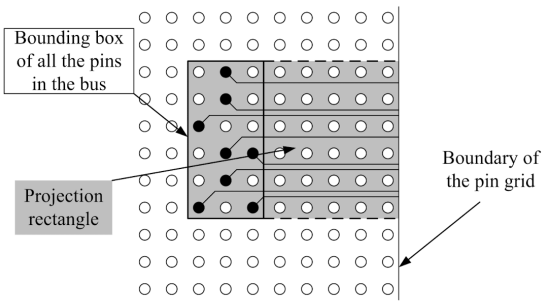

Fig. 7. Projection based escape routing style[29].

The given projection rectangles to the routing layers can be assigned to satisfy non-overlap and planar constraints on each layer. The main idea of non-overlap constraint is that no overlaps appear on the projection rectangles inside a pin array, based on Fig.8(a). Following this, according to Fig.8(b), planar constraints consist of matching the ordering of the two pin arrays' projection rectangle along the boundaries.

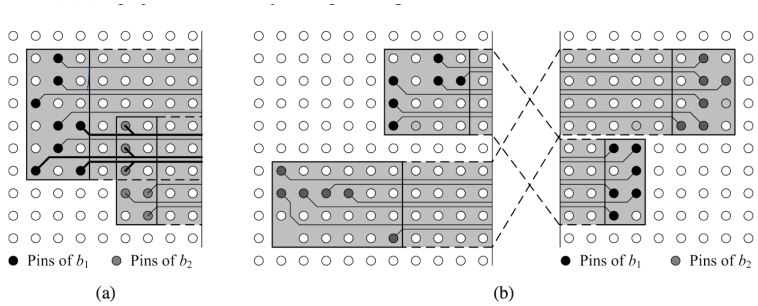

Fig. 8. Conflict between projection rectangles. (a): overlapping rectangles in a pin array lead to over-lapping escape routing; (b): reversed ordering of the rectangles in two pin arrays leads to wire crossing of two buses.[29].

On the other hand, the main task of the bus assignment outside components consists of assigning all escaped buses between components. The pins on any escaped bus must already be set on the boundary of a set of layers with a minimal constraint of the related component.

4.1 Assignment inside components

The bus assignment inside one component is also known as bus escape planning. In this case, there is no planar constraint, and only the non-overlap constraint

must be assumed. An optimal approach to discovering the disjoint boundary rectangles on two, three, and four available boundaries inside a larger rectangle was foremost studied by Kong et al.[13]. Nevertheless, the number of used layers in the bus-oriented escape routing cannot be minimized operating with this approach.

In a later work, Ma et al.[21] defined the rectangle escape problem (REP) in rectangle escape routing. Firstly, REP is formulated as the maximum clique size of the projection rectangles, which is minimized. In other words, a minimum of the maximum number of projection rectangles overlap is determined. To summarise, the lowest number of layers can be well estimated with the help of the largest clique size. Finally, the REP was solved by offering an approximation approach employing linear programming relaxation and rounding.

In [39], the REP problem was split into five assignment problems to minimize the number of layers according to the area of the available boundaries in the REP. Furthermore, a two-phase density-reduction oriented layer assignment can be applied to solve more complex problems optimally.

In order to solve the problem of the different escape directions for any bus that occurred in [39], an iterative algorithm based on the maximal densities of the buses on four boundaries was proposed by Yan and Chen in [37]. Their main idea was to decrease the maximal density of the buses that escaped to four boundaries in direction-constrained rectangle escape routing. Nevertheless, the maximal density of the buses that escaped to any of the four boundaries is just thought in a one-directional perspective for layer assignment, which may not lead to a relevant result for the 2-D layer assignment inside a bigger chip.

Ahmadinejad et al.[1] have recently continued to study the problem of obtaining the maximum disjoint set of boundary rectangles with application to PCB routing. The central concept of the algorithm is to control the optimal substructures of the problem and utilise dynamic programming to obtain a favourable result using optimal solutions to the smaller subproblems.

4.2 Assignment outside components

The bus assignment outside components in a PCB layout involves linking all buses among components positioned on the PCB. Kong et al.[12] developed the first automatic bus planer for complex PCB designs to simultaneously achieve global bus routing and layer assignment of the given buses. Furthermore, this bus planer is based on the bus decomposition and the escape routing result for a given cluster of buses. Moreover, the bus decomposition, escape routing, layer assignment, and global bus routing were solved simultaneously using an ILP-based bus planer proposed by Wu et al.[33].

In a subsequent work, Tsai et al.[30] proposed a global topological routing algorithm for single-layer routing. The approach was grounded on using a component connecting point (CCP) between two components and the dynamic pin sequence (DPS) to avoid net crossing. As such, the layer assignment of the given bus connections can be acquired by utilising the topological routing method for each consequent layer. Unfortunately, the CCP technique between

two components may determine the wiring route of the selected net. As a result, the number of assigned layers can grow considerably.

The task of layer minimisation discussed in previous works was later solved by Yan in [34]. The approach involves assigning all the nets inside a single bus on the same layer. However, the number of used layers may grow because of the bus pin's fixed places on the components' boundaries in the escape routing.

Recently, Yan in [35] proposed another algorithm of layer minimization. Firstly, they consider introducing flexible escape directions inside components in escape routing, which can decrease the number of used layers in bus assignment outside components. Then, the two upper bounds of the layer numbers inside and outside components can be computed. Lastly, an integrated algorithm can be further suggested to minimize the number of layers by eliminating the redundant bus connections for the buses and allocating all the physical connections of the buses onto the available layers.

5 AI-assisted routing

The advancement in PCB routing has been marked by a steady increase in the routing algorithms' difficulty, thereby making the task of a designer an almost impossible hurdle. That is why several approaches and algorithms are used to automate this difficult yet very important branch of the semiconductor industry. Consequently, the optimisation of human and machine interaction is worth researching for present and future endeavours.

The most recent research on combining human intelligence with ever-growing AI methods is GeniusRoute[43]. It is an entirely automated, analog routing model that combines machine learning with complex human layout procedures to provide routing assistance. However, it features analog routing, an approach that has to be driven according to the designer's experience instead of a fully automated set of algorithms. That is because this routing style offers a set of distinctive challenges, such as symmetric restrictions, that must be regarded alongside the usual PCB layout restraints.

That is where the GeniusRoute can display its best qualities. To uncover layout patterns and predict the appropriate human behaviour for routing, it uses machine learning(ML) models. The ML models automatically extract regulations from existing analog routing architectures and use the best-recorded approaches for layout and machine learning models to construct a template library. This vast knowledge is then used to predict the best routing path for the given nets while avoiding all the layout errors and starting the routing process. The detailed routing will adhere to the guidance produced by machine learning while respecting additional geometric restrictions like symmetry constraints. This routing model is successful in creating high-quality layouts with substantial performance. Its only limitation is that its ML models for analog routing still need to be researched and completed.

There are many different analog designs, making it challenging to establish a universally applicable model. Research and community involvement are the only

ways to advance this process. As such, currently, GeniusRoute cannot display its full potential. In the end, we anticipate seeing a variety of approaches to automating analog routing that leverages both human and artificial intelligence.

6 Conclusion

Modern circuit routing is a difficult and time-consuming process, which is why it tends to be automated. This paper provides suitable solutions for circuit routing optimisation in EDA, which includes common routing tasks while resolving various challenges and satisfying necessary conditions or constraints. Moreover, we offered an optimal combination of traditional and current solutions for each presented task. However, applying all these solutions requires very experienced designers. In order to solve this difficulty, a promising approach of combining human and machine intelligence was described. Based on this, using AI techniques and human design knowledge is a promising direction for future research.

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