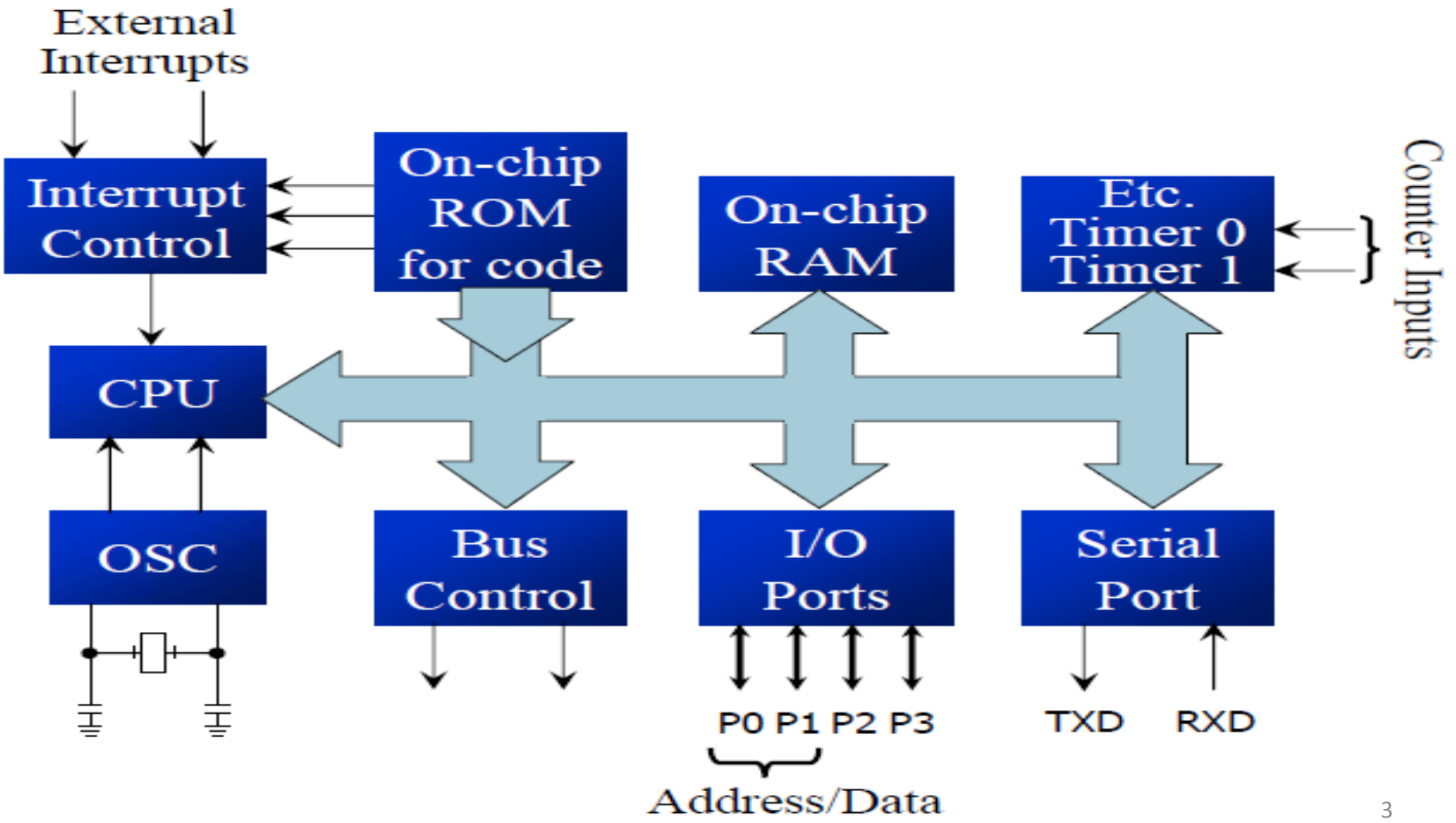
8051 Microcontroller

Salient Features

(1). 8 bit microcontroller originally developed by Intel in 1980.
(2). High-performance CMOS Technology.
(3). Contains Total 40 pins.
(4). Address bus is of 16 bit & data bus is of 8 bit.
(5). 4K bytes internal ROM (program).
(6). 128 bytes internal RAM (data).
(7). Four 8-bit I/O ports.
(8). Two 16-bit timers.
(9). Serial interface Communication.
(10). 64K external code & data memory space.
(11). 210 bit-addressable locations.
(12). Internal memory consists of on-chip ROM and on-chip data RAM.
(13). 8051 implements a separate memory space for programs (code) and data.
(14). Operating frequency is 24MHz-33MHz.
(15). +5V Regulated DC power supply is required to operate .
(16). It has four 8 bit ports, total 32 I/O lines.
(17). RAM, ROM, I/O ports, one serial port and timers are all on-chip.
(18). 6-interrupts (2 are external with 2 priority levels).
(19). Low-power Idle and Power-down Modes.
(20). Full duplex UART.
(21). 8051 has 21 special function registers (SFRs).

8051 Block Diagram



Internal Architecture

Oscillator Circuit:-

(1). The 8051 requires an external oscillator circuit.

(2). The oscillator circuit usually runs around 12MHz.

(3). The crystal generates 12M pulses in one second.

(4). The pulse is used to synchronize the system operation in a controlled pace.

(5). An 8051 machine cycle consists of 12 crystal pulses (clock cycle).

(6). Used for synchronizing internal operations.

(7). Pins XTAL1 & XTAL2 have been used.

(8). The length of machine cycle depends on the frequency of the crystal oscillator connected to 8051.

Internal Memory

(1). 8051 implements a separate memory space for programs (code) and data.

(2). Both code and data may be internal, however, both expand using external components to a maximum of 64K code memory and 64K data memory.

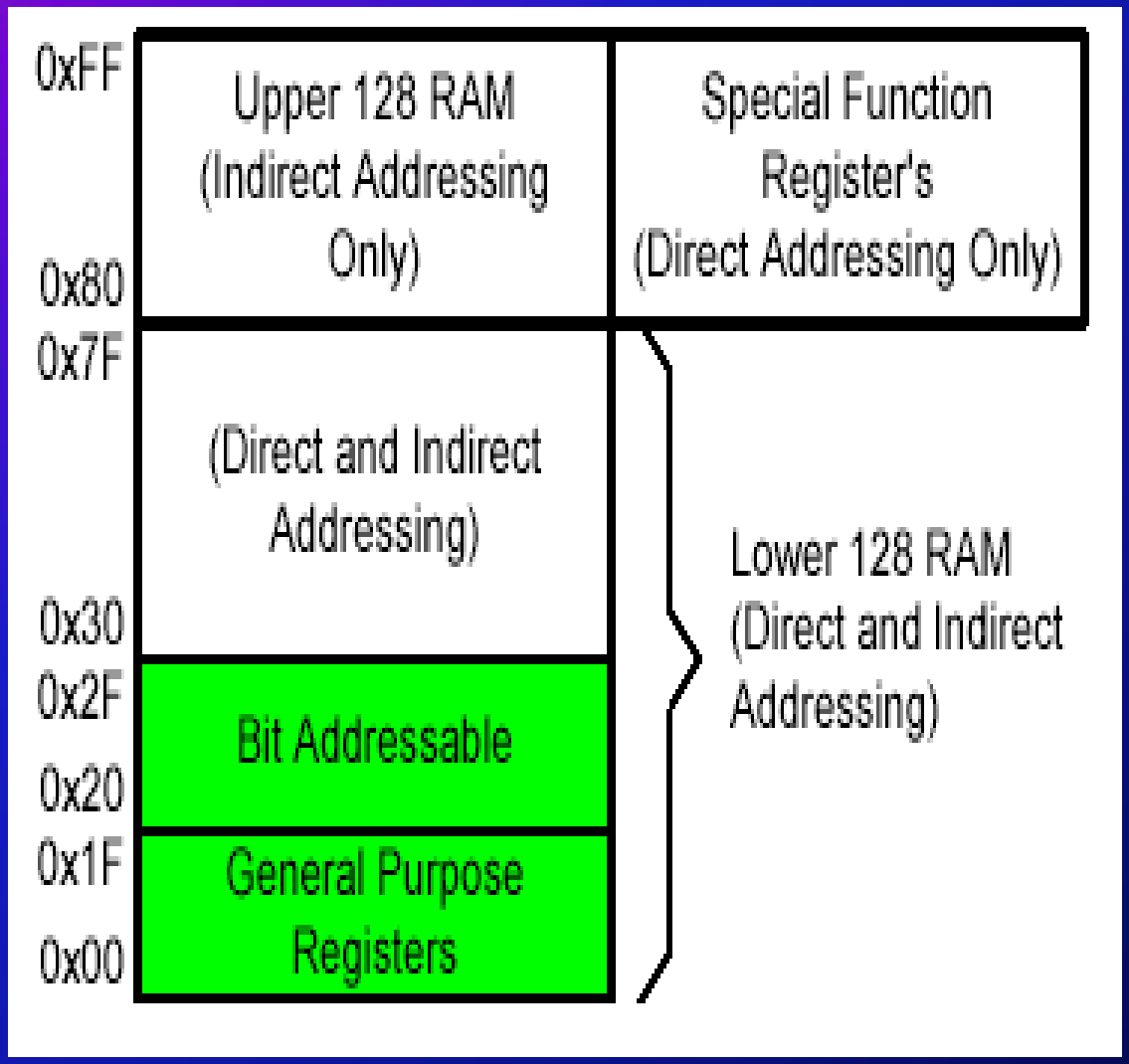
(3). Internal memory consists of on-chip ROM and on-chip data RAM.

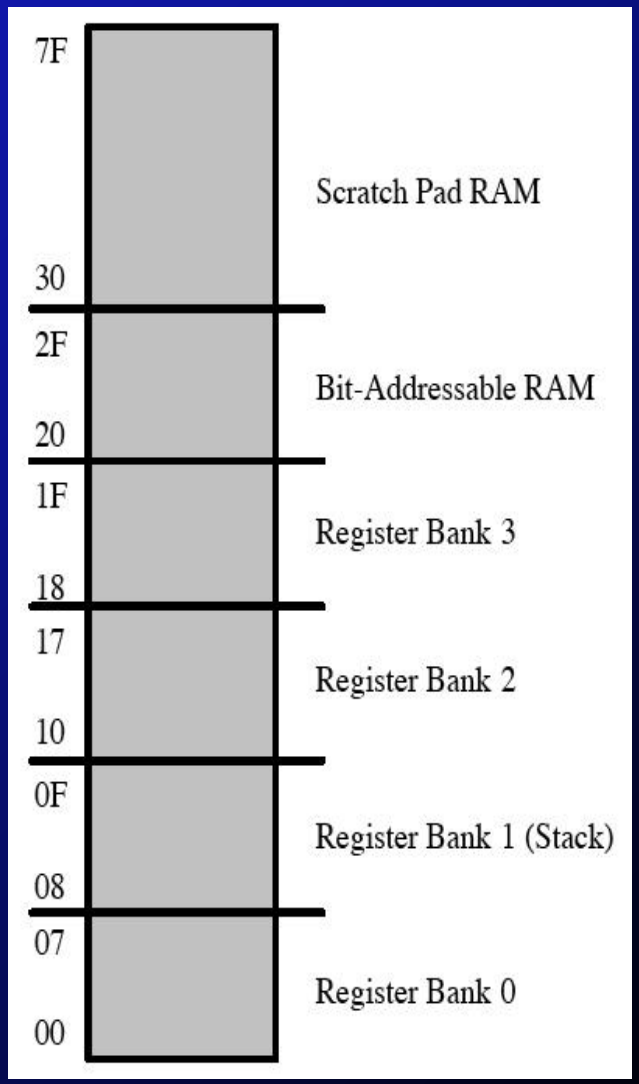
(4). On-chip RAM contains a rich arrangement of general purpose storage, bit addressable storage, register banks, and special function registers.

(5). In the 8051, the registers and input/output ports are memory mapped and accessible like any other memory location.

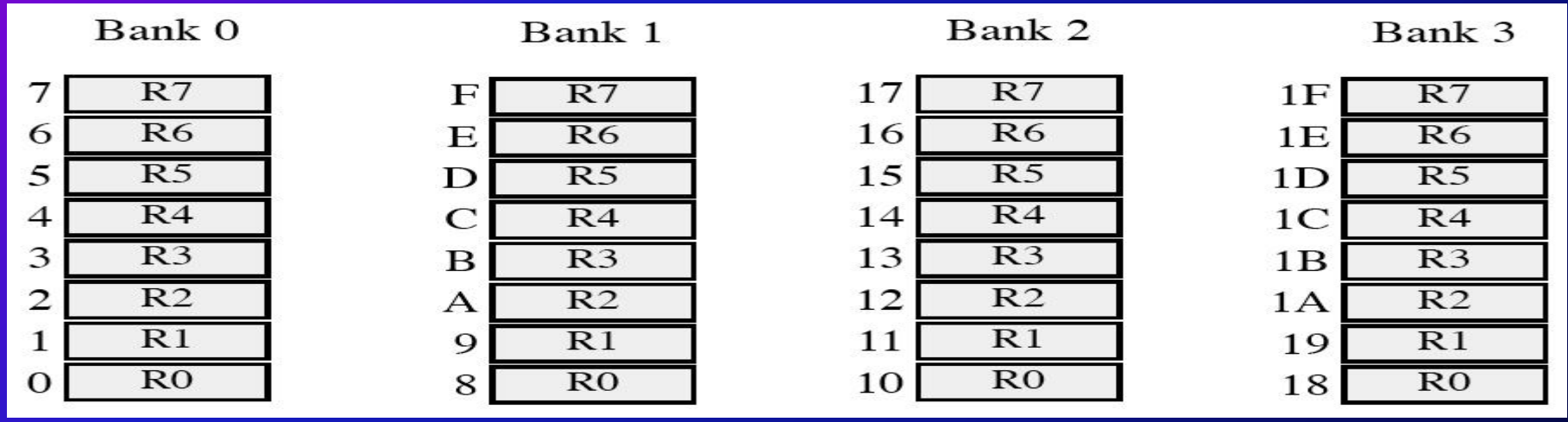
(6). In the 8051, the stack resides within the internal RAM, rather than in external RAM.

Registers RAM memory space allocation in the 8051 Microcontroller





Register banks in the 8051 Microcontroller



	RS1 (PSW.4)	RS0 (PSW.3)
Bank 0	0	0
Bank 1	0	1
Bank 2	1	0
Bank 3	1	1

Special Function Registers

(1). ACC

(2). B

(3). PSW

(4). SP

(5). DPTR

(5). IP

(6). PMODE

(7). PCON

(8). TMODE

(9). TCON etc.

Special Function Registers

(1). 8051 has 21 special function registers (SFRs) at the top of internal RAM from address 80H to FFH.

(2). Most of the addresses from 80H to FFH are not defined, except for 21 of them.

(3). Some SFR's are both bit-addressable and byte addressable, depending on the instruction accessing the register.

(4). This area consists of a series of memory-mapped ports and registers.

(5). All 8051 CPU registers, I/O ports, timers and other architecture components are accessible in 8051 C through SFRs

B Register

(1). B register or accumulator B is used along with the accumulator for multiply and divide operations.

(2). MUL AB: multiplies 8 bit unsigned values in A and B. and leaves the 16 bit result in A (low byte) and B (high byte).

(3). DIV AB: divided A by B, leaving the integer result in A and remainder in B.

(4). B register is bit-addressable.

PSW (Program Status word) / Flag Register

CY	AC	F0	RS1	RS0	OV	--	P

CY	PSW.7	Carry flag.
AC	PSW.6	Auxiliary carry flag.
F0	PSW.5	Available to the user for general purpose.
RS1	PSW.4	Register Bank selector bit 1.
RS0	PSW.3	Register Bank selector bit 0.
OV	PSW.2	Overflow flag.
--	PSW.1	User-definable bit.
P	PSW.0	Parity flag. Set/cleared by hardware each instuction cycle to indicate an odd/even number of 1 bits in the accumulator.

RS1	RS0	Register Bank	Address
0	0	0	00H - 07H
0	1	1	08H - 0FH
1	0	2	10H - 17H
1	1	3	18H - 1FH

Stack Pointer

(1). Stack pointer (SP) is an 8-bit register at address 81H.

(2). It contains the address of the data item currently on top of the stack.

(3). Stack operations include pushing data on the stack andpopping data off the stack.

(4). Pushing increments SP before writing the data

(5). Popping from the stack reads the data and decrements the SP

(6). 8051 stack is kept in the internal RAM

(7). Depending on the initial value of the SP, stack can have different sizes

(8). Example: MOV SP,#5FH

(9). On 8051 this would limit the stack to 32 bytes since the uppermost address of on chip RAM is 7FH.

Data pointer (DPTR)

(1). Data pointer (DPTR): is used to access external data or code.

(2). DPTR is a 16 bit register at addresses 82H (low byte) and 83H (high byte).

(3). The data pointer is used in operations regarding external RAM and some instructions involving code memory.

(4). Example: the following instructions write 55H into external RAM location 1000H:

- MOV A,#55H
- MOV DPTR,#1000H
- MOVX @DPTR,A

I/O Ports

(1). One of the major features of a microcontroller is the versatility built into the I/O circuits that connect the microcontroller to the outside world .

(2). To be commercially viable, the 8051 had to incorporate as many I/O functions as were technically and economically possible.

(3). One of the most useful features of the 8051 is four bidirectional I/O ports.

(4). Each port has an 8-bit latch in the SFR space as mentioned earlier.

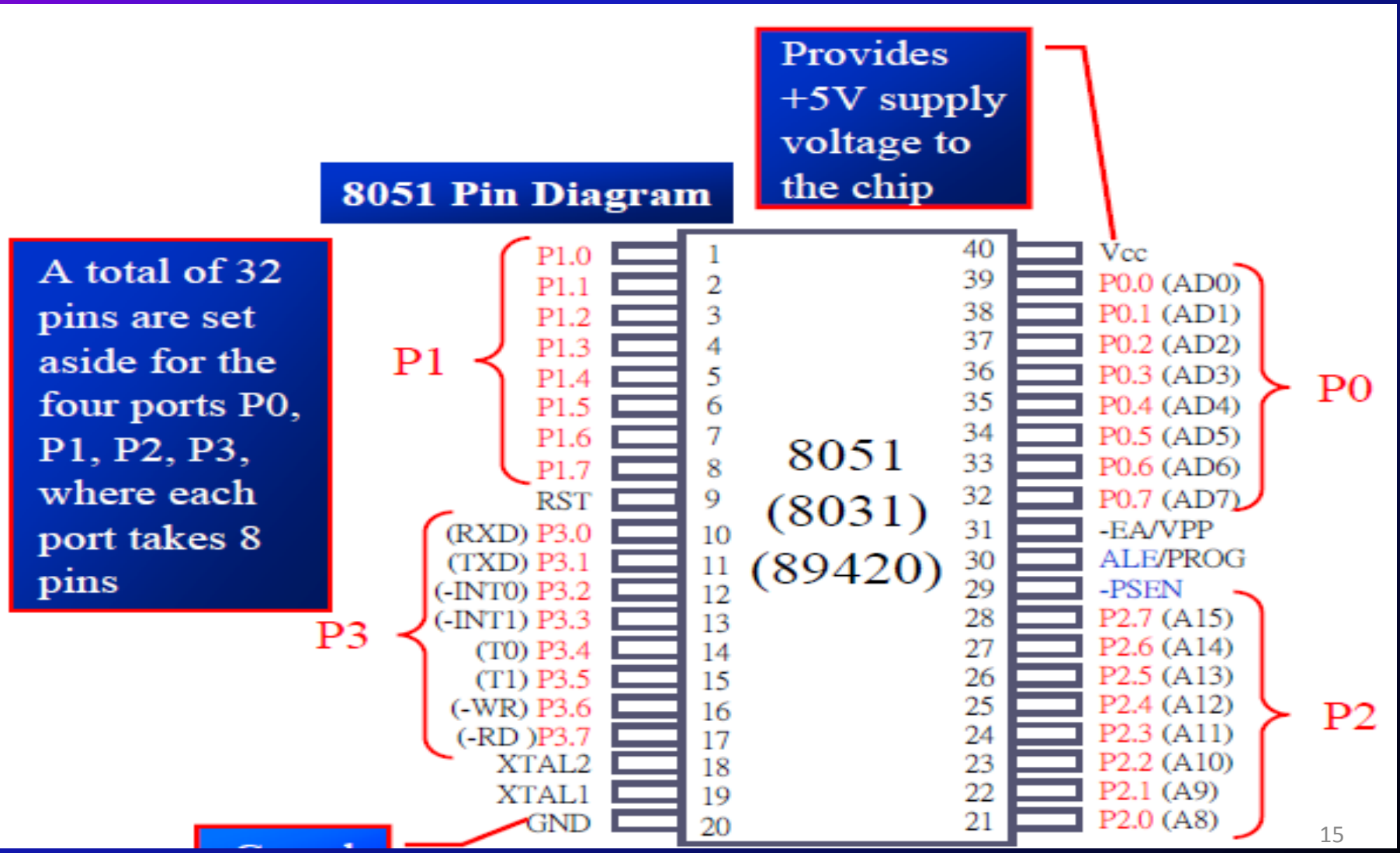
(5). To reduce the overall package pin count, the 8051 employs multiple functions for each port.

(6). Each port also has an output drive and an input buffer.

(7). These ports can be used to general purpose I/O, as an address and data lines.

(8). The four 8-bit I/O ports P0, P1, P2 and P3 each uses 8 pins

I/O Ports


Provides +5V supply voltage to the chip
8051 Pin Diagram
A total of 32 pins are set aside for the four ports P0, P1, P2, P3, where each port takes 8 pins
P1
P3
P0
P2
P1.0
P1.1
P1.2
P1.3
P1.4
P1.5
P1.6
P1.7
RST
(RXD) P3.0
(TXD) P3.1
(-INT0) P3.2
(-INT1) P3.3
(T0) P3.4
(T1) P3.5
(-WR) P3.6
(-RD) P3.7
XTAL2
XTAL1
GND
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
8051
(8031)
(89420)
40
39
38
37
36
35
34
33
32
31
30
29
28
27
26
25
24
23
22
21
Vcc
P0.0 (AD0)
P0.1 (AD1)
P0.2 (AD2)
P0.3 (AD3)
P0.4 (AD4)
P0.5 (AD5)
P0.6 (AD6)
P0.7 (AD7)
-EA/VPP
ALE/PROG
-PSEN
P2.7 (A15)
P2.6 (A14)
P2.5 (A13)
P2.4 (A12)
P2.3 (A11)
P2.2 (A10)
P2.1 (A9)
P2.0 (A8)

PORT 0

(1). Port 0 is 8-bitbidirectional I/O port.

(2). Port 0 pins can be used as high-impedance inputs.

(3). Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory.

(4). We r using pins no. from 32 to 39.

(5). When used as an output the pin latches are programmed to 0.

(5). When used as an input the pin latches are programmed to 1.

PORT 1

(1). Port 1 is an 8-bit bidirectional I/0 port.

(2). We r using pins no. from 1 to 9.

(3). Port 1 have no dual functions.

(4). When used as an output the pin latches are programmed to 0.

(5). When used as an input the pin latches are programmed to 1.

PORT 2

(1). Port 2 is an 8-bit bidirectional I/O port.

(2). Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR).

(3). When used as an output the pin latches are programmed to 0.

(4). When used as an input the pin latches are programmed to 1.

(5). We r using pins no. from 21 to 28.

PORT 3

(1). Port 3 is an 8-bit bi-directional I/0 port.

(2). We r using pins no. from 10 to 17.

- RXD (P3.0): Serial input port,
- TXD (P3.1): Serial output port,
- INT0 (P3.2): External interrupt,
- INT1 (P3.3): External interrupt,
- T0 T0 (P3.4): Timer 0 external input,
- T1 (P3.5): Timer 1 external input,
- WR (P3.6): External data memory write strobe,
- RD (P3.7): External data memory read strobe,

Timers and Counters

(1). Many microcontroller applications require the counting of external events, such as frequency of a pulse train, or the generation of precise internal time delays between actions.

(2). Both of these tasks can be accomplished using software techniques.

(3). The 8051 has two 16-bit registers that can be used as either timers or counters.

(4). These two up counters are name T0 and T1 and are provided for general use of the programmer.

(5). Each counter may be programmed to count internal clock pulses, act as a timer, or programmed to count external events as a counter.

(6). The counters are divided into two 8-bit registers called the timer low (TL0, TL1) and timer high (TH0, TH1) bytes.

TCON (Timer/Counter Control Register)

7	6	5	4	3	2	1	0
TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

Bit Number	Bit Mnemonic	Description
7	TF1	**Timer 1 Overflow Flag** Cleared by hardware when processor vectors to interrupt routine. Set by hardware on timer/counter overflow, when the timer 1 register overflows.
6	TR1	**Timer 1 Run Control Bit** Clear to turn off timer/counter 1. Set to turn on timer/counter 1.
5	TF0	**Timer 0 Overflow Flag** Cleared by hardware when processor vectors to interrupt routine. Set by hardware on timer/counter overflow, when the timer 0 register overflows.
4	TR0	**Timer 0 Run Control Bit** Clear to turn off timer/counter 0. Set to turn on timer/counter 0.
3	IE1	**Interrupt 1 Edge Flag** Cleared by hardware when interrupt is processed if edge-triggered (see IT1). Set by hardware when external interrupt is detected on INT1# pin.
2	IT1	**Interrupt 1 Type Control Bit** Clear to select low level active (level triggered) for external interrupt 1 (INT1#). Set to select falling edge active (edge triggered) for external interrupt 1.
1	IE0	**Interrupt 0 Edge Flag** Cleared by hardware when interrupt is processed if edge-triggered (see IT0). Set by hardware when external interrupt is detected on INT0# pin.
0	IT0	**Interrupt 0 Type Control Bit** Clear to select low level active (level triggered) for external interrupt 0 (INT0#). Set to select falling edge active (edge triggered) for external interrupt 0.

TMOD (Timer/Counter Control Register)

7	6	5	4	3	2	1	0
GATE1	C/T1#	M11	M01	GATE0	C/T0#	M10	M00

Bit Number	Bit Mnemonic	Description
7	GATE1	**Timer 1 Gating Control Bit** Clear to enable timer 1 whenever the TR1 bit is set. Set to enable timer 1 only while the INT1# pin is high and TR1 bit is set.
6	C/T1#	**Timer 1 Counter/Timer Select Bit** Clear for timer operation: timer 1 counts the divided-down system clock. Set for Counter operation: timer 1 counts negative transitions on external pin T1.
5	M11	**Timer 1 Mode Select Bits** M11 M01 Operating mode 0 0 Mode 0: 8-bit timer/counter (TH1) with 5-bit prescaler (TL1). 0 1 Mode 1: 16-bit timer/counter. 1 0 Mode 2: 8-bit auto-reload timer/counter (TL1). Reloaded from TH1 at overflow. 1 1 Mode 3: timer 1 halted. Retains count.
4	M01	
3	GATE0	**Timer 0 Gating Control Bit** Clear to enable timer 0 whenever the TR0 bit is set. Set to enable timer/counter 0 only while the INT0# pin is high and the TR0 bit is set.
2	C/T0#	**Timer 0 Counter/Timer Select Bit** Clear for timer operation: timer 0 counts the divided-down system clock. Set for counter operation: timer 0 counts negative transitions on external pin T0.
1	M10	**Timer 0 Mode Select Bit** M10 M00 Operating mode 0 0 Mode 0: 8-bit timer/counter (TH0) with 5-bit prescaler (TL0). 0 1 Mode 1: 16-bit timer/counter. 1 0 Mode 2: 8-bit auto-reload timer/counter (TL0). Reloaded from TH0 at overflow. 1 1 Mode 3: TL0 is an 8-bit timer/counter. TH0 is an 8-bit timer using timer 1's TR0 and TF0 bits.
0	M00	

SCON (Serial Port Control Register)

7	6	5	4	3	2	1	0
FE/SM0	SM1	SM2	REN	TB8	RB8	TI	RI

Bit Number	Bit Mnemonic	Description
7	FE	**Framing Error bit (SMOD0=1)** Clear to reset the error state, not cleared by a valid stop bit. Set by hardware when an invalid stop bit is detected. SMOD0 must be set to enable access to the FE bit
	SM0	**Serial port Mode bit 0** Refer to SM1 for serial port mode selection. SMOD0 must be cleared to enable access to the SM0 bit
6	SM1	Serial port Mode bit 1 **SM0 SM1 Mode Description Baud Rate** 0 0 0 Shift Register $F_{CPU\ PERIPH}/6$ 0 1 1 8-bit UART Variable 1 0 2 9-bit UART $F_{CPU\ PERIPH}/32$ or /16 1 1 3 9-bit UART Variable
5	SM2	Serial port Mode 2 bit / Multiprocessor Communication Enable bit Clear to disable multiprocessor communication feature. Set to enable multiprocessor communication feature in mode 2 and 3, and eventually mode 1. This bit should be cleared in mode 0.
4	REN	**Reception Enable bit** Clear to disable serial reception. Set to enable serial reception.
3	TB8	Transmitter Bit 8 / Ninth bit to transmit in modes 2 and 3. o transmit a logic 0 in the 9th bit. Set to transmit a logic 1 in the 9th bit.
2	RB8	**Receiver Bit 8 / Ninth bit received in modes 2 and 3** Cleared by hardware if 9th bit received is a logic 0. Set by hardware if 9th bit received is a logic 1. In mode 1, if SM2 = 0, RB8 is the received stop bit. In mode 0 RB8 is not used.
1	TI	**Transmit Interrupt flag** Clear to acknowledge interrupt. Set by hardware at the end of the 8th bit time in mode 0 or at the beginning of the stop bit in the other modes.
0	RI	**Receive Interrupt flag** Clear to acknowledge interrupt. Set by hardware at the end of the 8th bit time in mode 0, see Figure 2-26. and Figure 2-27. in the other modes.

PCON (Power Mode Control Register)

7	6	5	4	3	2	1	0
SMOD1	SMOD0	-	POF	GF1	GF0	PD	IDL

Bit Number	Bit Mnemonic	Description
7	SMOD1	**Serial port Mode bit 1 for UART** Set to select double baud rate in mode 1, 2 or 3.
6	SMOD0	Serial port Mode bit 0 for UART Cleared to select SM0 bit in SCON register. Set to select FE bit in SCON register.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	POF	**Power-Off Flag** Cleared to recognize next reset type. Set by hardware when VCC rises from 0 to its nominal voltage. Can also be set by software.
3	GF1	**General purpose Flag** Cleared by user for general purpose usage. Set by user for general purpose usage.
2	GF0	**General purpose Flag** Cleared by user for general purpose usage. Set by user for general purpose usage.
1	PD	**Power-Down mode bit** Cleared by hardware when reset occurs. Set to enter power-down mode.
0	IDL	**Idle mode bit** Cleared by hardware when interrupt or reset occurs. Set to enter idle mode.

Interrupts

- An interrupt is a special feature which Allows the 8051 to provide the illusion of "multitasking," although in reality the 8051 is only doing one thing at a time. The word "interrupt" can often be substituted with the word "event."

- An interrupt is triggered whenever corresponding event occurs. When the event occurs, the 8051 temporarily puts "on hold" the normal execution of the program and executes a special section of code referred to as an interrupt handler.

- Whenever any device needs its service, the device notifies the microcontroller by sending it an interrupt signal.

- There are total 5 interrupt sources in 8051 Microprocessor as follows.

  (1). Timer Flag 0, (2). Timer Flag 1, (TF1 & TF2 are Timer Flag Interrupts).

  (3). INT 0, (4). INT 1, (INT 0 & INT 1 are external interrupts).

  (5). Serial Port Interrupt (RI or TI).

Interrupts Priorities

When the 8051 is powered up, the priorities are assigned according to the following

- In reality, the priority scheme is nothing but an internal polling sequence in which the 8051 polls the interrupts in the sequence listed and responds accordingly

Interrupt Priority Upon Reset

Highest To Lowest Priority	
External Interrupt 0	(INT0)
Timer Interrupt 0	(TF0)
External Interrupt 1	(INT1)
Timer Interrupt 1	(TF1)
Serial Communication	(RI + TI)

Interrupt Destinations

	Interrupt	Address (Hex)
1	IE0	0003H
2	TF0	000BH
3	IE1	0013H
4	TF1	001BH
5	SERIAL	0023H

Interrupt Priority (IP) SFR

Interrupt Priority Register (Bit-addressable)

D7							D0
--	--	PT2	PS	PT1	PX1	PT0	PX0

--	IP.7	Reserved
--	IP.6	Reserved
PT2	IP.5	Timer 2 interrupt priority bit (8052 only)
PS	IP.4	Serial port interrupt priority bit
PT1	IP.3	Timer 1 interrupt priority bit
PX1	IP.2	External interrupt 1 priority bit
PT0	IP.1	Timer 0 interrupt priority bit
PX0	IP.0	External interrupt 0 priority bit

Priority bit=1 assigns high priority

Priority bit=0 assigns low priority

Interrupt Enable (IE) SFR

IE (Interrupt Enable) Register

D7							D0
EA	--	ET2	ES	ET1	EX1	ET0	EX0

EA (enable all) must be set to 1 in order for rest of the register to take effect

EA	IE.7	Disables all interrupts
--	IE.6	Not implemented, reserved for future use
ET2	IE.5	Enables or disables timer 2 overflow or capture interrupt (8952)
ES	IE.4	Enables or disables the serial port interrupt
ET1	IE.3	Enables or disables timer 1 overflow interrupt
EX1	IE.2	Enables or disables external interrupt 1
ET0	IE.1	Enables or disables timer 0 overflow interrupt
EX0	IE.0	Enables or disables external interrupt 0

END OF SESSION