A 16Gb 27Gb/s/pin T-coil based GDDR6 DRAM with Merged-MUX TX, Optimized WCK Operation, and Alternative-Data-Bus

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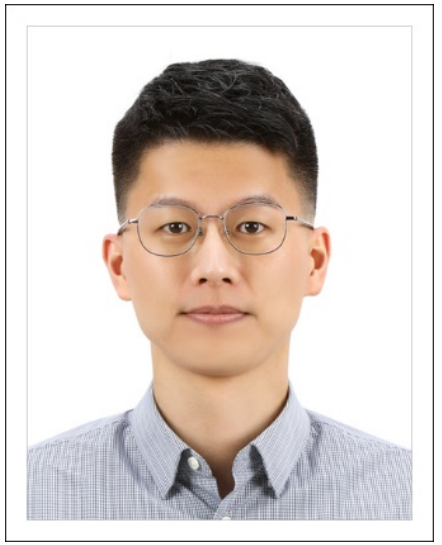
Samsung Electronics, Korea

Self Introduction

- **First author (speaker): Daewoong Lee**
- **Education**
  - B.S. in EE from KAIST, Korea in 2013
  - M.S. in EE from KAIST, Korea in 2015
  - Ph.D. in EE from KAIST, Korea in 2019
- **Working at Samsung Electronics (2019.09 ~)**
- **Interest**
  - High-speed wireline interfaces
  - High-performance DRAM



Outline

- **Introduction of GDDR6**
- **Key schemes**
  - T-coil based GDDR6
  - Merged-MUX transmitter
  - WCK optimization
  - ZQ calibration
  - Alternative data bus
- **Implementation and measurements**
- **Conclusion**

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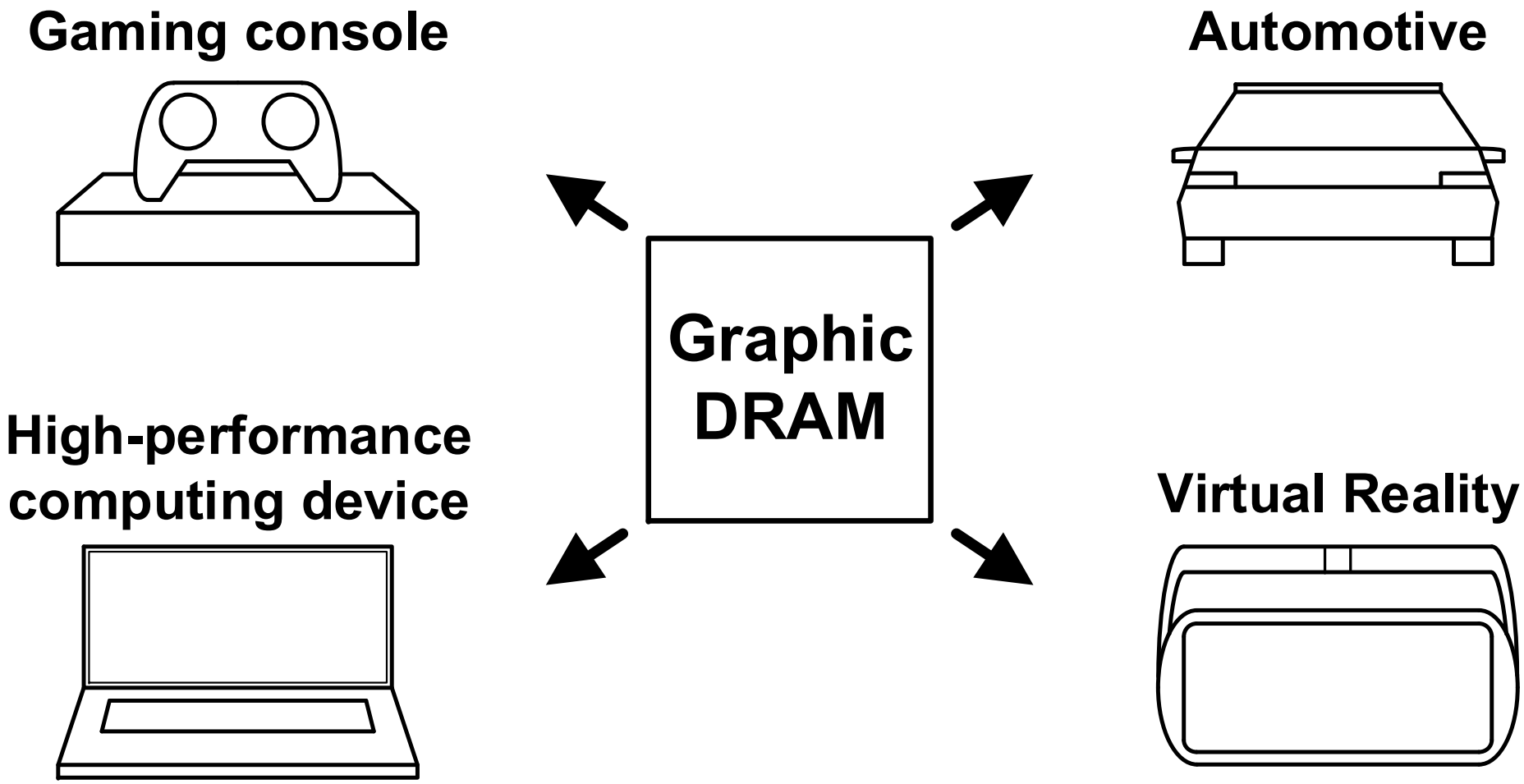
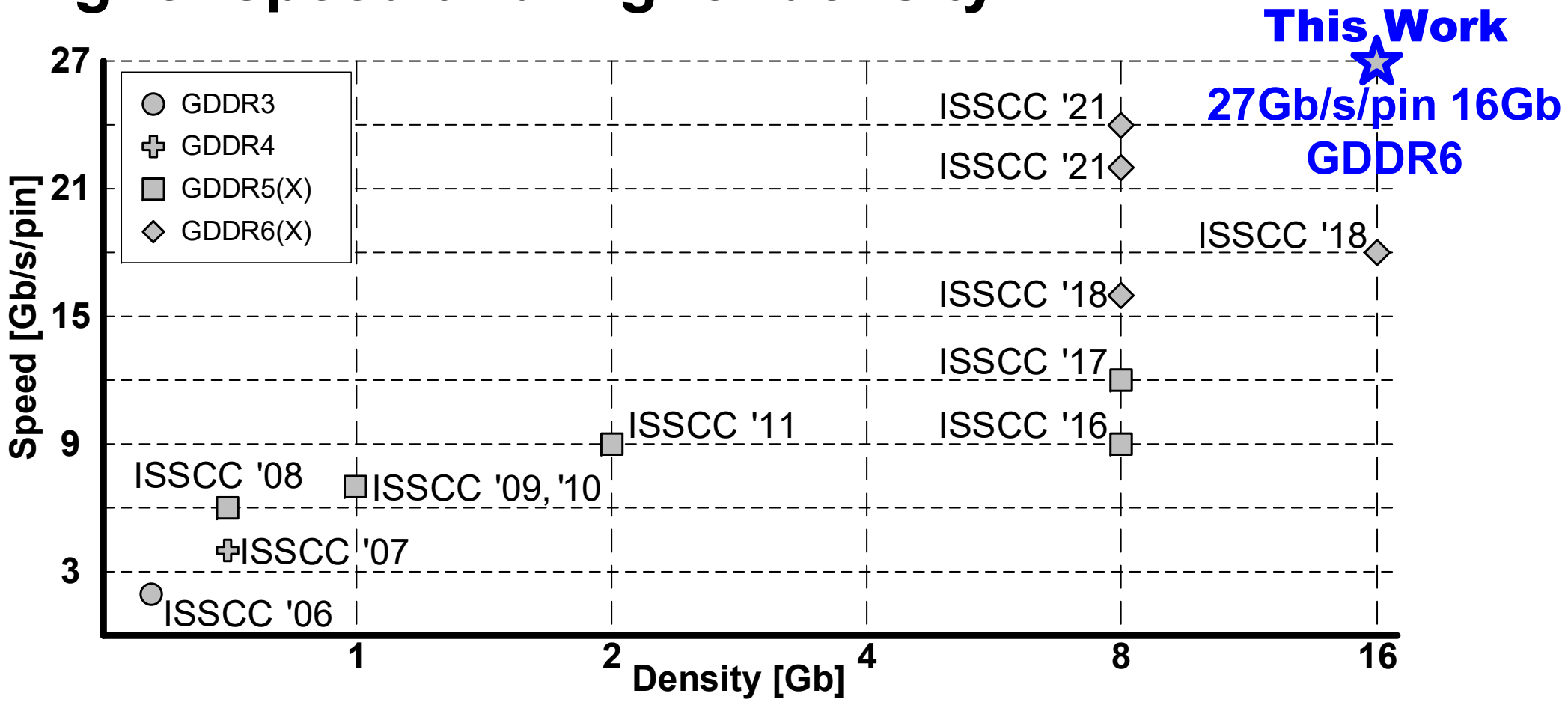
GDDR application

- Higher speed and higher density



GDDR trend

- **Higher speed and higher density**



➔ **Achieves 27Gb/s/pin by improving IO & data bus (How?)**

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Key schemes

- **T-coil based GDDR6**
  - T-coil design in DRAM process
- **Merged-MUX transmitter**
  - Improve ISI & PSIJ
- **WCK optimization**
  - Quad-skew adjustment & wide freq. operation
- **ZQ calibration**
  - T-coil impact consideration
- **Alternative data bus**
  - Increase data window of G-BUS by x2

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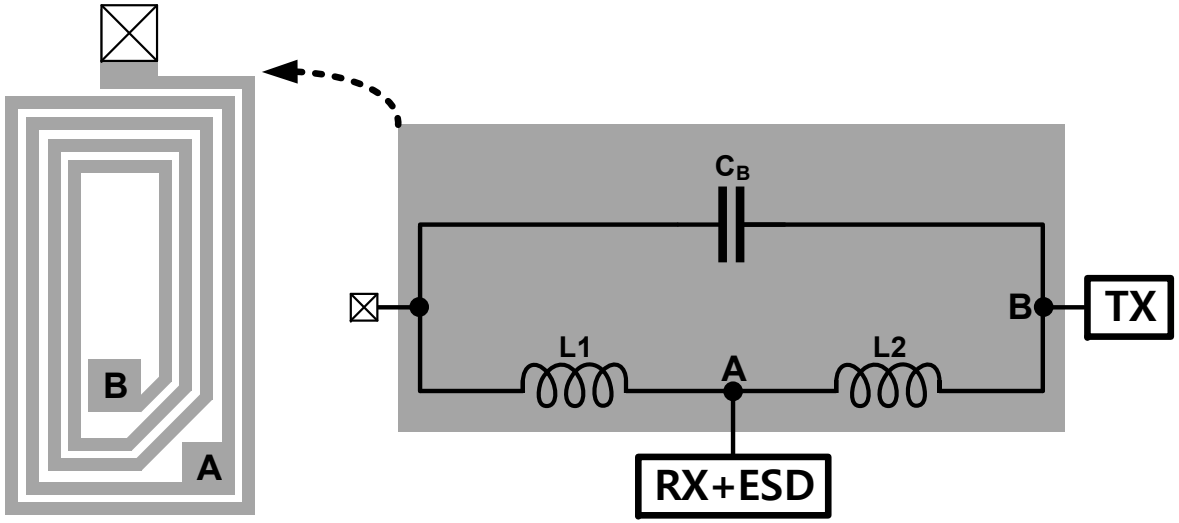
T-coil based GDDR6

*Rs: Sheet resistance

**RDL: Redistribution layer

- **T-coil enhances I/O BW consuming no power**
  - Only a few metal layers in DRAM process
    - *Rs of **RDL: 0.1 X Rs of nearest lower layer

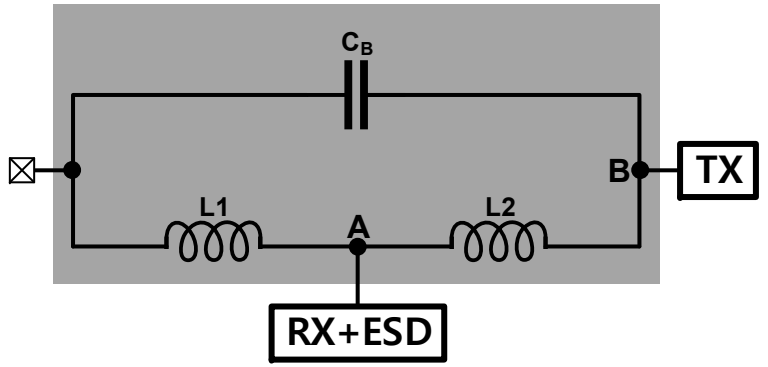
- **T-coil design: RDL based T-coil layer (single layer)**
  - Optimum thickness & width for T-coil design are supported



T-coil based GDDR6

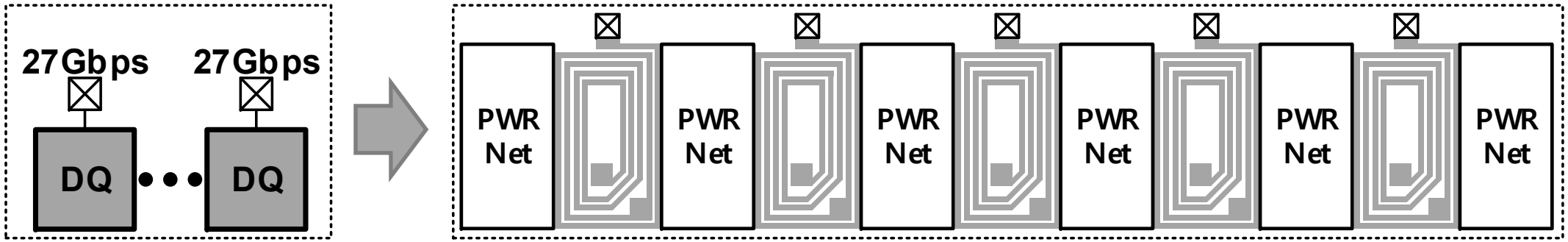
■ To improve BW of both RX and TX

- Considering C_{TX}, C_{ESD}+C_{RX}
  - Inductance (RDL length): L1 < L2
    → Asymmetric T-coil



■ Area efficient T-coil design

- Rectangular aspect ratio, rather than square for power net



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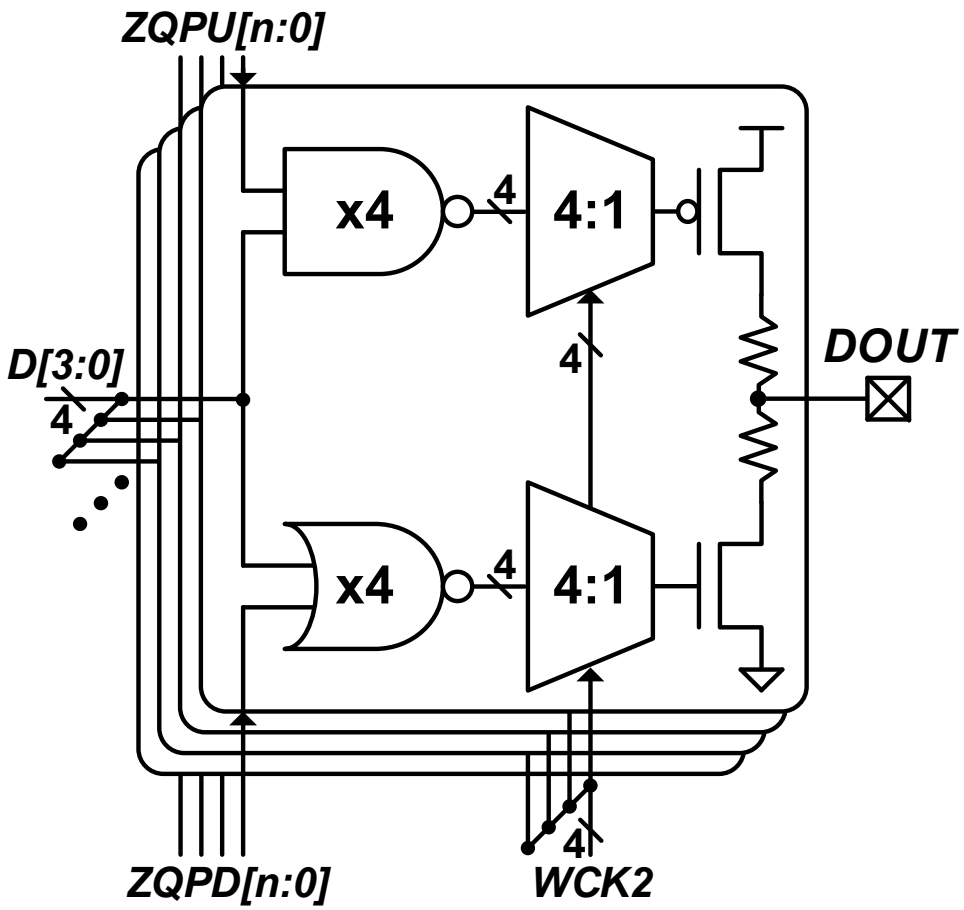
ZQ-coded transmitter [ISSCC'18]

- **Full-rate path: 2 stages (4:1+Out drv.)**

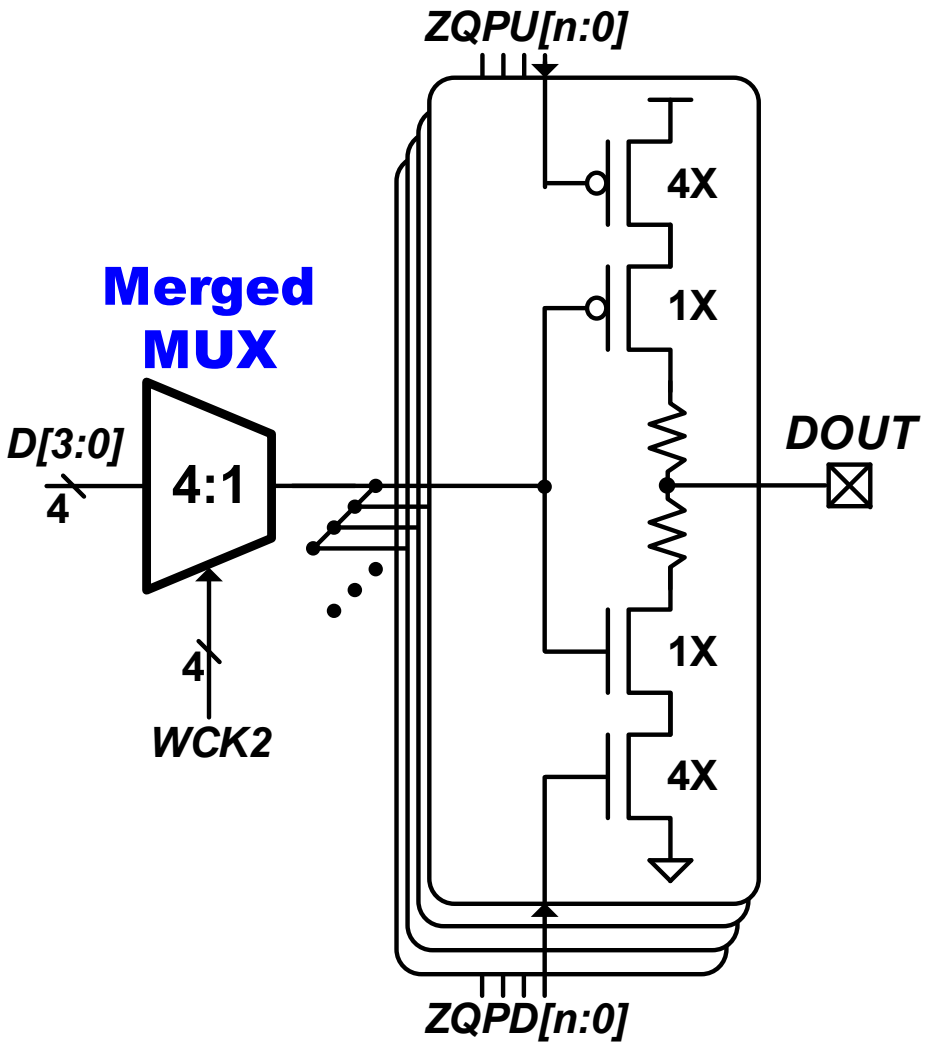
➔ ISI & PSIJ improvement ☺



- **Scattered 4:1 MUXs**
  - ✓ *WCK2* metal loading ☹
- **Skew among multiple 4:1 MUXs**
  - ✓ Degraded SI of *DOUT* ☹
- **ZQ code logic gates (NOR/NAND)**
  - ✓ Power & area ☹

Proposed Merged-MUX transmitter

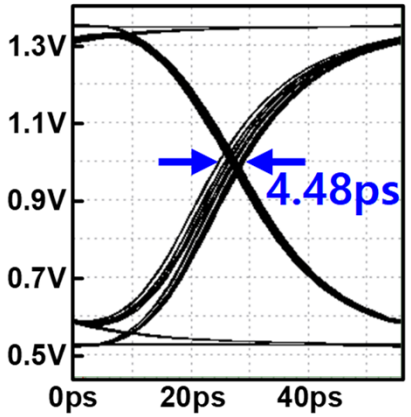
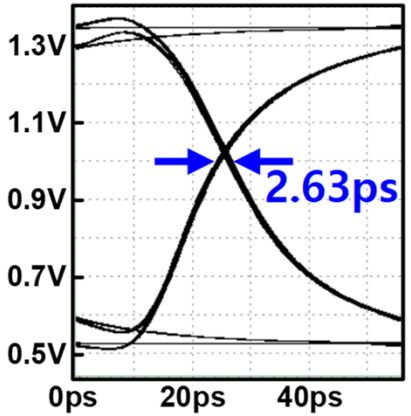
■ Full-rate path: 2 stages (4:1+Out drv.)



- **Merged 4:1 MUX**
  - ✓ *WCK2* metal loading ☺
- **No skew by merged 4:1 MUX**
  - ✓ Improved SI of *DOUT* ☺
- **No ZQ code logic gate**
  - ✓ Power & area ☺

Transmitter comparison

- **Better performance on Merged-MUX transmitter**

	DOUT	Power	Area
Previous ZQ-coded Transmitter		X1	X1
Proposed Merged-MUX Transmitter		X0.71	X0.6

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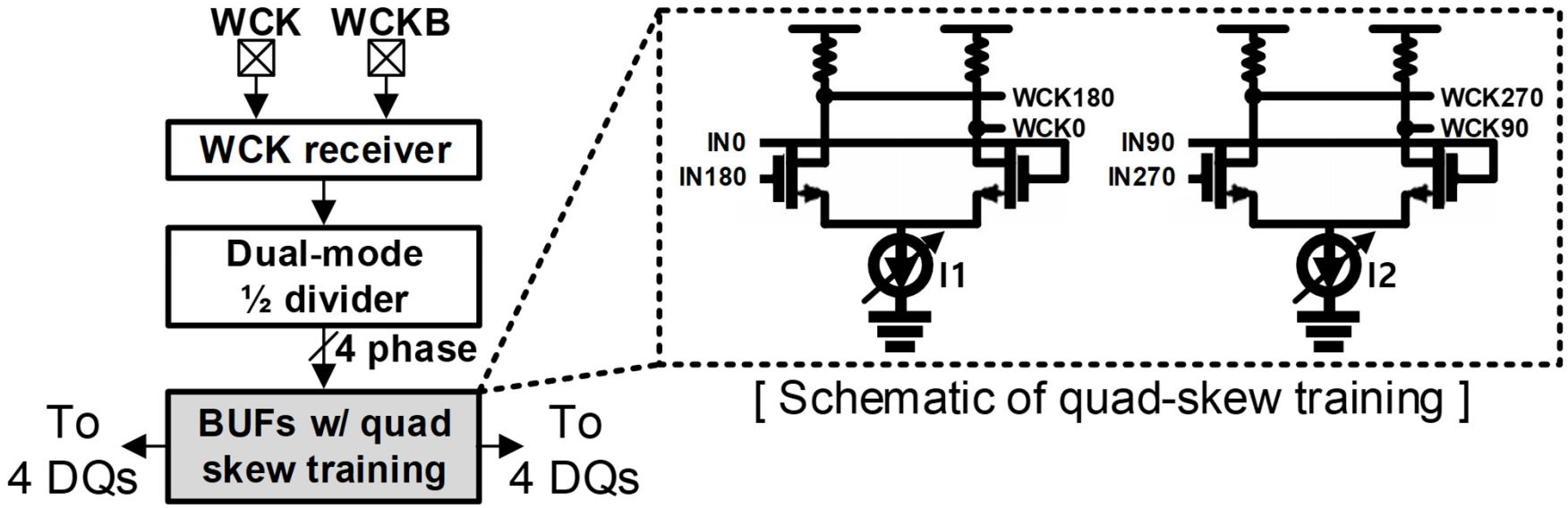
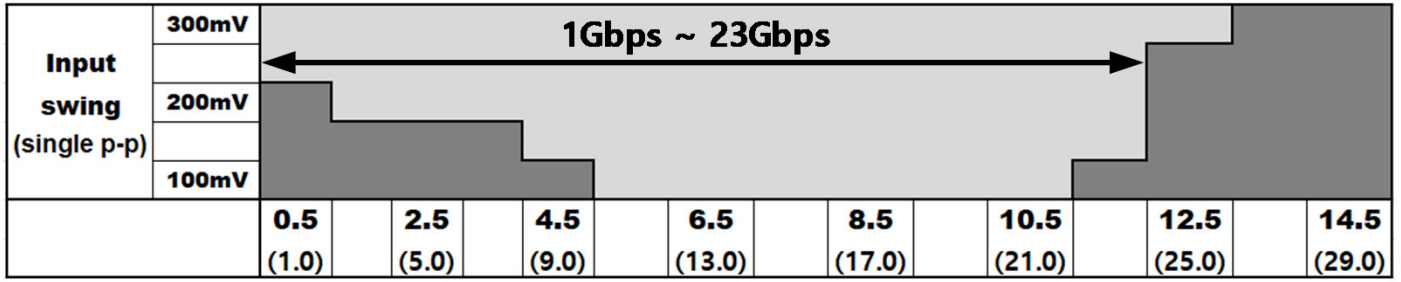
Quad-skew training

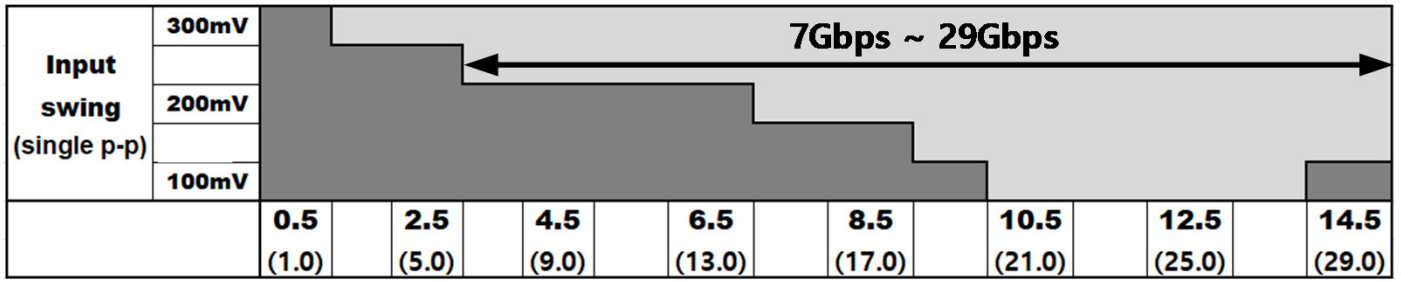
Controllable max T_{qskew} : 3ps (8.1% of 1UI for 27Gbps)



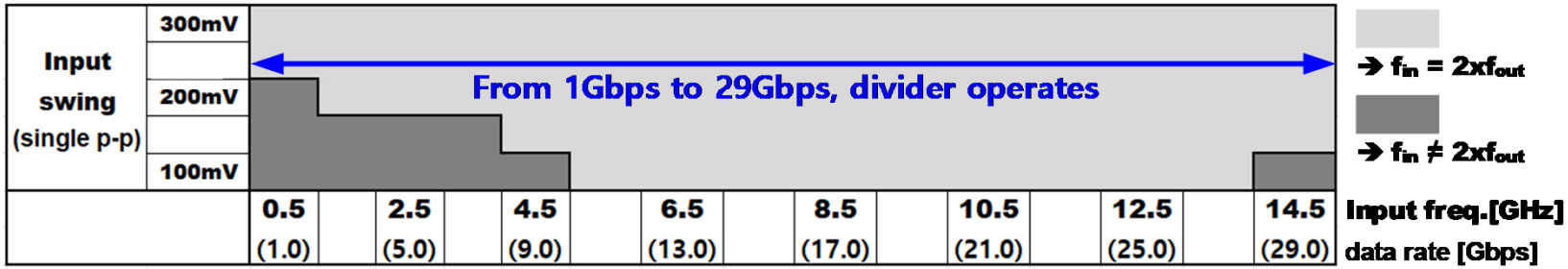
Dual-mode frequency divider



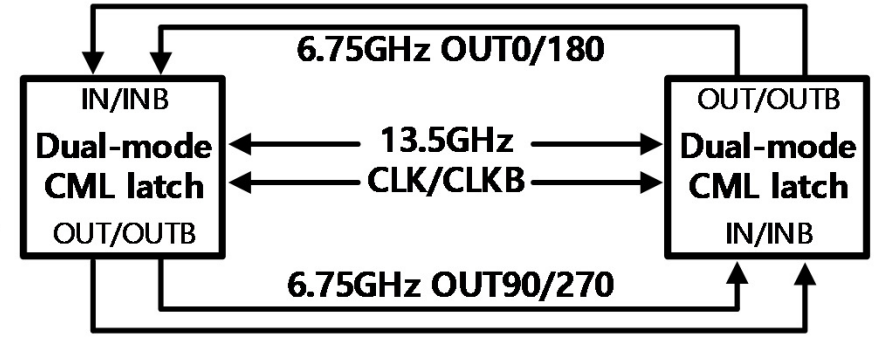
< LF mode >



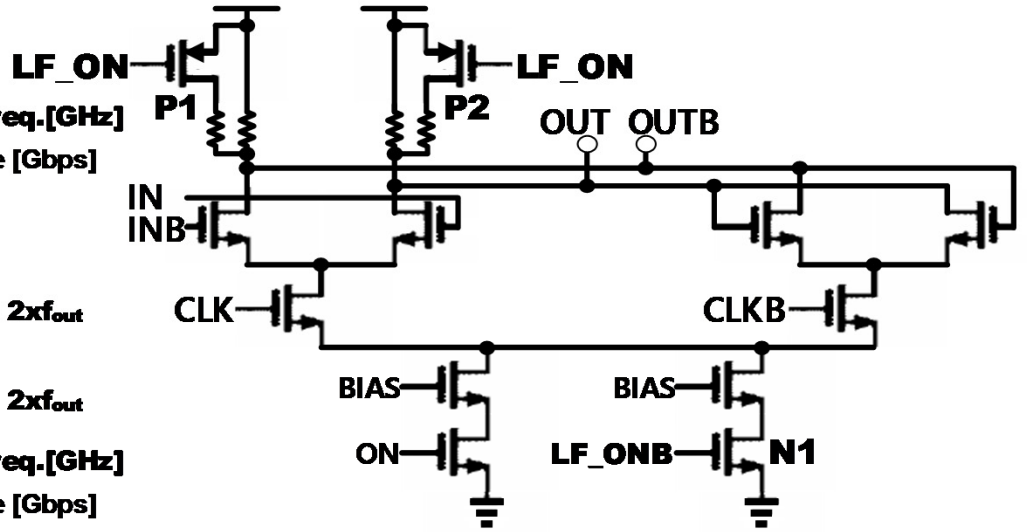
< HF mode >



< Effective freq. range (LF mode + HF mode) >



< Dual-mode frequency divider >



< Dual-mode CML latch >

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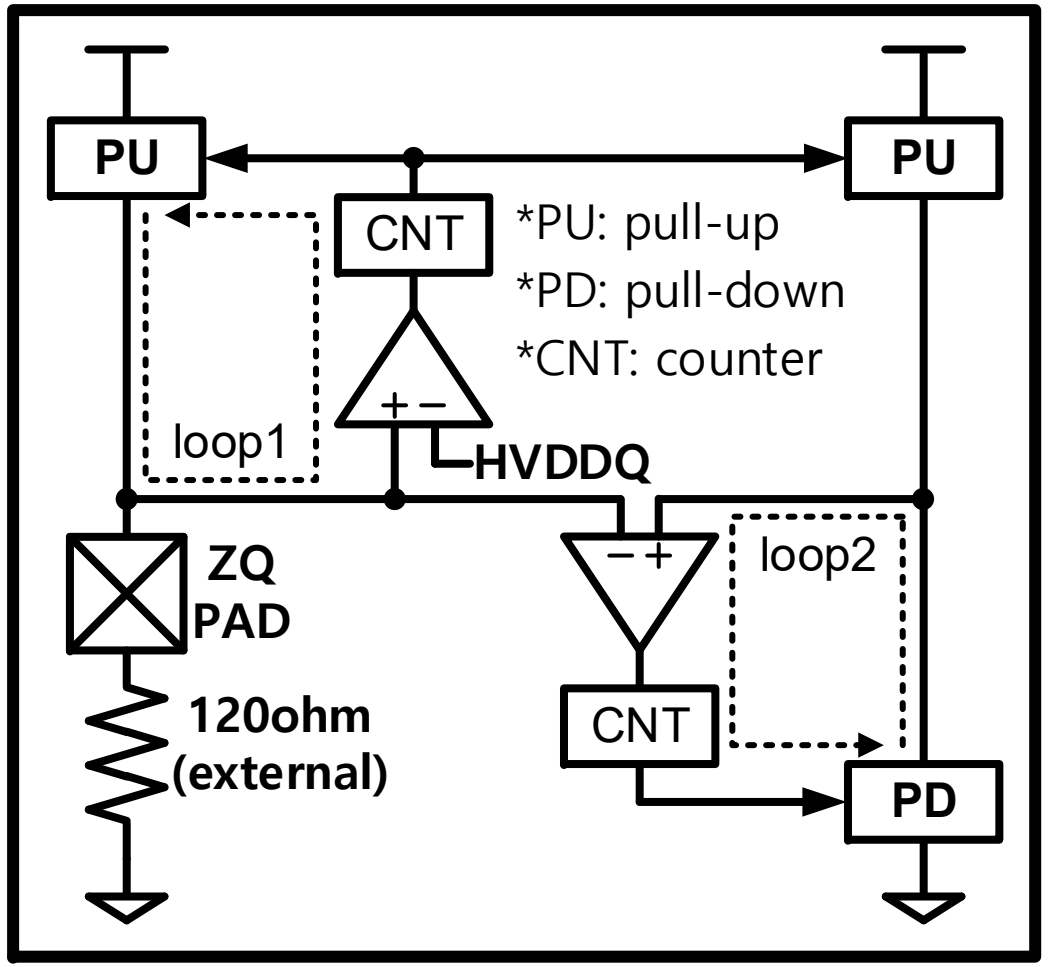
ZQ calibration

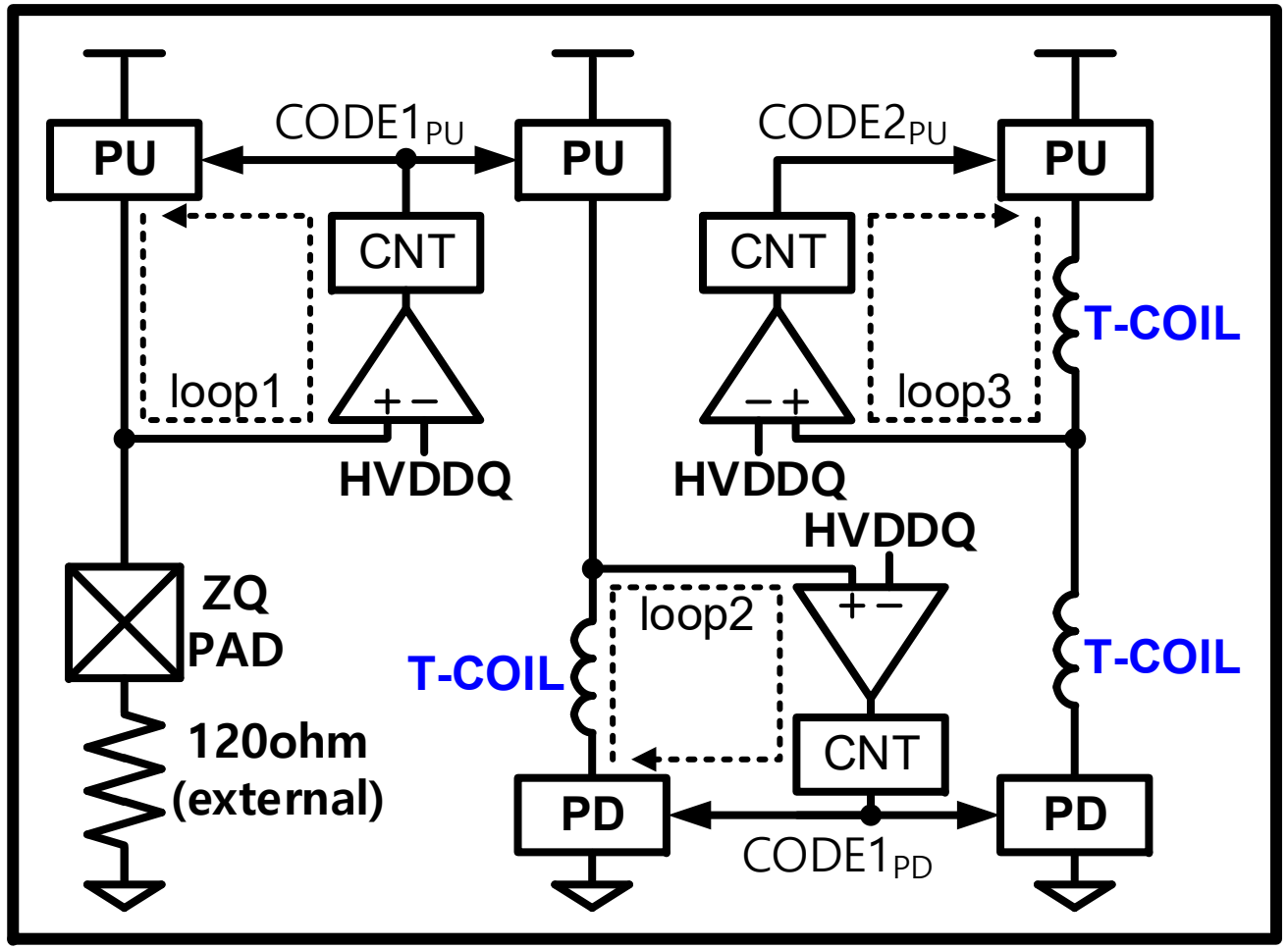
■ Conventional



- **Loop1**
  - ✓ Obtain pull-up codes
- **Loop2**
  - ✓ Obtain pull-down codes

ZQ calibration considering T-coil

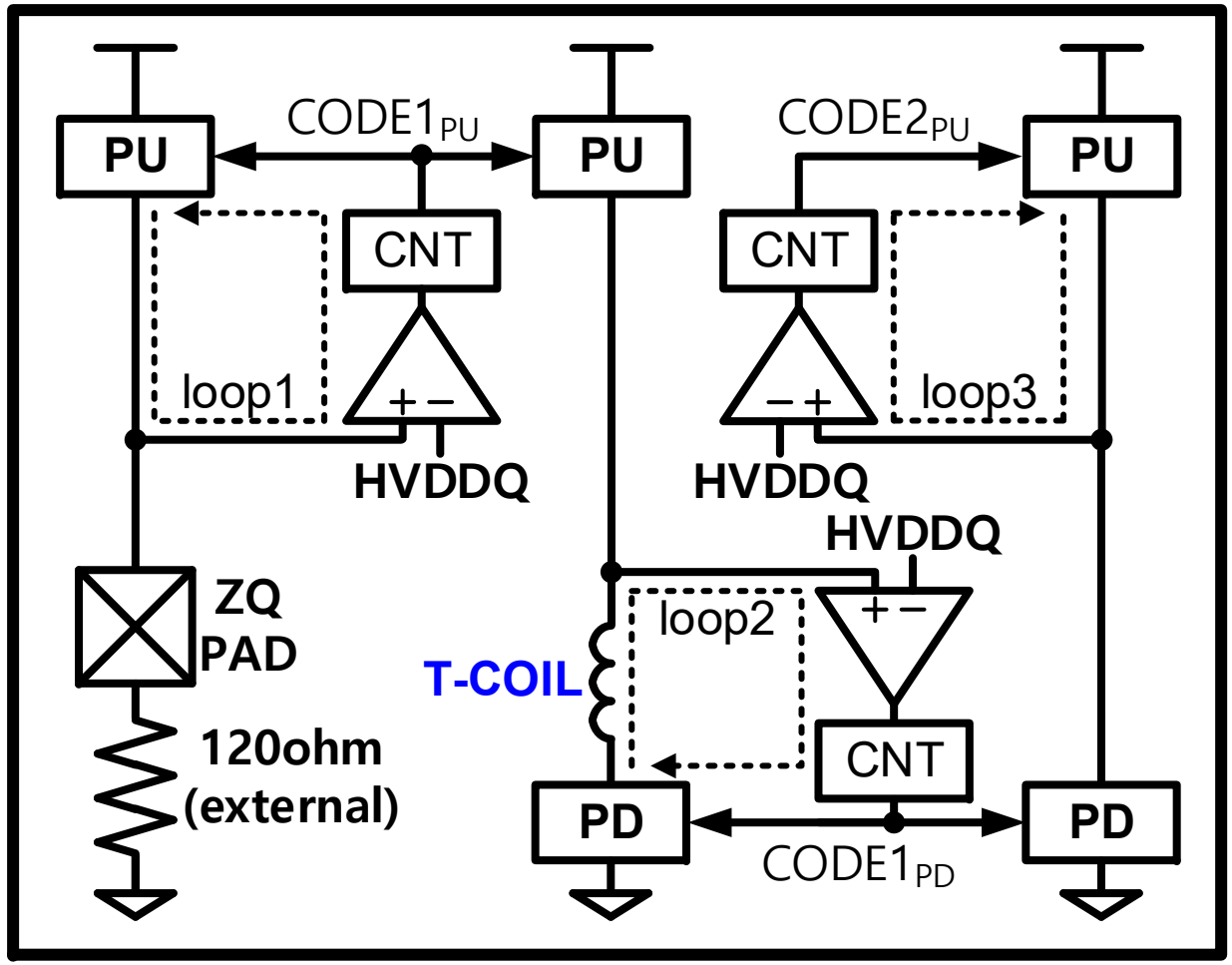
Three T-coils in calibration



- **Loop1**
  - ✓ Obtain pull-up codes
- **Loop2**
  - ✓ Obtain pull-down codes considering T-coil
- **Loop3**
  - ✓ Obtain pull-up codes considering T-coil

ZQ calibration considering T-coil

- **Proposed (One T-coil in cal.): area reduction**



- **Loop1**
  - ✓ Obtain pull-up codes
- **Loop2**
  - ✓ Obtain pull-down codes considering T-coil
- **Loop3**
  - ✓ Obtain pull-up codes considering T-coil

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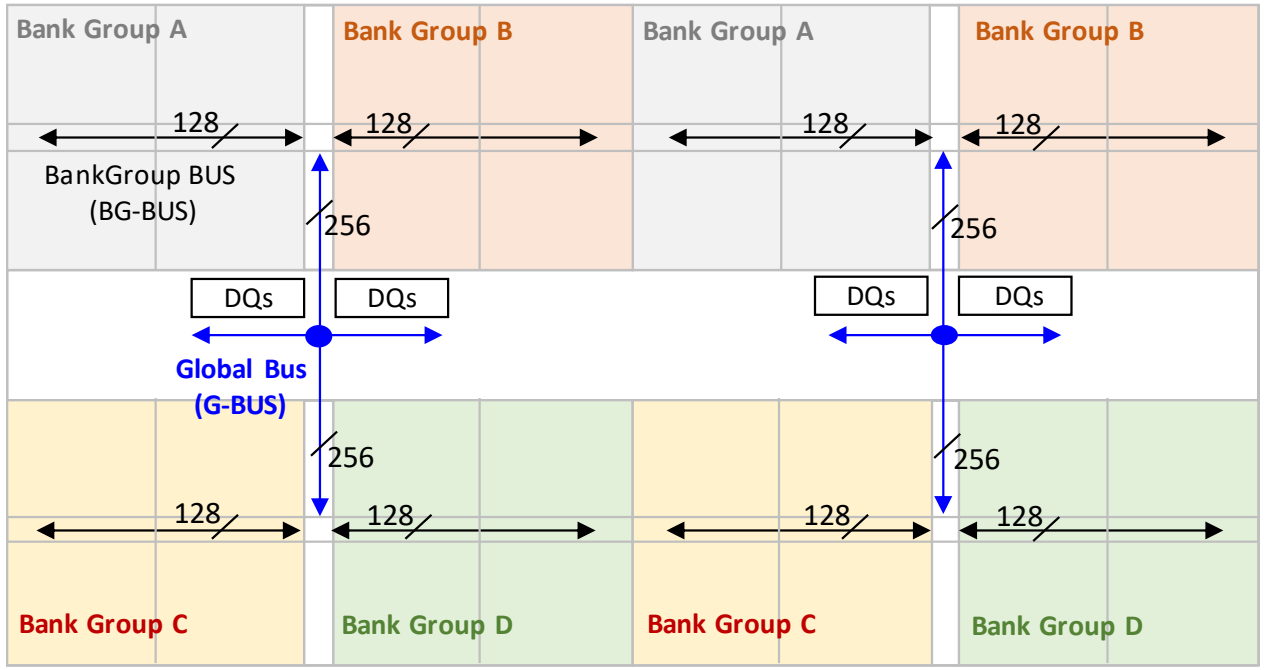
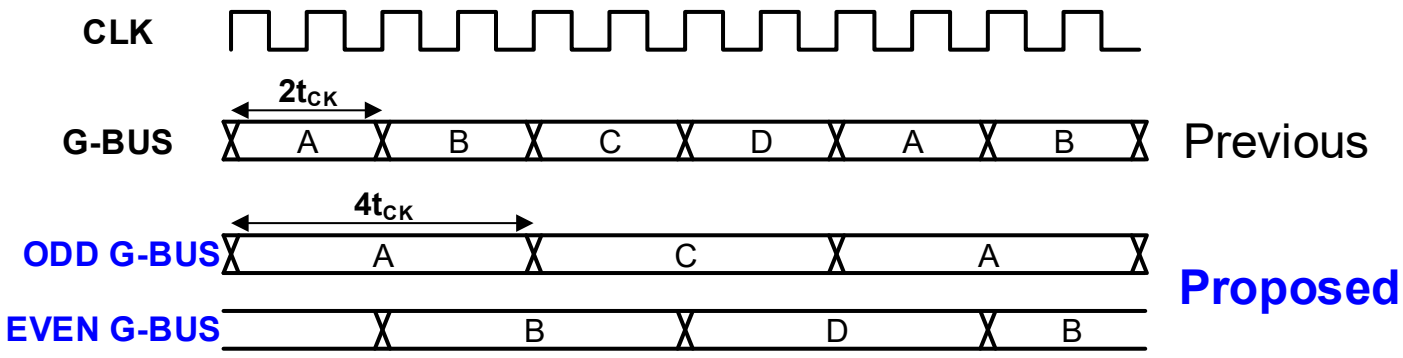
Alternative data bus





- **G-bus: frequency limit**
- **Two G-BUSes**
  - ✓ EVEN&ODD
- **Increase data window of G-BUS by 2x**
  - ✓ Achieve high BW (27Gbps)

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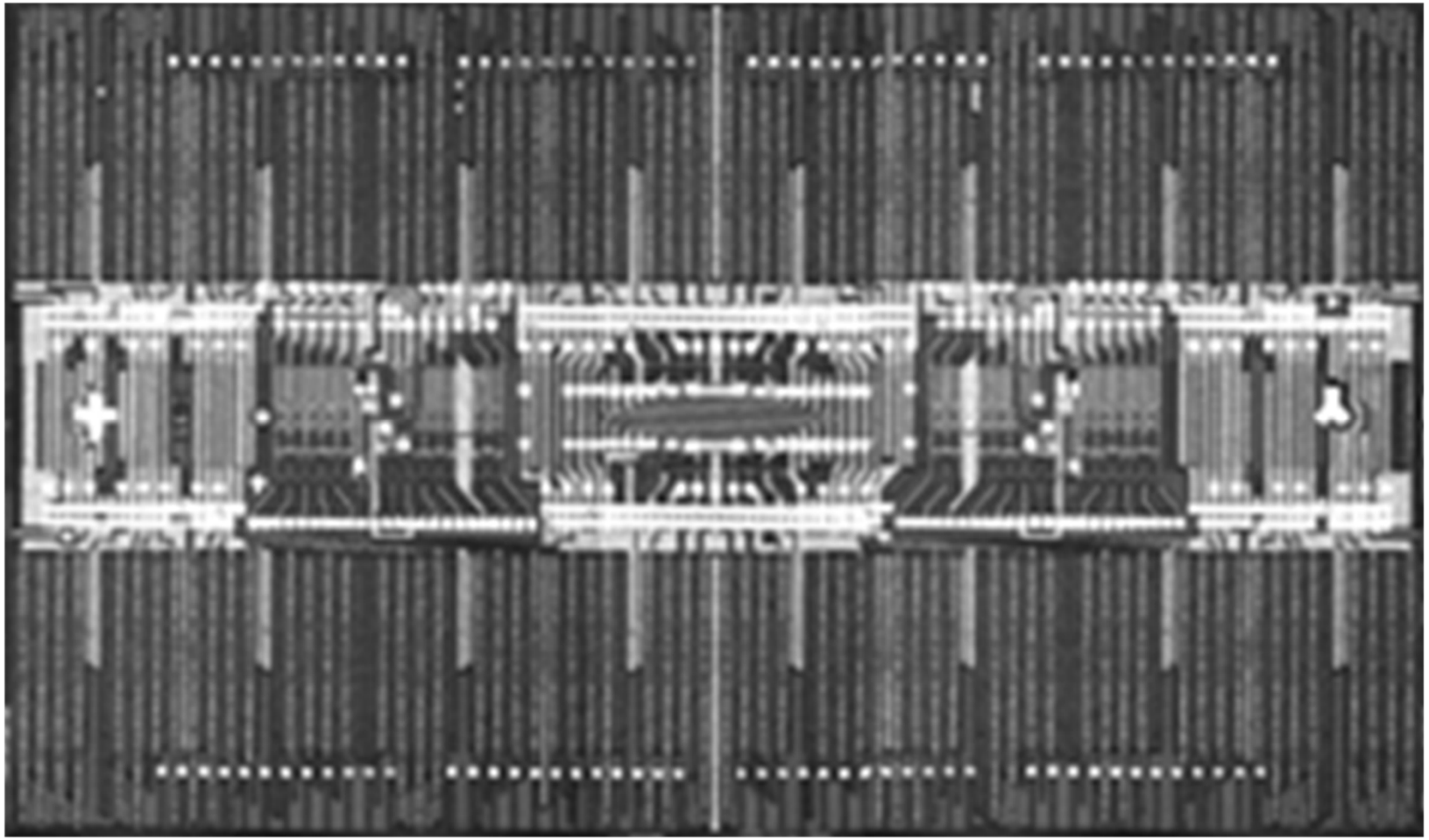
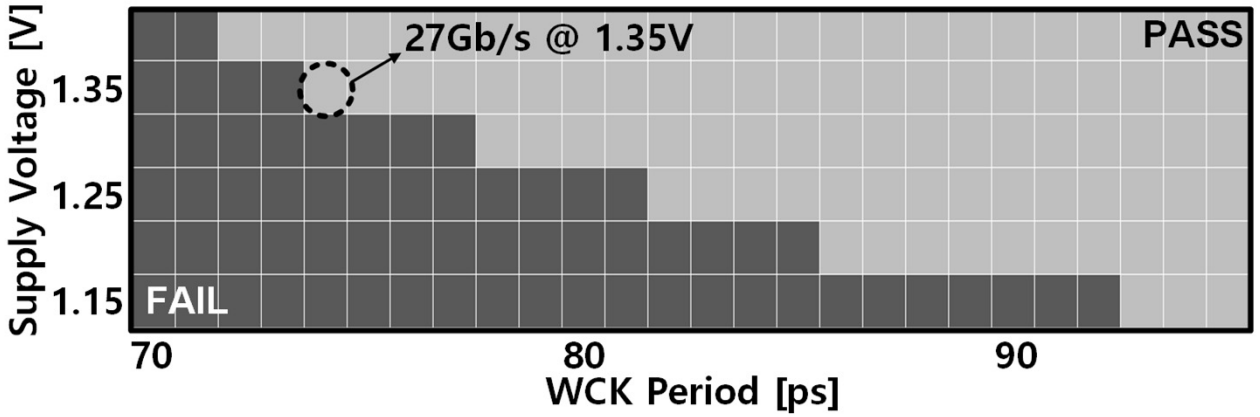
Chip implementation

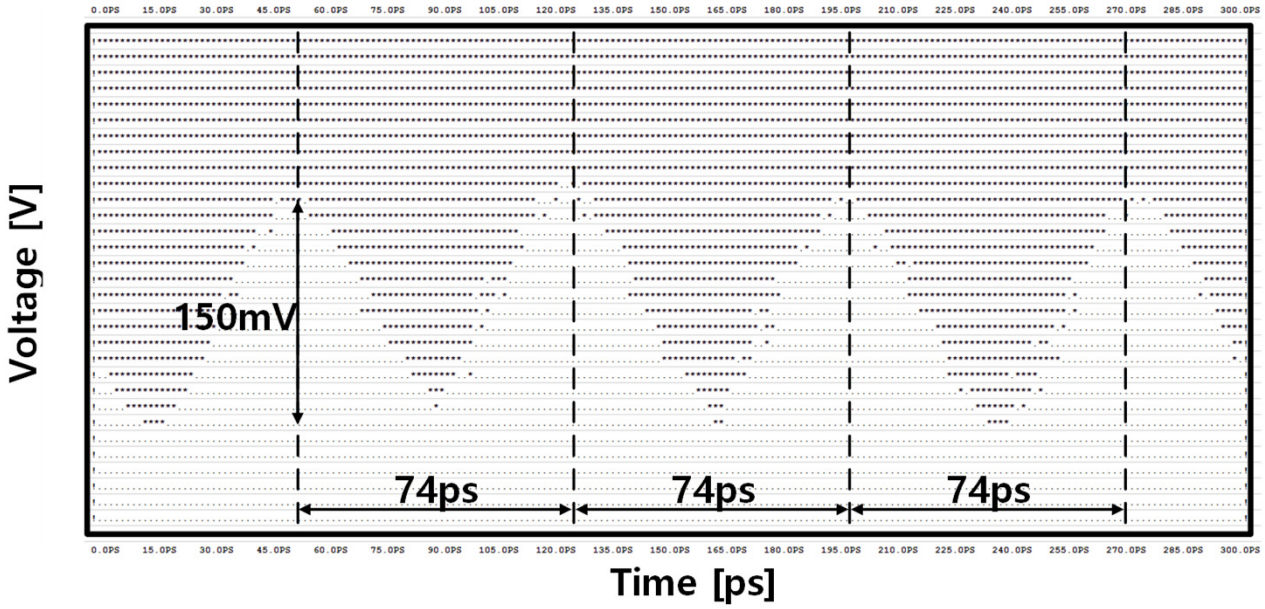


27Gb/s/pin
1z nm CMOS
Supply voltage: 1.35V
16 Bank/1-CH
8 Gb/1-CH
X16 IO/1-CH
36.3mm^2/1-CH

Measurements



- **Frequency-voltage shmoo**
  - ✓ 27Gb/s @ 1.35V



- **Error detection code (EDC) pin**
  - ✓ 27Gb/s (1UI=37ps)
  - ✓ 0101 pattern, 1.35V

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Conclusion

- **27Gb/s/pin 16Gb GDDR6 DRAM is implemented**

- **I/O Bandwidth improvement**
  - T-coil for the first time in DRAM process
  - Merged-MUX transmitter
  - Quad-skew training & dual-mode divider

- **Alternative data bus**
  - Increase data window of G-BUS by x2