

## Práctica 6: Algebra de Boole

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No. de lista: 3

a)

### Reducción con Algebra de Boole

$$\begin{aligned}
 a) & (X \cdot \bar{Z} + \bar{Y} \cdot \bar{Z}) + (X \cdot Z + \bar{Y} \cdot Z) = X + \bar{Y} \\
 & (\bar{Z}(X + \bar{Y})) + (Z(X + \bar{Y})) = X + \bar{Y} \quad \textcircled{5} X \cdot (Y + Z) = (X \cdot Y) + (X \cdot Z) \\
 & (X + \bar{Y}) \cdot (\bar{Z} + Z) = X + \bar{Y} \quad \textcircled{5} X \cdot (Y + Z) = (X \cdot Y) + (X \cdot Z) \\
 & (X + \bar{Y}) \cdot 1 = X + \bar{Y} \quad \textcircled{8} X + \bar{X} = 1 \\
 & \underline{X + \bar{Y} = X + \bar{Y}} \quad \textcircled{3} X \cdot 1 = X
 \end{aligned}$$

### Tablas de verdad

$$X \cdot \bar{Z} + \bar{Y} \cdot \bar{Z} + X \cdot Z + \bar{Y} \cdot Z$$

X	Y	Z	$\bar{Y}$	$\bar{Z}$	$X \cdot \bar{Z}$	$\bar{Y} \cdot \bar{Z}$	$X \cdot Z$	$\bar{Y} \cdot Z$	$(X \cdot \bar{Z}) + (\bar{Y} \cdot \bar{Z})$	$(X \cdot Z) + (\bar{Y} \cdot Z)$	$((X \cdot \bar{Z}) + (\bar{Y} \cdot \bar{Z})) + (X \cdot Z)$	$((X \cdot \bar{Z}) + (\bar{Y} \cdot \bar{Z})) + (X \cdot Z)$
0	0	0	1	1	0	1	0	0	1	0	1	1
0	0	1	1	0	0	0	0	1	0	1	1	1
0	1	0	0	1	0	0	0	0	0	0	0	0
0	1	1	0	0	0	0	0	0	0	0	0	0
1	0	0	1	1	1	1	0	0	1	1	1	1
1	0	1	1	0	0	0	1	1	0	1	1	1
1	1	0	0	1	1	0	0	0	1	1	1	1
1	1	1	0	0	0	0	1	0	0	1	1	1

$$X + \bar{Y}$$

X	Y	$\bar{Y}$	$X + \bar{Y}$
0	0	1	1
0	1	0	0
1	0	1	1
1	1	0	1

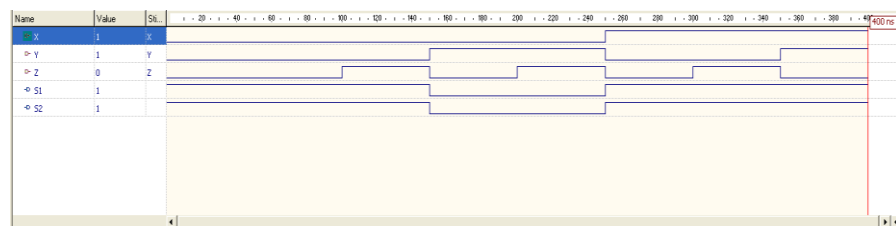
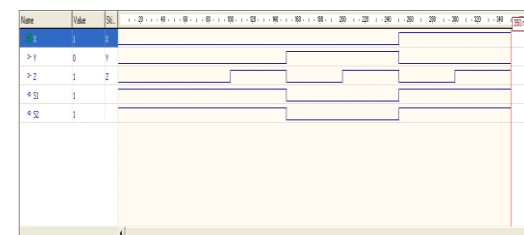
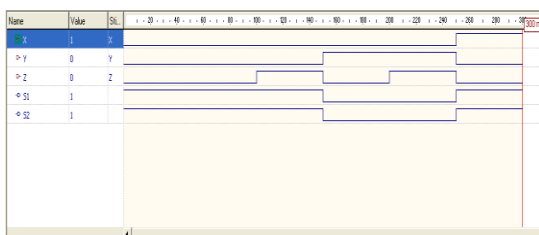
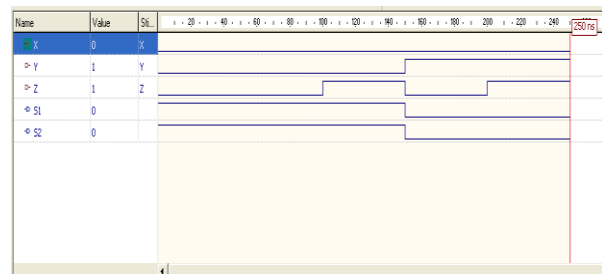
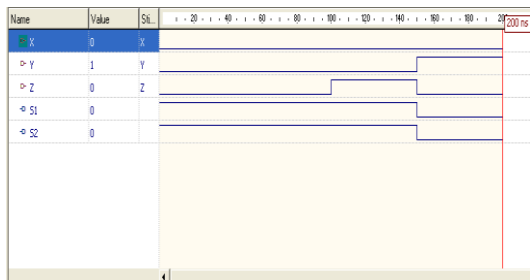
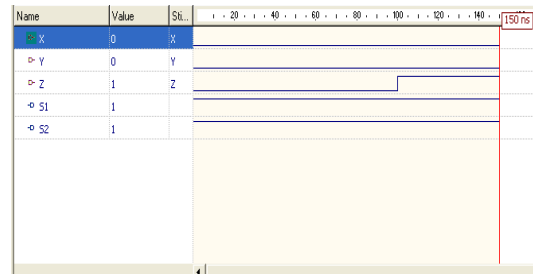
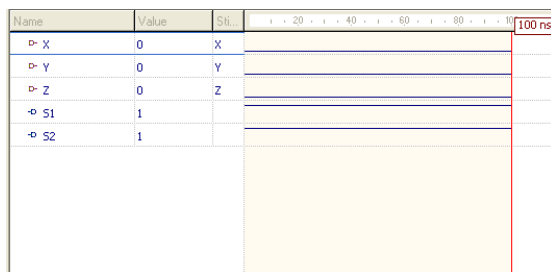
## Código VHDL

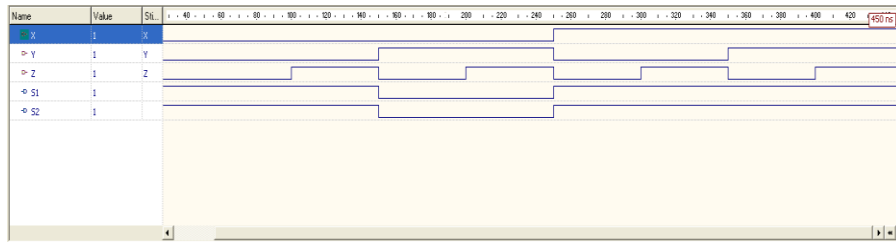
```

1 library ieee;
2 use ieee.std_logic_1164.all;
3 entity expresiona is
4 port(
5     X, Y, Z :in std_logic;
6     S1, S2:out std_logic
7 );
8 end expresiona;
9 architecture Aexpresiona of expresiona is
10 begin
11     S1 <= (X AND (NOT Z)) OR ((NOT Y) AND (NOT Z)) OR (X AND Z) OR ((NOT Y) AND Z);
12     S2 <= X OR (NOT Y);
13 end Aexpresiona;

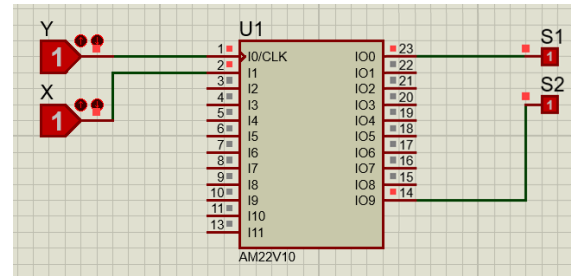
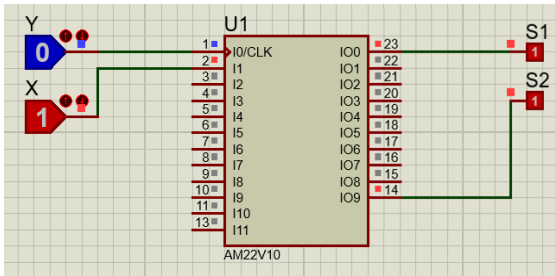
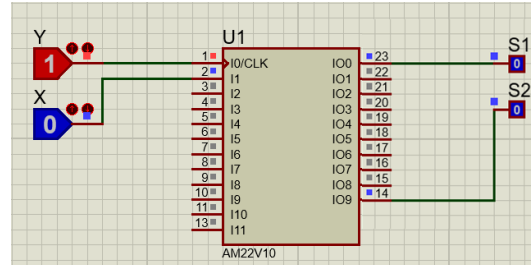
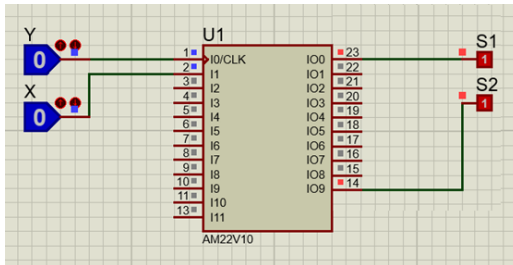
```

## Simulacion de Galaxy





## Simulación en Proteus



b)

## Reducción con Algebra de Boole

$$\begin{aligned}
 b) \quad & \overline{(\overline{X \cdot Y} + Z)} = \overline{X \cdot \bar{Z}} + Y \cdot \bar{Z} \\
 & \overline{(\overline{X \cdot Y} \cdot \bar{Z})} = \overline{X \cdot \bar{Z}} + Y \cdot \bar{Z} \\
 & \overline{(\overline{X + Y} \cdot \bar{Z})} = \overline{X \cdot \bar{Z}} + Y \cdot \bar{Z} \\
 & \overline{(\overline{X + Y} \cdot \bar{Z})} = \overline{X \cdot \bar{Z}} + Y \cdot \bar{Z} \\
 & \underline{\overline{(\overline{X \cdot \bar{Z}})} + (Y \cdot \bar{Z}) = (\overline{X \cdot \bar{Z}}) + Y \cdot \bar{Z}}
 \end{aligned}$$

$$\begin{aligned}
 \textcircled{10} \quad & \overline{X + Y} = \overline{X} \cdot \overline{Y} \\
 \textcircled{11} \quad & \overline{X \cdot Y} = \overline{X} + \overline{Y} \\
 & \text{Doble negación} \\
 \textcircled{12} \quad & X \cdot (Y + Z) = (X \cdot Y) + (X \cdot Z)
 \end{aligned}$$

## Tablas de verdad

$$(x \cdot \bar{y} + z)$$

$$\bar{x} \cdot \bar{z} + y \cdot \bar{z}$$

$x$	$y$	$z$	$\bar{y}$	$x \cdot \bar{y}$	$(x \cdot \bar{y}) + z$	$\overline{(x \cdot \bar{y}) + z}$
0	0	0	1	0	0	1
0	0	1	1	0	1	0
0	1	0	0	0	0	1
0	1	1	0	0	1	0
1	0	0	1	1	1	0
1	0	1	1	1	1	0
1	1	0	0	0	0	1
1	1	1	0	0	1	0

$X$	$Y$	$Z$	$\bar{X}$	$\bar{Z}$	$\bar{X} \cdot \bar{Z}$	$Y \cdot \bar{Z}$	$(\bar{X} \cdot \bar{Z}) + (Y \cdot \bar{Z})$
0	0	0	1	1	1	0	1
0	0	1	1	0	0	0	0
0	1	0	1	1	1	1	1
0	1	1	1	0	0	0	0
1	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0
1	1	0	0	1	0	1	1
1	1	1	0	0	0	0	0

## Código VHDL

```

1 library ieee;
2 use ieee.std_logic_1164.all;
3 entity expresionb is
4 port(
5     X,Y,Z:in std_logic;
6     S1,S2:out std_logic
7 );
8 end expresionb;
9 architecture Aexpresionb of expresionb is
10 begin
11     S1 <= NOT((X AND (NOT Y)) OR Z);
12     S2 <= ((NOT X) AND (NOT Z)) OR (Y AND (NOT Z));
13 end Aexpresionb;

```

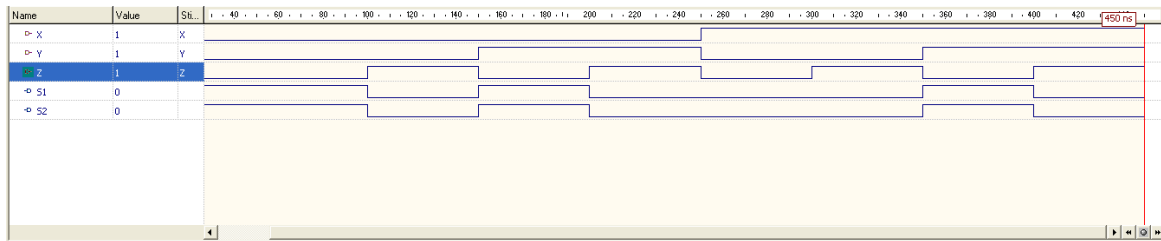
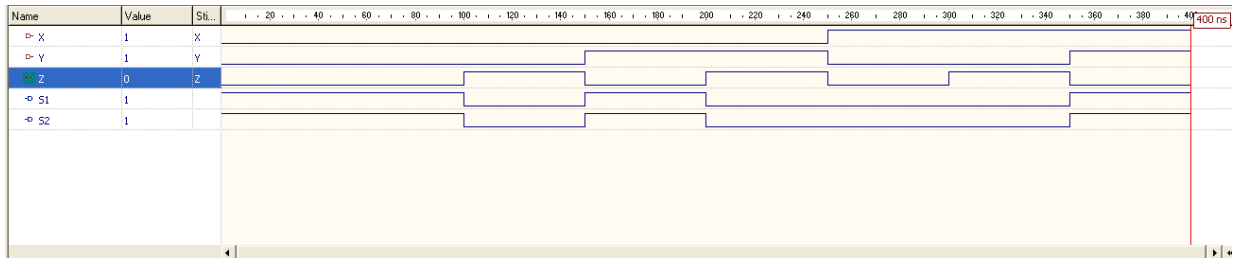
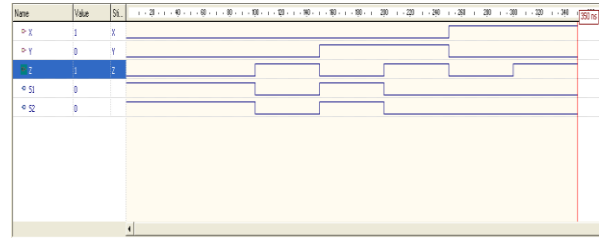
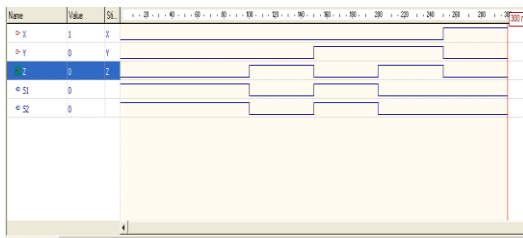
## Simulación en Galaxy

Name	Value	Sti...	. . . 20 . . . 40 . . . 60 . . . 80 . . . 100 ns
-> X	0	X	
-> Y	0	Y	
<- Z	0	Z	
-> S1	1		
-> S2	1		

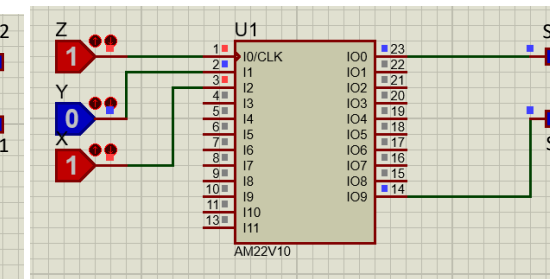
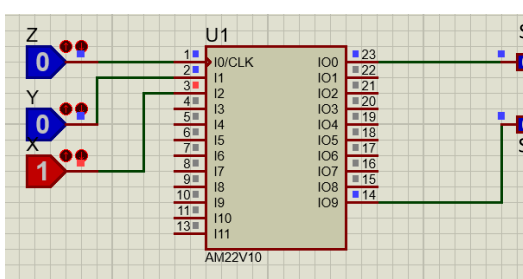
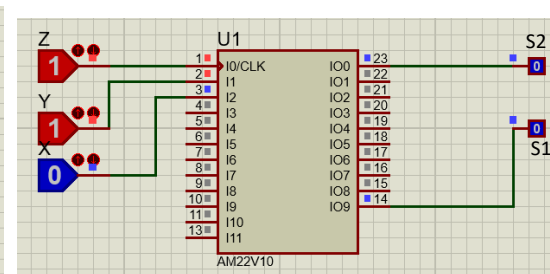
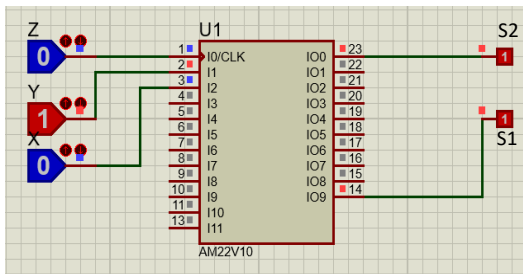
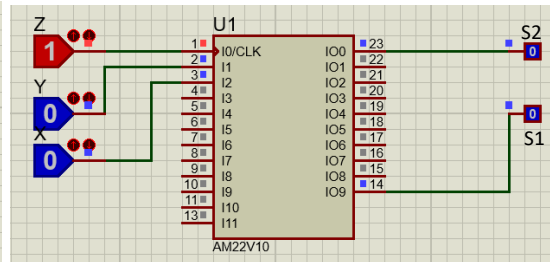
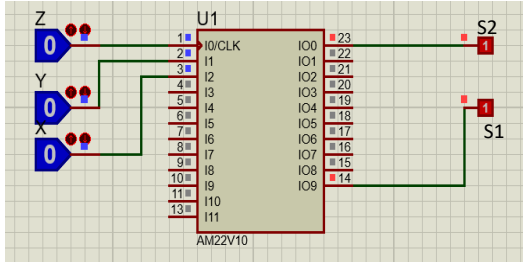
Name	Value	Status
X	0	X
Y	0	Y
Z	1	Z
S1	0	
S2	0	

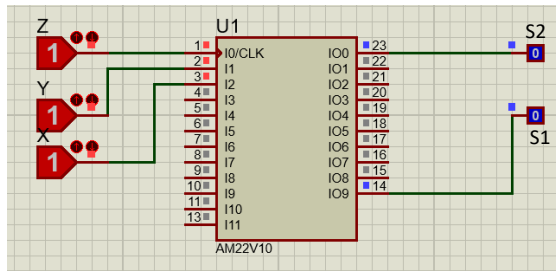
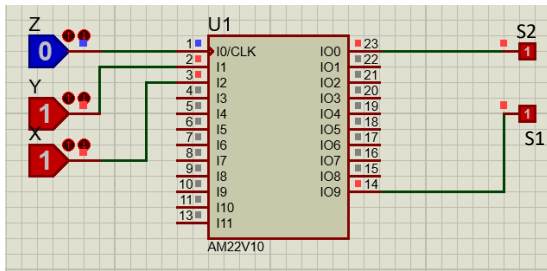
Name	Value	St.	t : 20 : : 40 : : 60 : : 80 : : 90 : : 120 : : 140 : : 160 : : 180 : : 200 ns
> X	0	X	
> Y	1	Y	
> Z	0	Z	
< S1	1		
< S2	1		

[illegible]



## Simulación en Proteus





c)

## Reducción con Algebra de Boole

$$\begin{aligned}
 & \text{c) } X \cdot \bar{Y} \cdot Z + W \cdot Y \cdot Z + W \cdot \bar{X} \cdot Z = X \cdot \bar{Y} \cdot Z + W \cdot Z \\
 & Z((X \cdot \bar{Y}) + (W \cdot Y) + (W \cdot \bar{X})) = X \cdot \bar{Y} \cdot Z + W \cdot Z \quad \text{Factorizar "Z"} \\
 & Z((X \cdot \bar{Y}) + (W(\bar{X} + Y))) = X \cdot \bar{Y} \cdot Z + W \cdot Z \quad \text{Factorizar "W"} \\
 & Z((X \cdot \bar{Y}) + W \cdot ((X \cdot \bar{Y}) + (\bar{X} \cdot Y))) = X \cdot \bar{Y} \cdot Z + W \cdot Z \quad \text{a) } X + (Y \cdot Z) = (X + Y) \cdot (X + Z) \\
 & Z(((X \cdot \bar{Y}) + W) \cdot ((X + \bar{X}) \cdot (Y + \bar{Y}))) = X \cdot \bar{Y} \cdot Z + W \cdot Z \quad \text{b) } X + (Y \cdot Z) = (X + Y) \cdot (X + Z) \\
 & Z(((X \cdot \bar{Y}) + W) \cdot 1 \cdot 1) = X \cdot \bar{Y} \cdot Z + W \cdot Z \quad \text{c) } X + \bar{X} = 1 \\
 & Z((X \cdot \bar{Y}) + W) = X \cdot \bar{Y} \cdot Z + W \cdot Z \quad \text{d) } X \cdot 1 = X \\
 & X \cdot \bar{Y} \cdot Z + W \cdot Z = X \cdot \bar{Y} \cdot Z + W \cdot Z \quad \text{e) } X \cdot (Y + Z) = (X \cdot Y) + (X \cdot Z)
 \end{aligned}$$

## Tablas de verdad

$$X \cdot \bar{Y} \cdot Z + W \cdot Y \cdot Z + W \cdot \bar{X} \cdot Z$$

$$X \cdot \bar{Y} \cdot Z + W \cdot Z$$

c)

X	Y	Z	W	$\bar{X}$	$\bar{Y}$	$X \cdot \bar{Y} \cdot Z$	$W \cdot Y \cdot Z$	$W \cdot \bar{X} \cdot Z$	$(X \cdot \bar{Y} \cdot Z) + (W \cdot Y \cdot Z) + (W \cdot \bar{X} \cdot Z)$
0	0	0	0	1	1	0	0	0	0
0	0	0	1	1	1	0	0	0	0
0	0	1	0	1	1	0	0	0	0
0	0	1	1	1	1	0	0	0	0
0	1	0	0	1	0	0	0	0	0
0	1	0	1	1	0	0	0	0	0
0	1	1	0	1	0	0	0	0	0
0	1	1	1	1	0	0	0	0	0
1	0	0	0	0	1	0	0	0	0
1	0	0	1	0	1	0	0	0	0
1	0	1	0	0	1	0	0	0	0
1	0	1	1	0	1	0	0	0	0
1	1	0	0	0	0	0	0	0	0
1	1	0	1	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0

X	Y	Z	W	$\bar{Y}$	$X \cdot \bar{Y} \cdot Z$	$W \cdot Z$	$(X \cdot \bar{Y} \cdot Z) + (W \cdot Z)$
0	0	0	0	1	0	0	0
0	0	0	1	1	0	0	0
0	0	1	0	1	0	0	0
0	0	1	1	1	0	0	0
0	1	0	0	0	0	0	0
0	1	0	1	0	0	0	0
0	1	1	0	0	0	0	0
0	1	1	1	0	0	0	0
1	0	0	0	1	0	0	0
1	0	0	1	1	0	0	0
1	0	1	0	1	0	0	0
1	0	1	1	1	0	0	0
1	1	0	0	0	0	0	0
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1	1	1	1	0	0	0	0

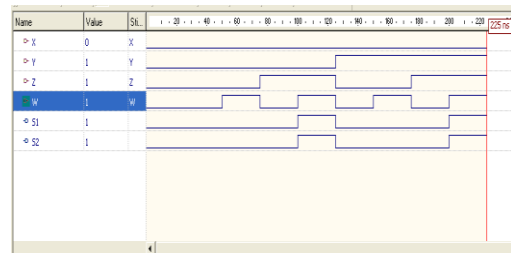
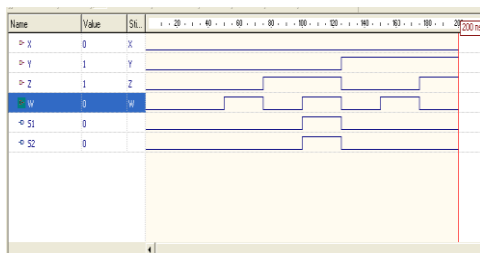
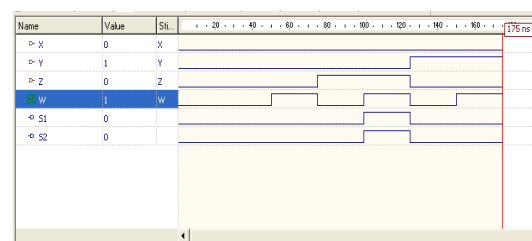
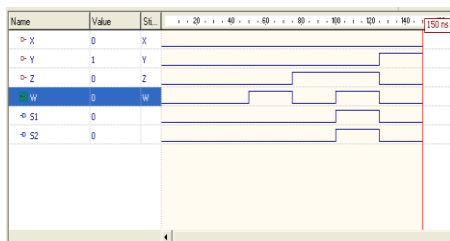
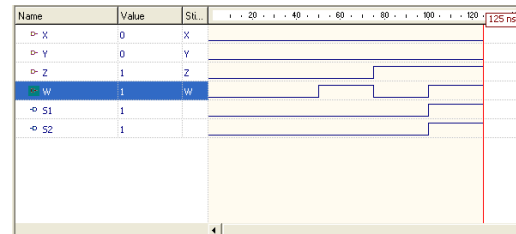
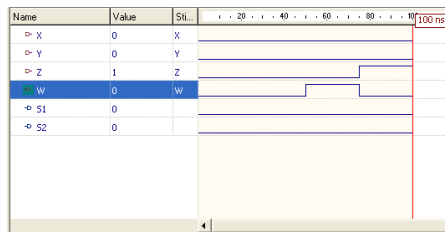
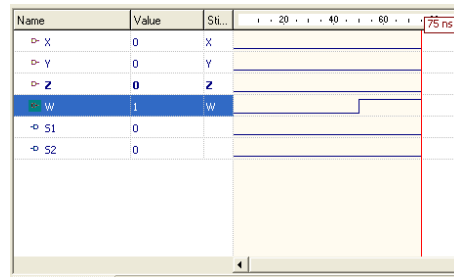
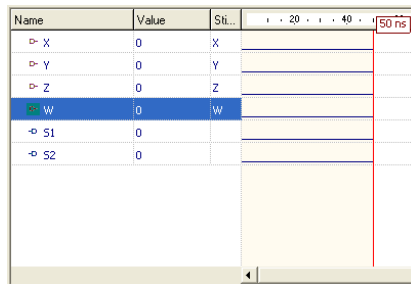
## Código VHDL

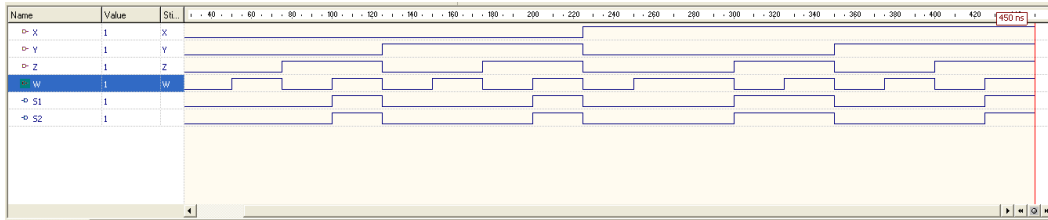
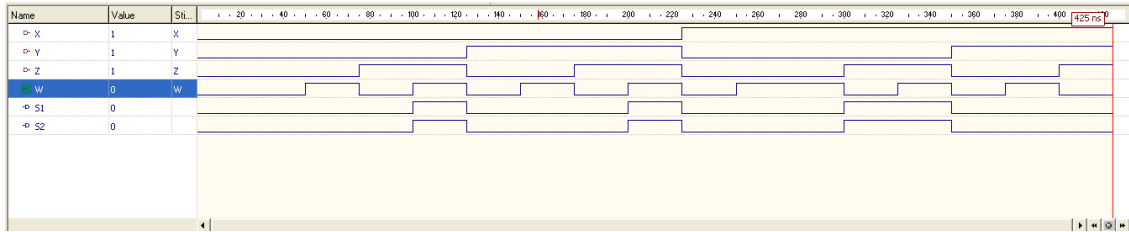
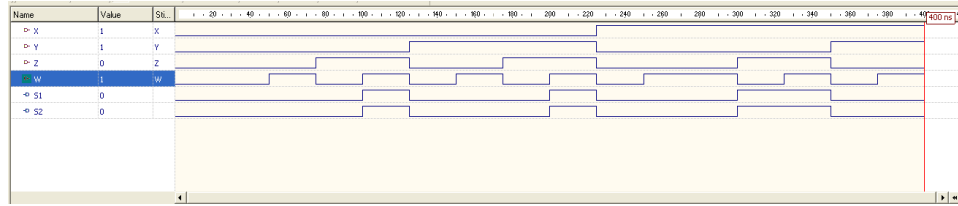
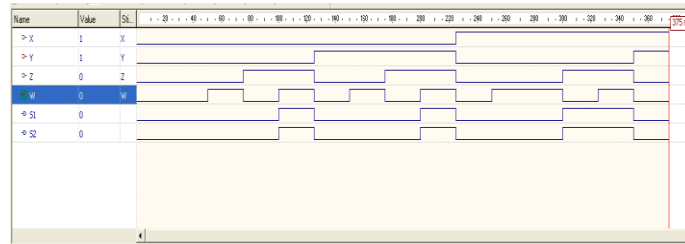
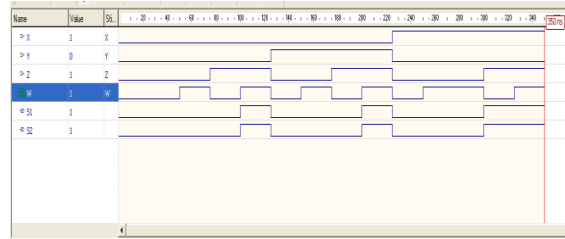
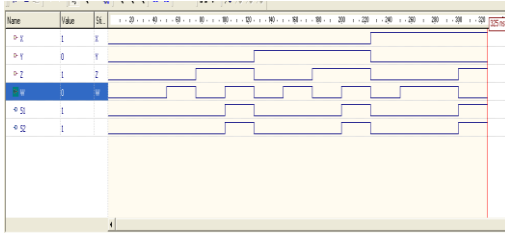
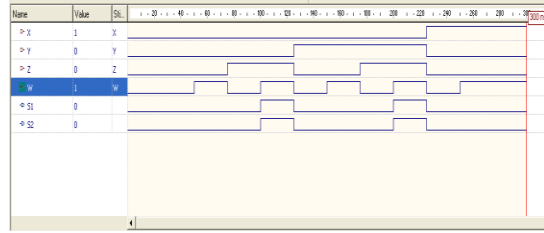
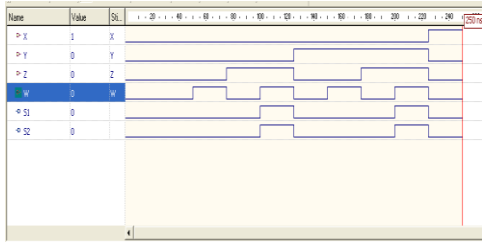
```

1 library ieee;
2 use ieee.std_logic_1164.all;
3 entity expresionc is
4 port(
5     X,Y,Z,W :in std_logic;
6     S1,S2 :out std_logic
7 );
8 end expresionc;
9 architecture Aexpresionc of expresionc is
10 begin
11     S1 <= (X AND (NOT Y) AND Z) OR (W AND Y AND Z) OR (W AND (NOT X) AND Z);
12     S2 <= (X AND (NOT Y) AND Z) OR (W AND Z);
13 end Aexpresionc;

```

## Simulación en Galaxy







## Simulación en Proteus

