

Práctica 10: Compuertas lógicas en VHDL

Nombre: Colín Ramiro Joel

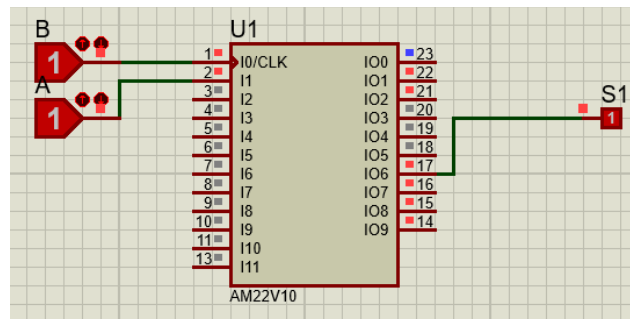
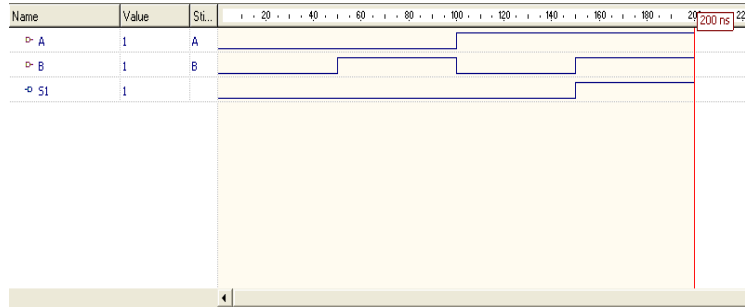
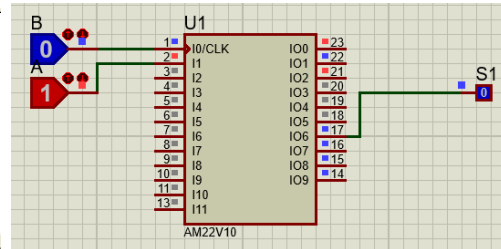
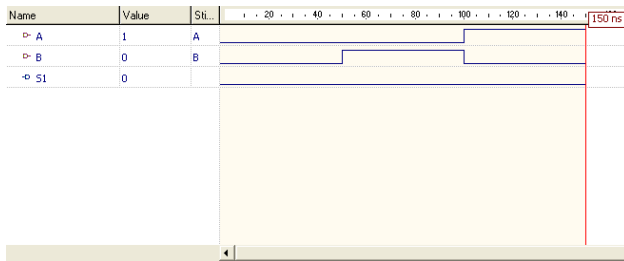
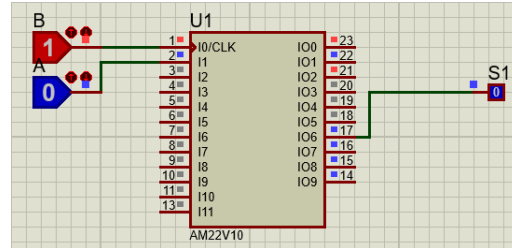
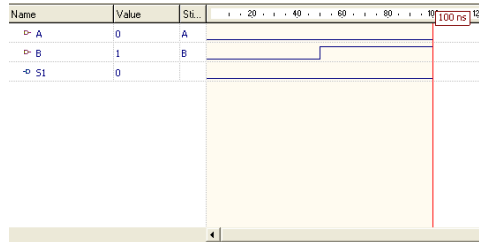
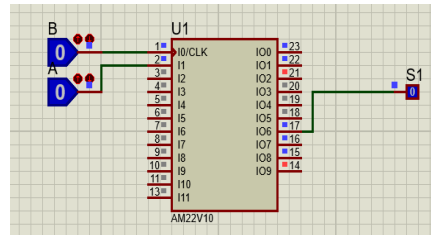
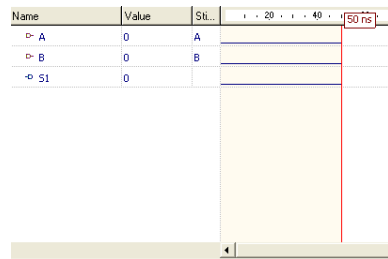
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Código:

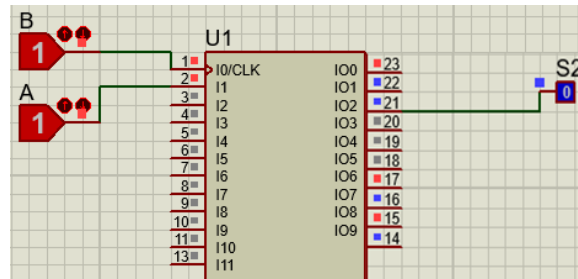
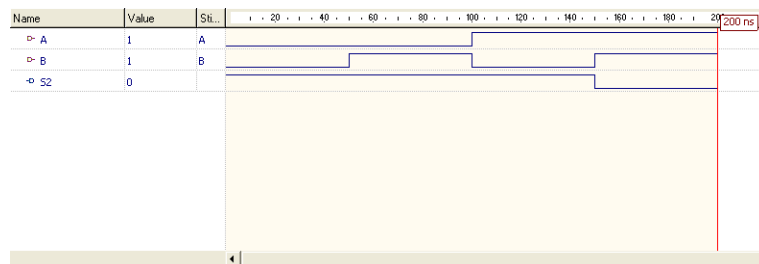
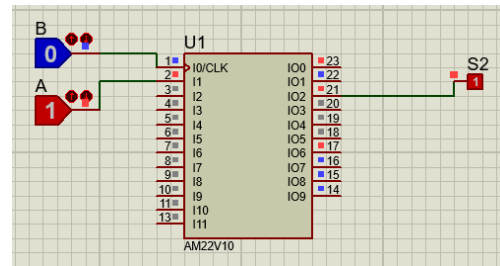
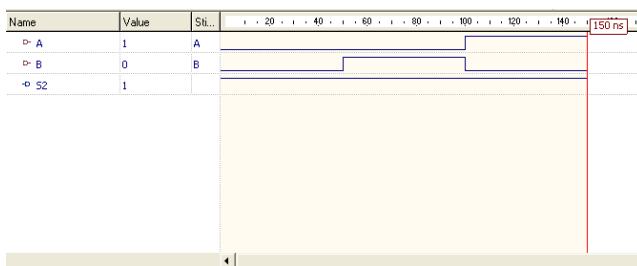
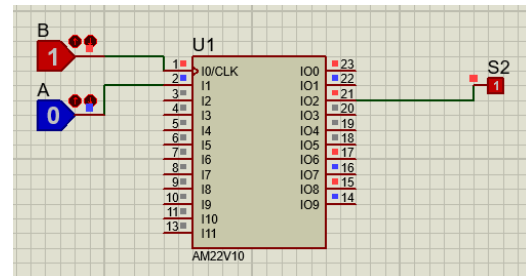
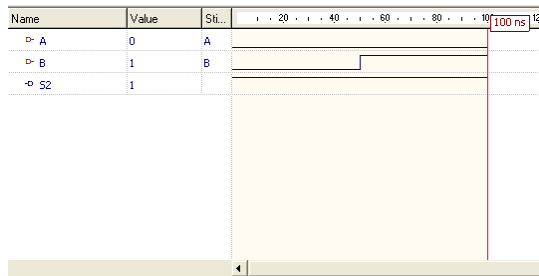
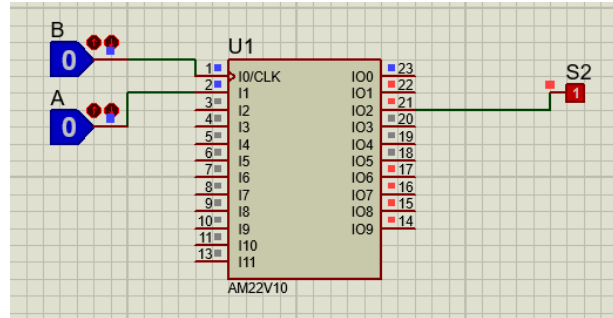
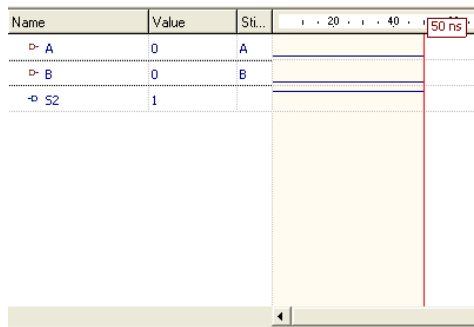
```
library ieee;
use ieee.std_logic_1164.all;
entity practica_diez is
port(
    A, B: in std_logic;
    S1, S2, S3, S4, S5, S6, S7: out std_logic
);
end practica_diez;

architecture Apractica_diez of practica_diez is
begin
    S1 <= (A AND B);
    S2 <= (A NAND B);
    S3 <= (A OR B);
    S4 <= (A NOR B);
    S5 <= (A XOR B);
    S6 <= (A XNOR B);
    S7 <= (NOT A);
end Apractica_diez;
```

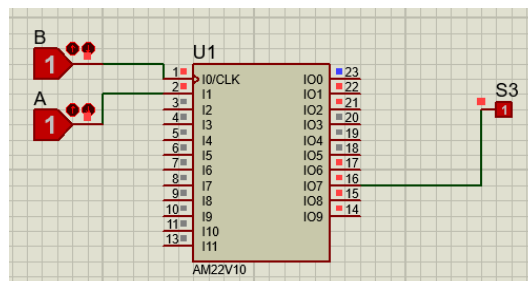
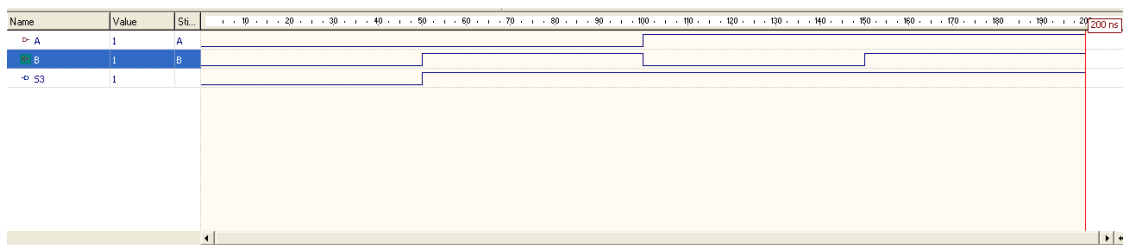
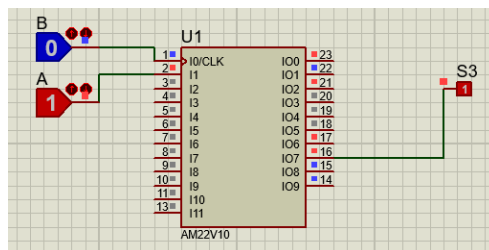
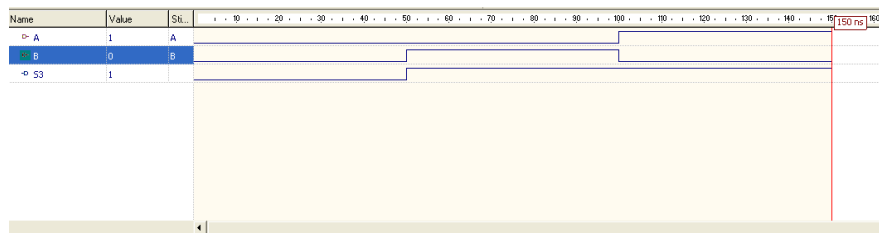
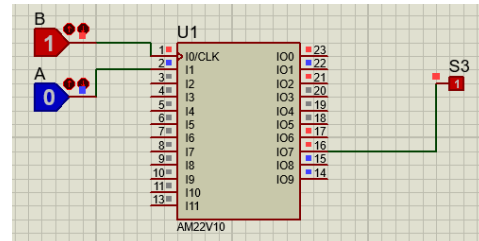
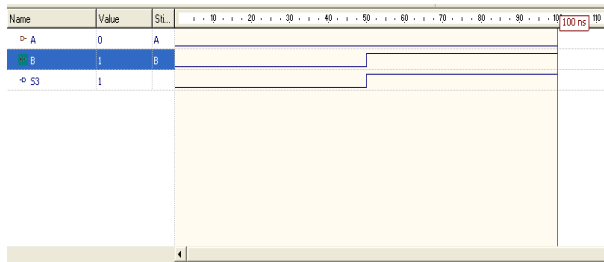
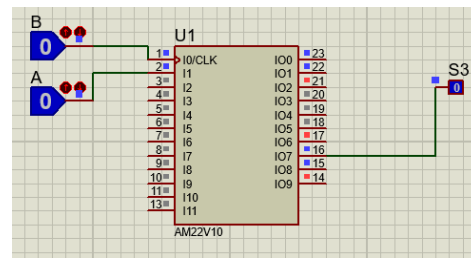
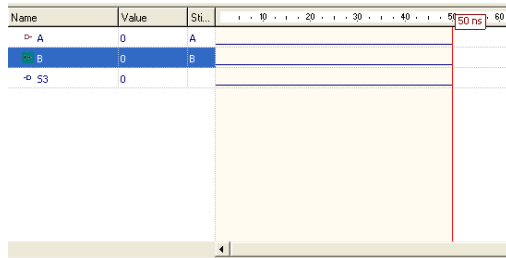
1.- A AND B



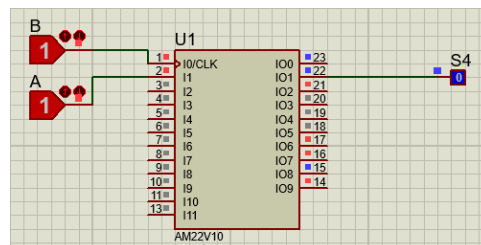
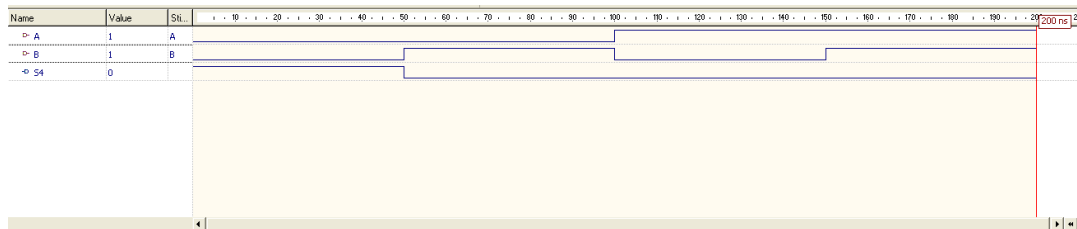
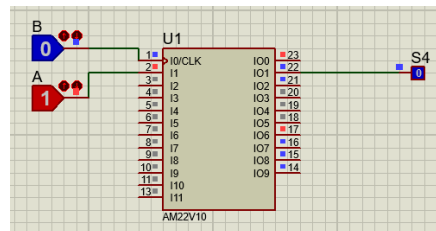
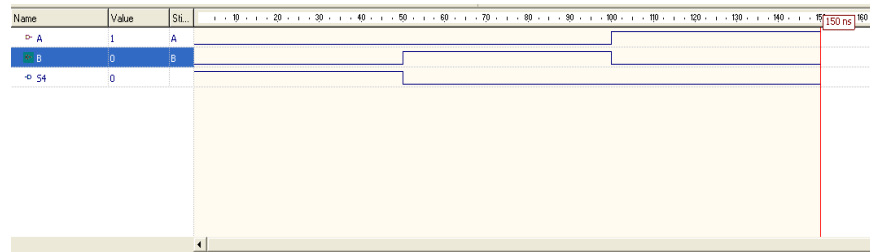
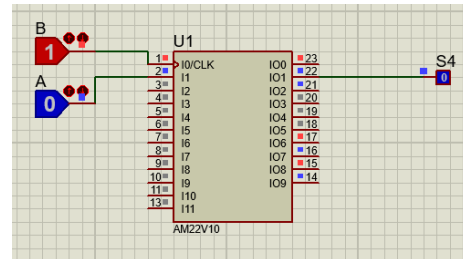
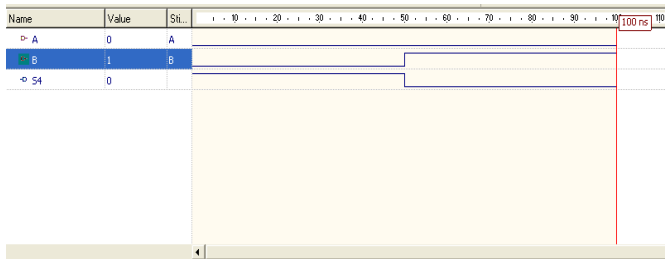
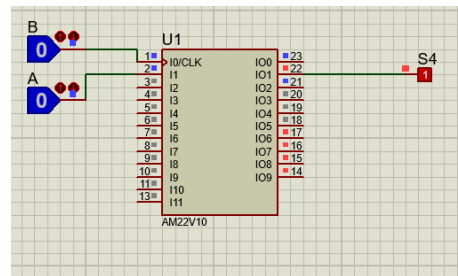
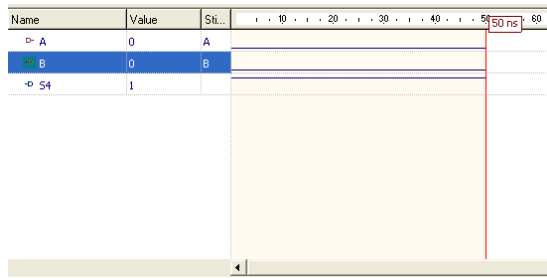
2.- A NAND B



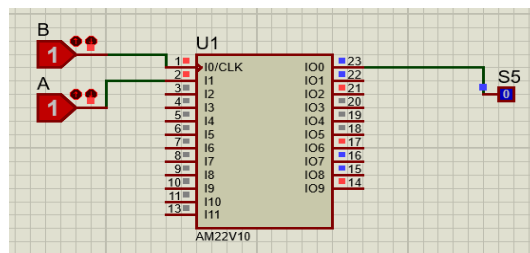
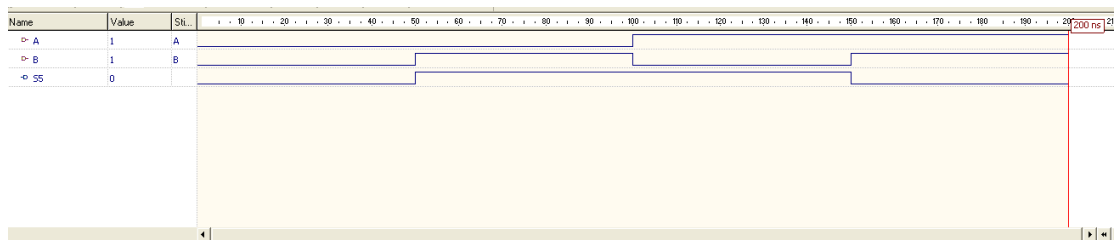
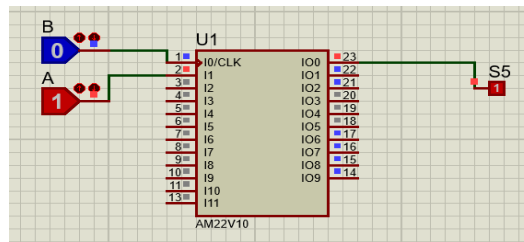
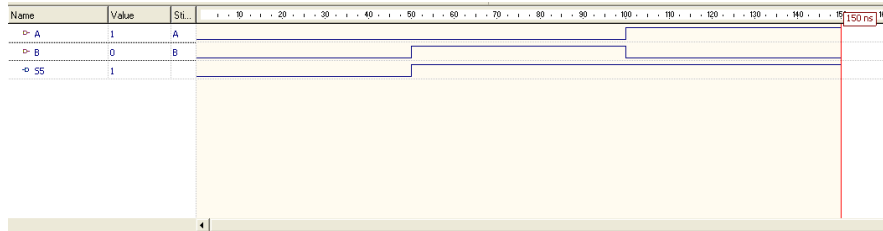
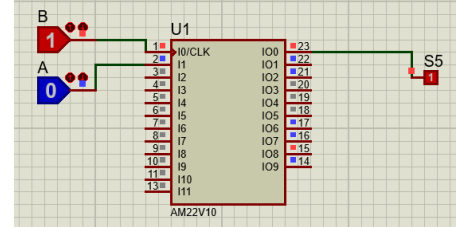
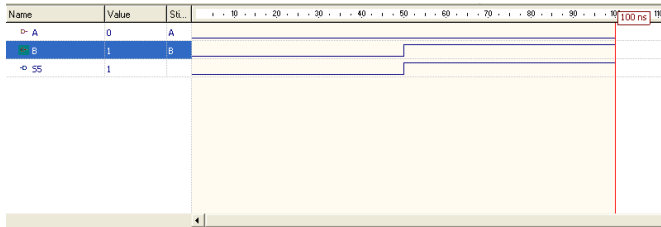
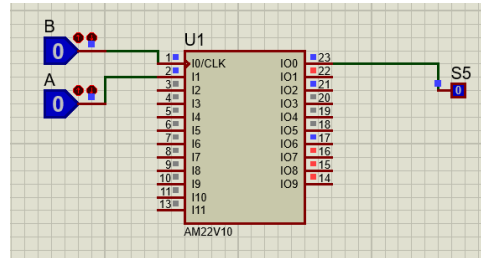
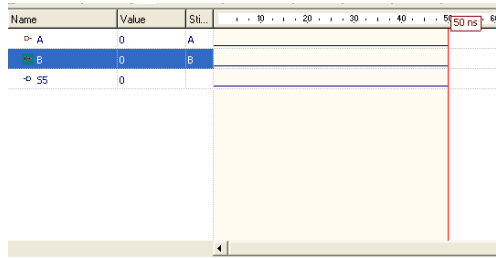
3.- A OR B



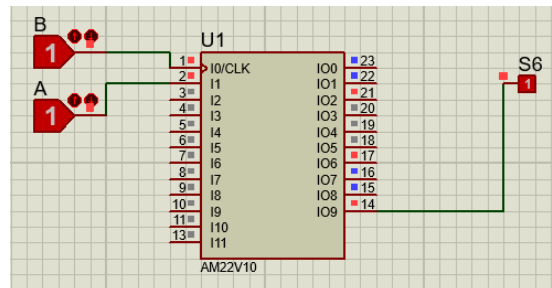
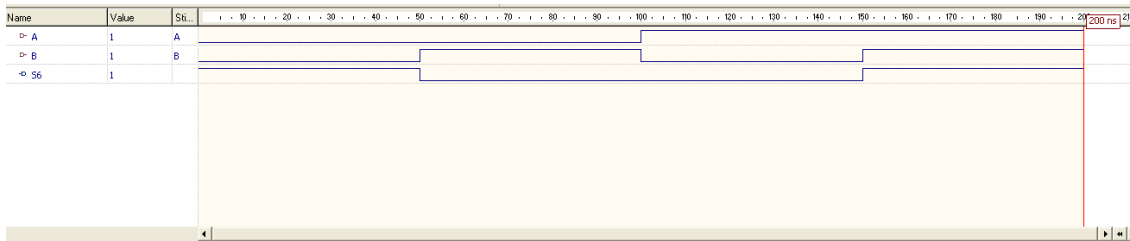
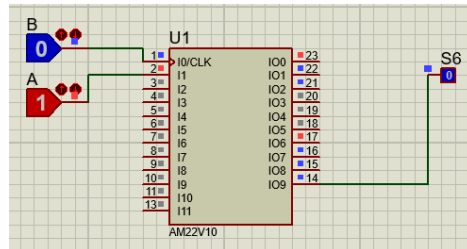
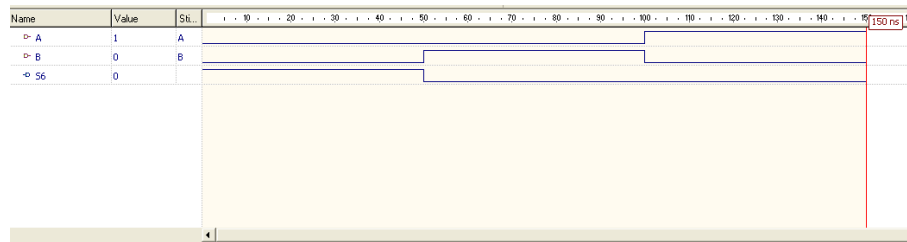
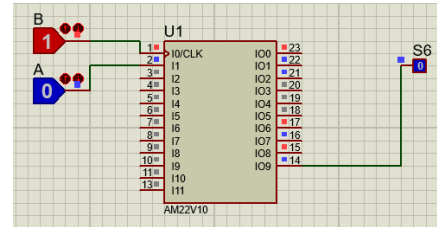
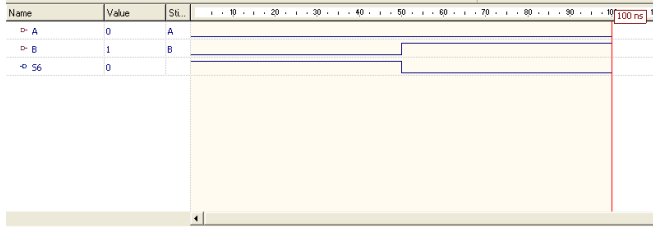
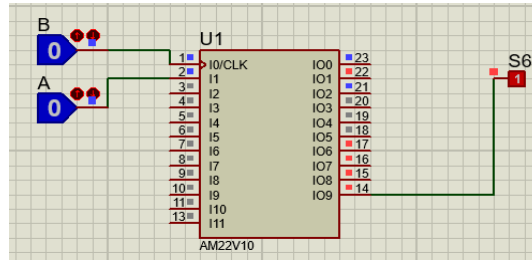
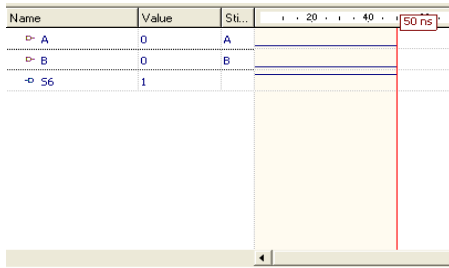
4.- A NOR B



5.- A XOR B



6.- A XNOR B



7.- NOT A

