



Instituto Politécnico Nacional

Escuela Superior de Cómputo

Diseño de Sistemas Digitales

Práctica 7: Contador Síncrono (boletas)

Integrantes: Bravo Esquivel Gustavo

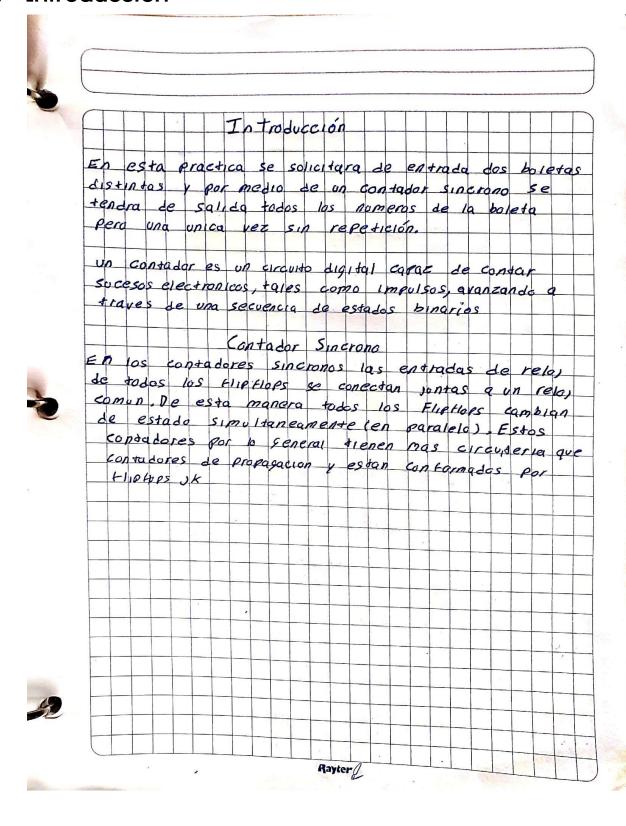
Colín Ramiro Joel

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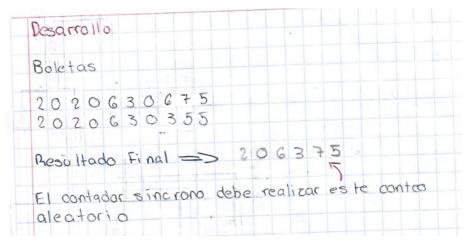
Profesor: Mújica Ascencio Cesar

Grupo: 4CV3

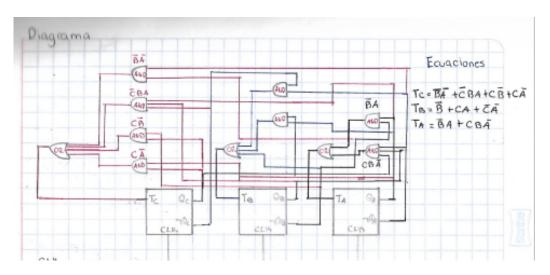
I. Introducción



II. Desarrollo

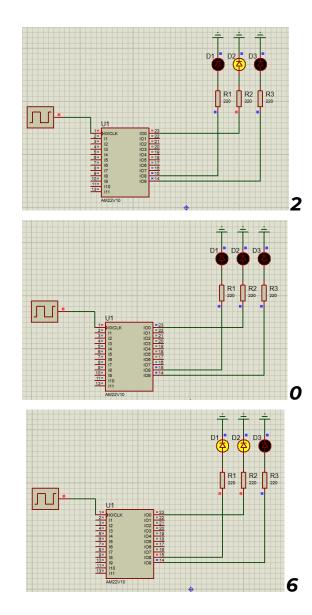


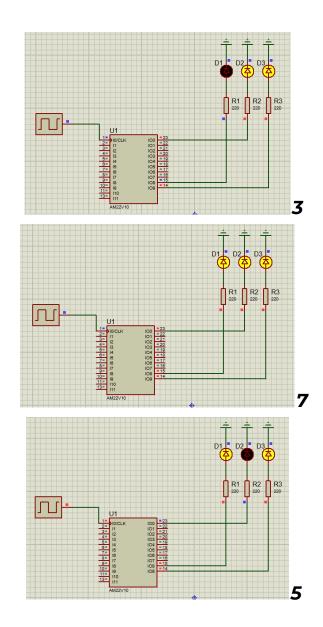
	1.515	Diegro		
	B* A* Tc	Te	TA	
0001		1	0	
0010	100	1	1	
0100	000	1	0	
0111	111	0	0	
1000	101	1	0	
1010	10 1	1	1	
1100	141	0	1	
1111	010	1	0	
1 1 1	Tc=	BA + (CB4+0	CB +CA
0 1 1 6		3 + CA	+ēĀ	



III. Simulaciones

Proteus





IV. Código VHDL

```
begin
               if(clk'event and clk='1')then
                      if(t0='0')then
                              internalQ0 <= internalQ0;
                      else
                              internalQ0 <= not internalQ0;
                      end if;
               end if;
       end process;
       process(clk, t1)
       begin
               if(clk'event and clk='1')then
                      if(t1='0')then
                              internalQ1 <= internalQ1;
                      else
                              internalQ1 <= not internalQ1;</pre>
                      end if:
               end if;
       end process;
       process(clk, t2)
       begin
               if(clk'event and clk='1')then
                      if(t2='0')then
                              internalQ2 <= internalQ2;
                      else
                              internalQ2 <= not internalQ2;
                      end if;
               end if:
       end process;
       notinternalQ0 <= not internalQ0;
       notinternalQ1 <= not internalQ1;
       notinternalQ2 <= not internalQ2;
       t0<= (notinternalQ1 and notinternalQ2) or (notinternalQ0 and internalQ1 and
       internalQ2) or (internalQ0 and notinternalQ1) or (internalQ0 and
       notinternalQ2);
       t1<= notinternalQ1 or (internalQ0 and internalQ2) or (notinternalQ0 and
       notinternalQ2);
       t2<= (notinternalQ1 and internalQ2) or (internalQ0 and internalQ1 and
       notinternalQ2);
       Q(0) \le internalQ0;
       Q(1) \le internalQ1;
       Q(2) \le internalQ2;
end architecture;
```

V. Conclusión y Bibliografía

