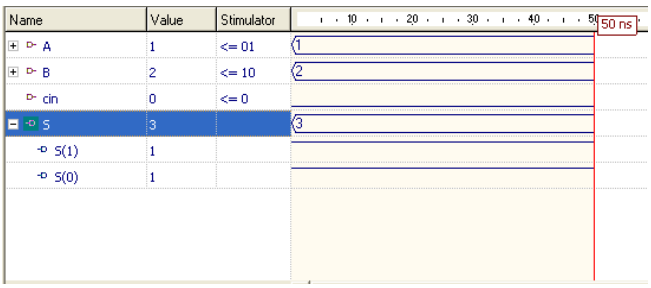
Práctica 16: Sumador de 4 bits

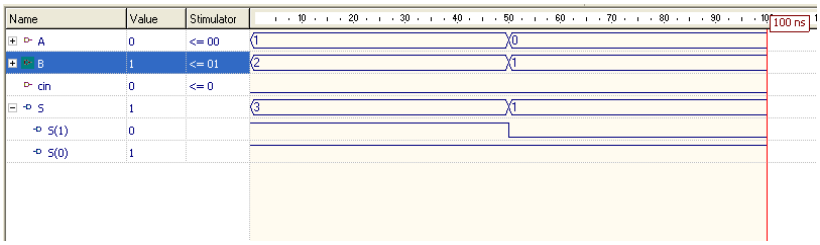
Nombre: Colín Ramiro Joel No. de lista: 3

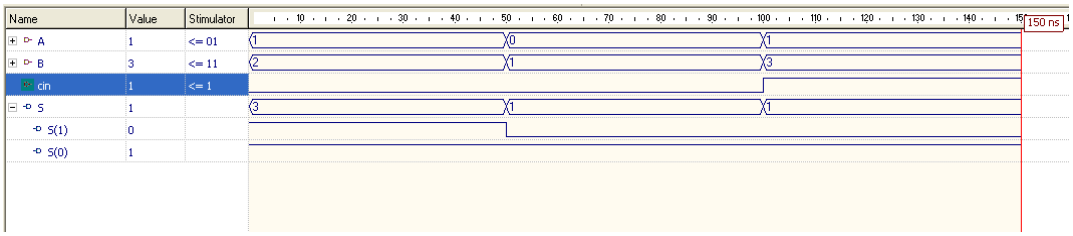
Código VHDL

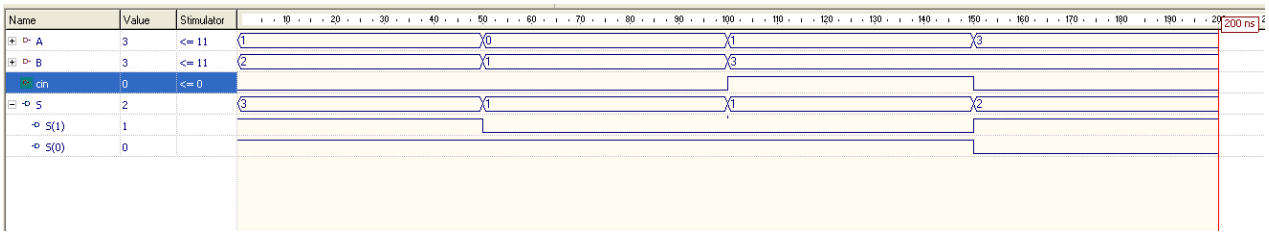
```
library ieee;
use ieee.std_logic_1164.all;
entity sumador4 is
port(
        A,B : in std_logic_vector(1 downto 0);
        cin : in std_logic;
        S :  out std_logic_vector (1 downto 0);
        co: out std_logic
);
end sumador4;

architecture asumador4 of sumador4 is
signal C : std_logic_vector(2 downto 0);
begin
        C(0) <= cin;
        s(0) <= A(0) XOR B(0) XOR C(0);
        C(1) <= (B(0) AND C(0)) OR(A(0) AND C(0)) OR (A(0) AND B(0));
        s(1) <= A(1) XOR B(1) XOR C(1);
        C(2) <= (B(1) AND C(1)) OR(A(1) AND C(1)) OR (A(1) AND B(1));
        co <= C(2);
end asumador4;
```

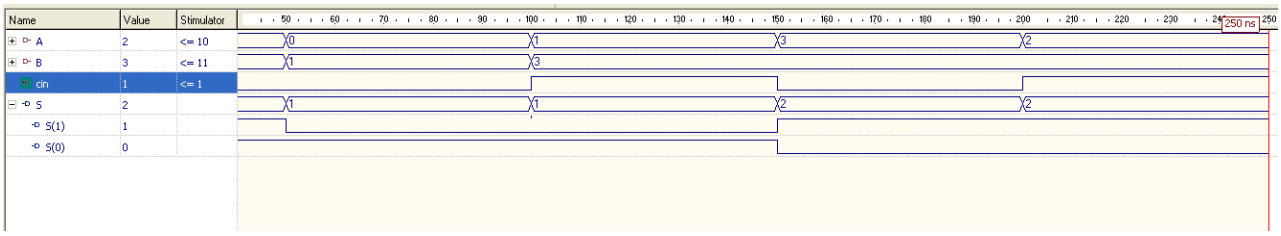
Capturas en Galaxy



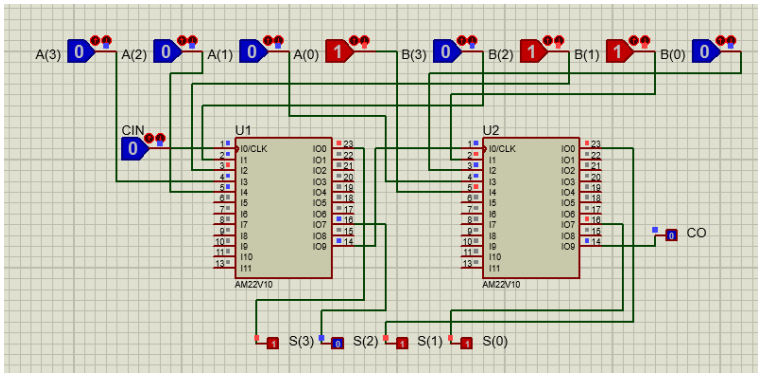


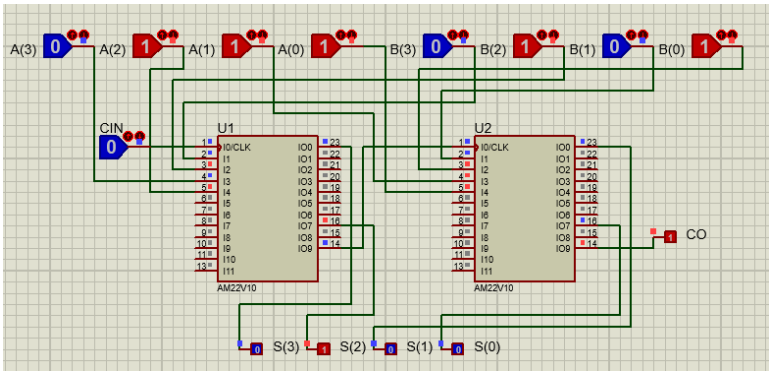


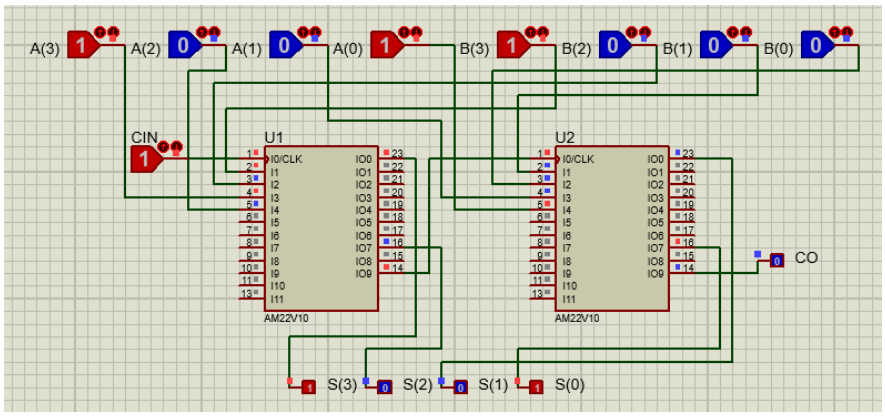


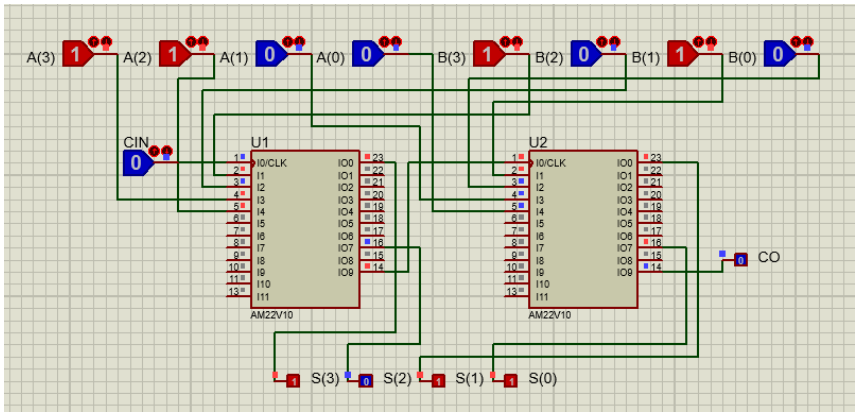


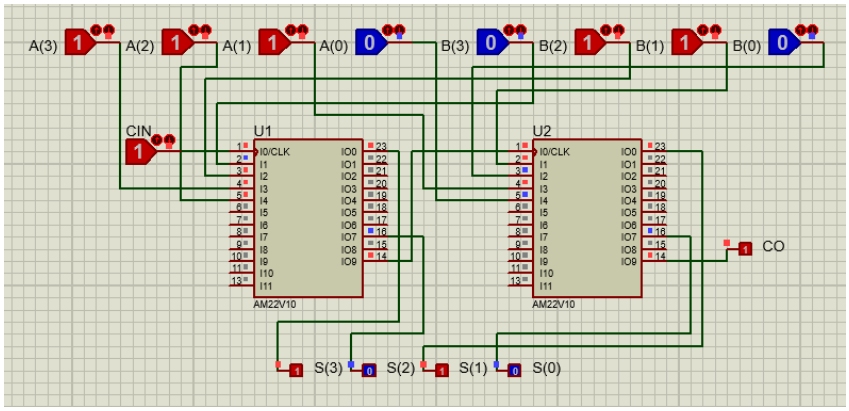
Capturas en Proteus






A(3) 1
A(2) 0
A(1) 0
A(0) 1
B(3) 1
B(2) 0
B(1) 0
B(0) 0
CIN 1
U1
U2
I0/CLK
I1
I2
I3
I4
I5
I6
I7
I8
I9
I10
I11
IO0
IO1
IO2
IO3
IO4
IO5
IO6
IO7
IO8
IO9
AM22V10
CO 0
S(3) 1
S(2) 0
S(1) 1
S(0)


A(3) 1
A(2) 1
A(1) 0
A(0) 0
B(3) 1
B(2) 0
B(1) 1
B(0) 0
CIN 0
U1
U2
I0/CLK
I1
I2
I3
I4
I5
I6
I7
I8
I9
I10
I11
IO0
IO1
IO2
IO3
IO4
IO5
IO6
IO7
IO8
IO9
AM22V10
CO 0
S(3) 1
S(2) 0
S(1) 1
S(0) 1


A(3) 1
A(2) 1
A(1) 1
A(0) 0
B(3) 0
B(2) 1
B(1) 1
B(0) 0
CIN 1
U1
U2
I0/CLK
I1
I2
I3
I4
I5
I6
I7
I8
I9
I10
I11
IO0
IO1
IO2
IO3
IO4
IO5
IO6
IO7
IO8
IO9
AM22V10
CO 1
S(3) 1
S(2) 1
S(1) 0
S(0)