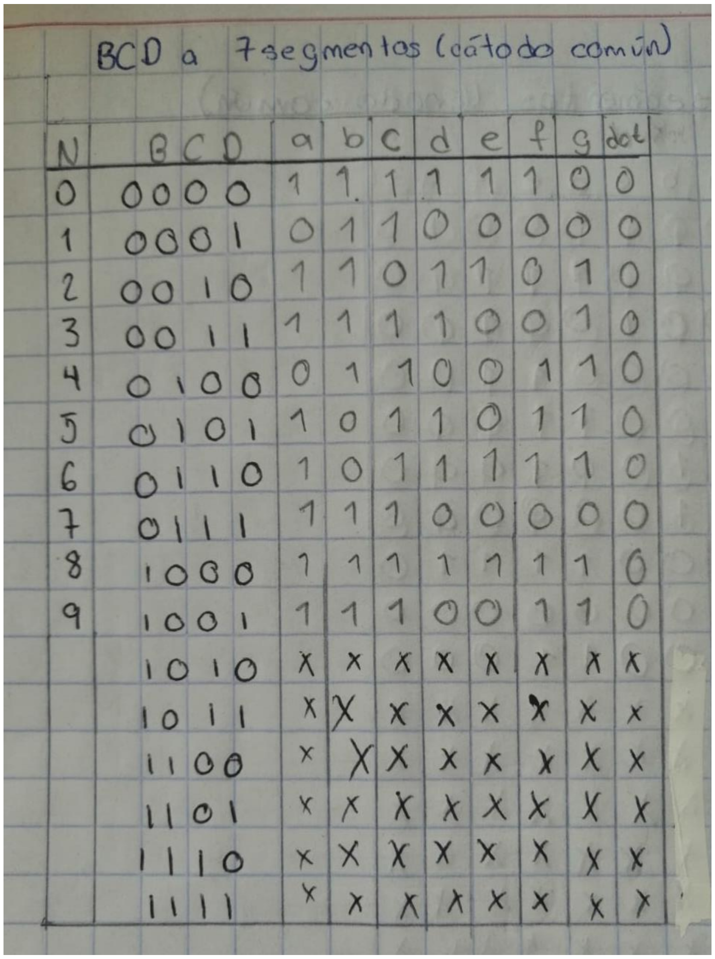
Práctica 15: Convertidores de código

Nombre: Colín Ramiro Joel No. de lista: 3

a) BCD a display de 7 segmentos de cátodo común

Tabla de verdad

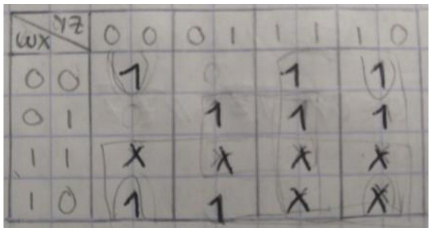


BCD a 7segmentos (cátodo común)

N	BCD	a	b	c	d	e	f	g	dot
0	0000	1	1	1	1	1	1	0	0
1	0001	0	1	1	0	0	0	0	0
2	0010	1	1	0	1	1	0	1	0
3	0011	1	1	1	1	0	0	1	0
4	0100	0	1	1	0	0	1	1	0
5	0101	1	0	1	1	0	1	1	0
6	0110	1	0	1	1	1	1	1	0
7	0111	1	1	1	0	0	0	0	0
8	1000	1	1	1	1	1	1	1	0
9	1001	1	1	1	0	0	1	1	0
	1010	X	X	X	X	X	X	X	X
	1011	X	X	X	X	X	X	X	X
	1100	X	X	X	X	X	X	X	X
	1101	X	X	X	X	X	X	X	X
	1110	X	X	X	X	X	X	X	X
	1111	X	X	X	X	X	X	X	X

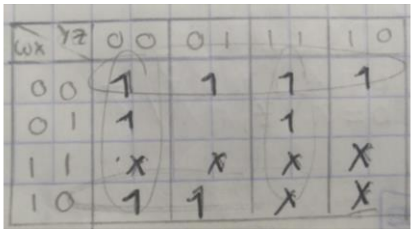
Mapas de Karnaugh

a)



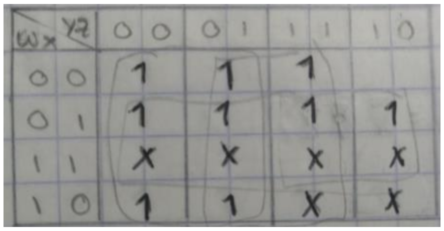
wx \ yz	00	01	11	10
00	1		1	1
01		1	1	1
11	X	X	X	X
10	1	1	X	X

b)



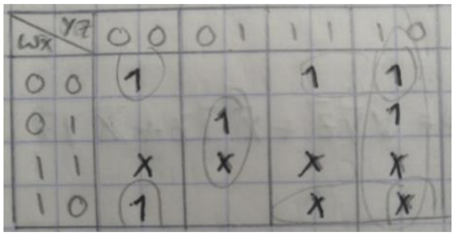
wx \ yz	00	01	11	10
00	1	1	1	1
01	1		1	
11	X	X	X	X
10	1	1	X	X

c)



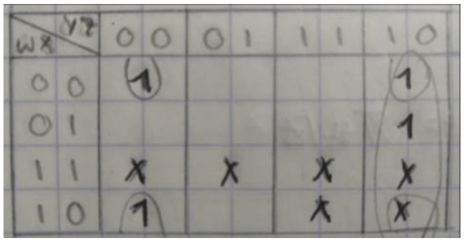
wx \ yz	00	01	11	10
00	1	1	1	
01	1	1	1	1
11	X	X	X	X
10	1	1	X	X

d)



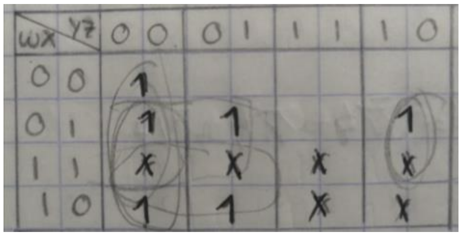
wx \ yz	00	01	11	10
00	1		1	1
01		1		1
11	X	X	X	X
10	1		X	X

e)



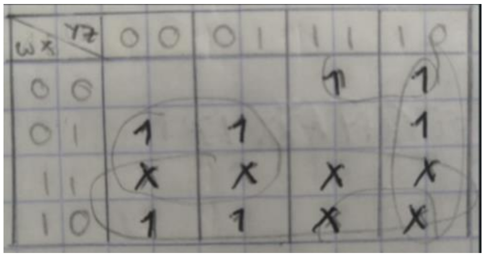
wx \ yz	00	01	11	10
00	1			1
01				1
11	X	X	X	X
10	1		X	X

f)



wx \ yz	00	01	11	10
00	1			
01	1	1		1
11	X	X	X	X
10	1	1	X	X

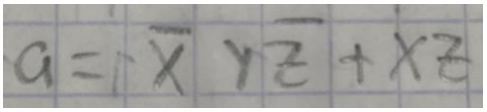
g)



wx \ yz	00	01	11	10
00			1	1
01	1	1		1
11	X	X	X	X
10	1	1	X	X

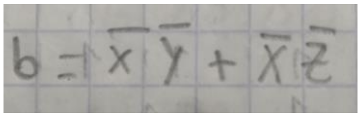
Ecuaciones de salida

a)



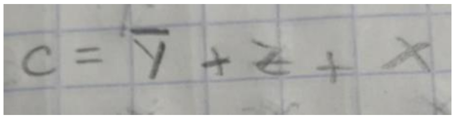
$a = \bar{x}\, y \bar{z} + x z$

b)



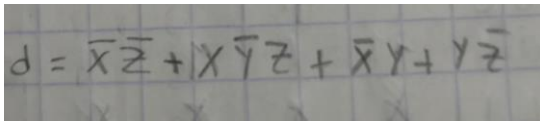
$b = \bar{x}\,\bar{y} + \bar{x}\,\bar{z}$

c)



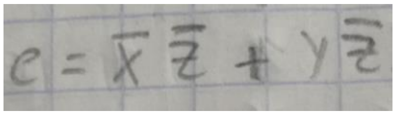
$c = \bar{y} + z + x$

d)



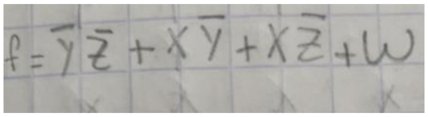
$d = \bar{x}\bar{z} + x\bar{y}z + \bar{x}y + y\bar{z}$

e)



$e = \bar{x}\,\bar{z} + y\bar{z}$

f)



$f = \bar{y}\bar{z} + x\bar{y} + x\bar{z} + w$

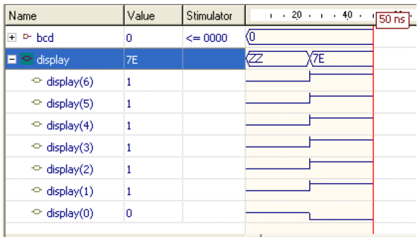
g)

$$g = \bar{x}y + x\bar{y} + w + y\bar{z}$$

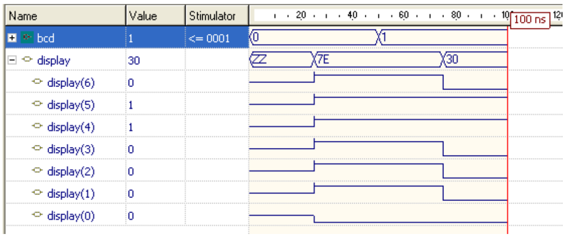
Código en VHDL

```
library ieee;
use ieee.std_logic_1164.all;
entity cod1 is
port(
        bcd : in std_logic_vector(3 downto 0);
        display : out std_logic_vector(6 downto 0)
);
end cod1;
architecture acod1 of cod1 is
begin
        display <= "1111110" when bcd = "0000" else
                        "0110000" when bcd = "0001" else
                        "1101101" when bcd = "0010" else
                        "1111001" when bcd = "0011" else
                        "0110011" when bcd = "0100" else
                        "1011011" when bcd = "0101" else
                        "1011111" when bcd = "0110" else
                        "1110000" when bcd = "0111" else
                        "1111111" when bcd = "1000" else
                        "1110011" when bcd = "1001" else
                        "0000000";
end acod1;
```

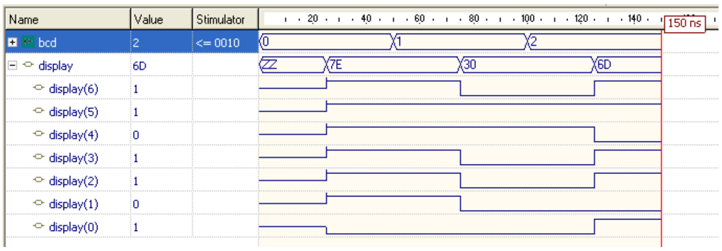
Simulación en Galaxy



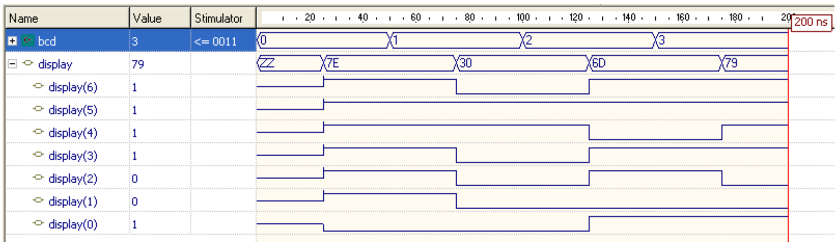
Name	Value	Stimulator
bcd	0	<= 0000
display	7E	
display(6)	1	
display(5)	1	
display(4)	1	
display(3)	1	
display(2)	1	
display(1)	1	
display(0)	0	



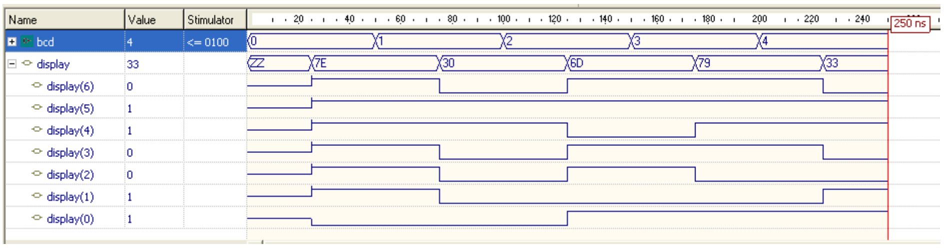
Name	Value	Stimulator
bcd	1	<= 0001
display	30	
display(6)	0	
display(5)	1	
display(4)	1	
display(3)	0	
display(2)	0	
display(1)	0	
display(0)	0	



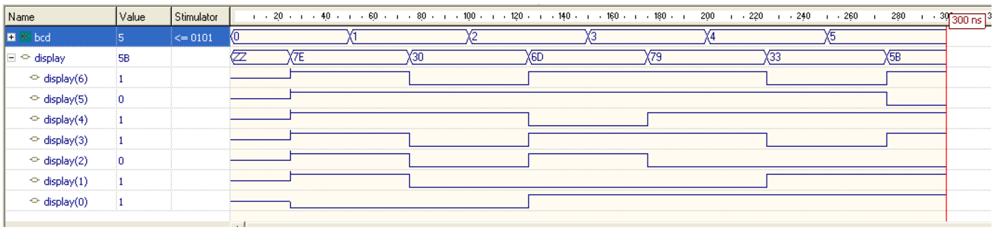
Name	Value	Stimulator
bcd	2	<= 0010
display	6D	
display(6)	1	
display(5)	1	
display(4)	0	
display(3)	1	
display(2)	1	
display(1)	0	
display(0)	1	



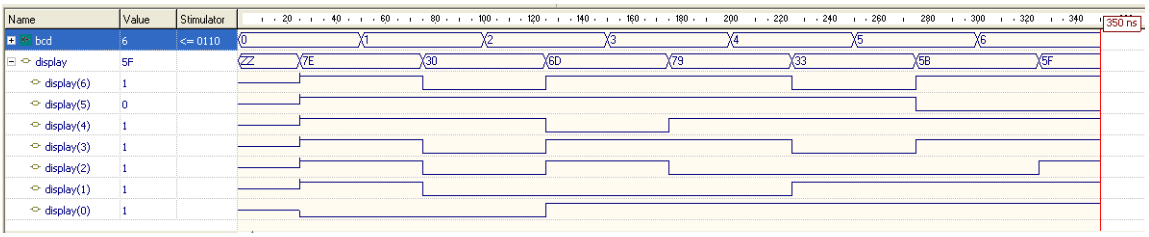
Name	Value	Stimulator
bcd	3	<= 0011
display	79	
display(6)	1	
display(5)	1	
display(4)	1	
display(3)	1	
display(2)	0	
display(1)	0	
display(0)	1	



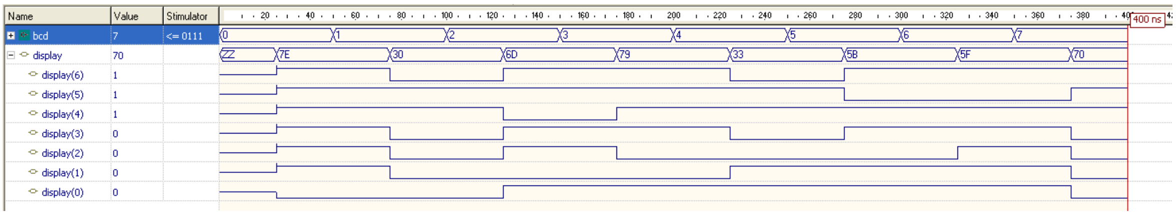
Name	Value	Stimulator
bcd	4	<= 0100
display	33	
display(6)	0	
display(5)	1	
display(4)	1	
display(3)	0	
display(2)	0	
display(1)	1	
display(0)	1	



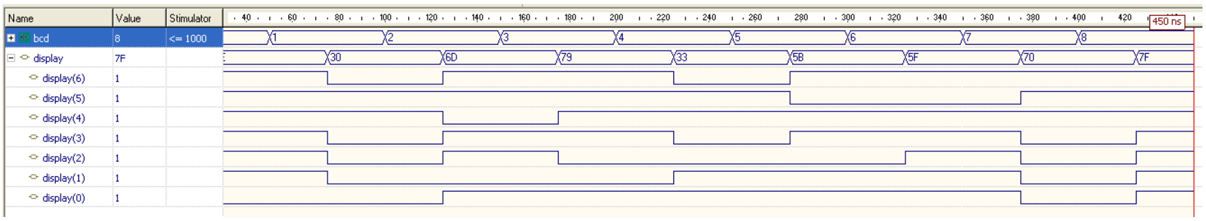
Name	Value	Stimulator
bcd	5	<= 0101
display	5B	
display(6)	1	
display(5)	0	
display(4)	1	
display(3)	1	
display(2)	0	
display(1)	1	
display(0)	1	



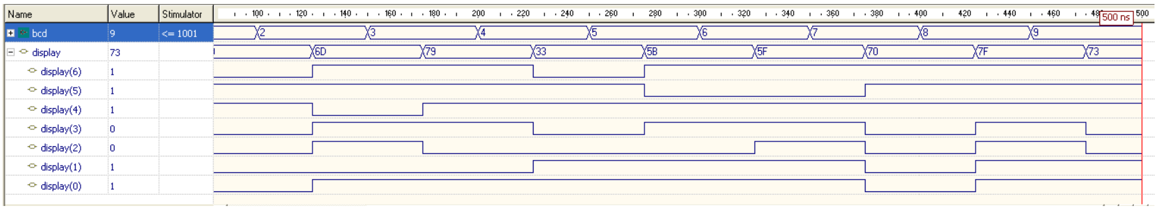
Name	Value	Stimulator
bcd	6	<= 0110
display	5F	
display(6)	1	
display(5)	0	
display(4)	1	
display(3)	1	
display(2)	1	
display(1)	1	
display(0)	1	



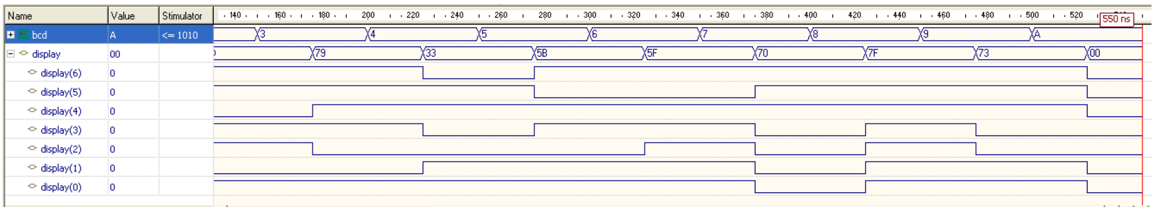
Name	Value	Stimulator
bcd	7	<= 0111
display	70	
display(6)	1	
display(5)	1	
display(4)	1	
display(3)	0	
display(2)	0	
display(1)	0	
display(0)	0	



Name	Value	Stimulator
bcd	8	<= 1000
display	7F	
display(6)	1	
display(5)	1	
display(4)	1	
display(3)	1	
display(2)	1	
display(1)	1	
display(0)	1	

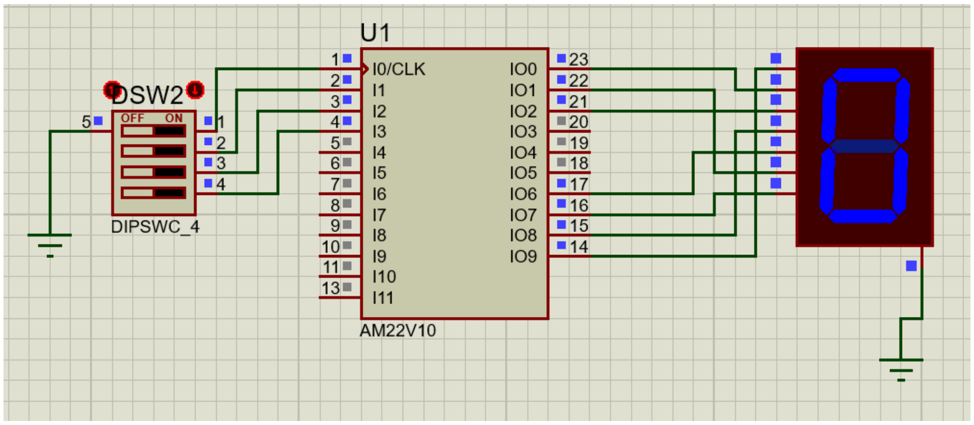


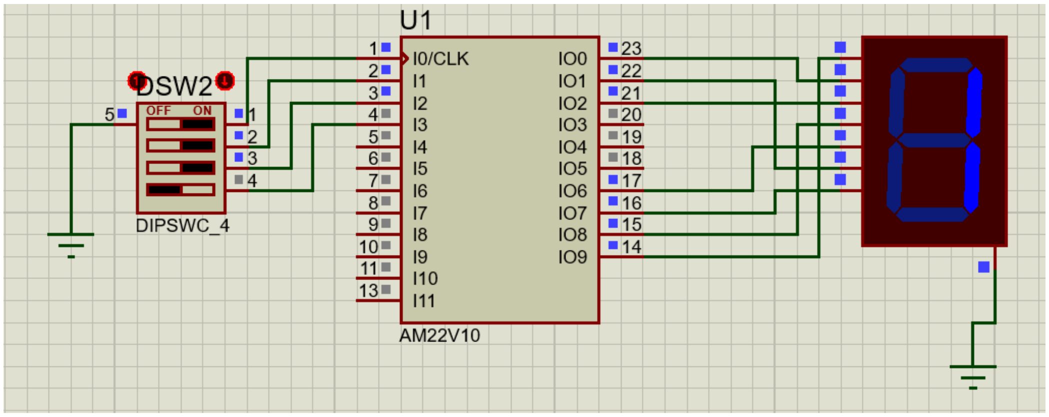
Name	Value	Stimulator
bcd	9	<= 1001
display	73	
display(6)	1	
display(5)	1	
display(4)	1	
display(3)	0	
display(2)	0	
display(1)	1	
display(0)	1	



Name	Value	Stimulator
bcd	A	<= 1010
display	00	
display(6)	0	
display(5)	0	
display(4)	0	
display(3)	0	
display(2)	0	
display(1)	0	
display(0)	0	

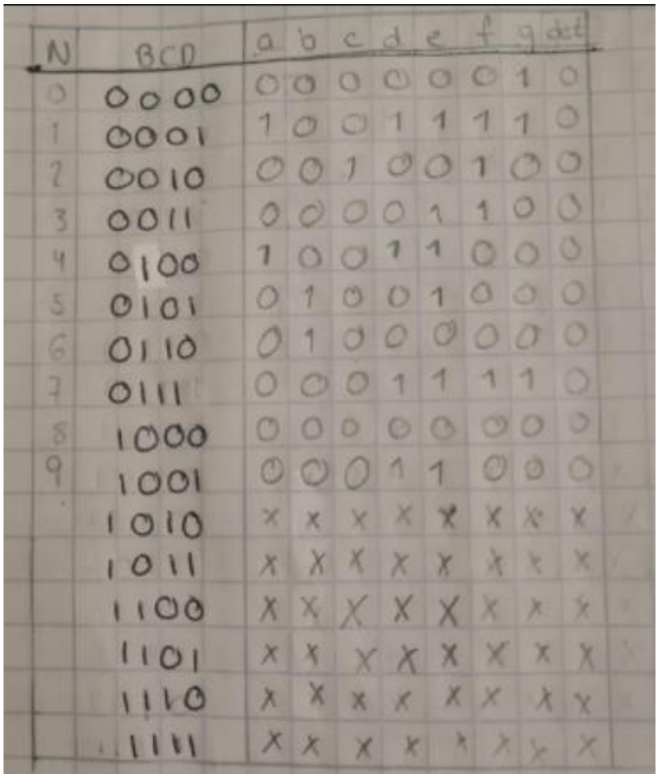
Simulación de 2 casos en Proteus





b) BCD a display de 7 segmento de ánodo común

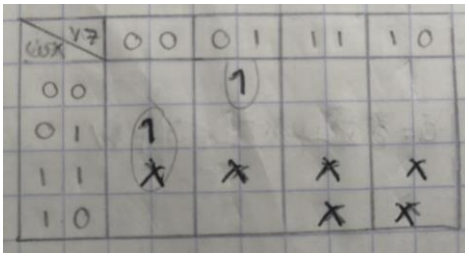
Tabla de verdad



N	BCD	a	b	c	d	e	f	g	dot
0	0000	0	0	0	0	0	0	1	0
1	0001	1	0	0	1	1	1	1	0
2	0010	0	0	1	0	0	1	0	0
3	0011	0	0	0	0	1	1	0	0
4	0100	1	0	0	1	1	0	0	0
5	0101	0	1	0	0	1	0	0	0
6	0110	0	1	0	0	0	0	0	0
7	0111	0	0	0	1	1	1	1	0
8	1000	0	0	0	0	0	0	0	0
9	1001	0	0	0	1	1	0	0	0
	1010	x	x	x	x	x	x	x	x
	1011	x	x	x	x	x	x	x	x
	1100	x	x	x	x	x	x	x	x
	1101	x	x	x	x	x	x	x	x
	1110	x	x	x	x	x	x	x	x
	1111	x	x	x	x	x	x	x	x

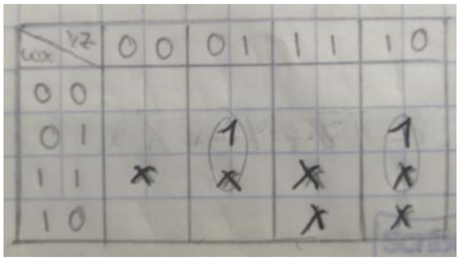
Mapas de Karnaugh

a)



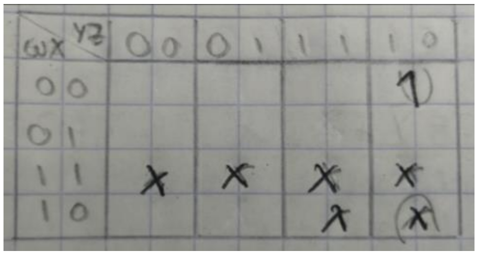
wx \ yz	00	01	11	10
00		1		
01	1			
11	x	x	x	x
10			x	x

b)



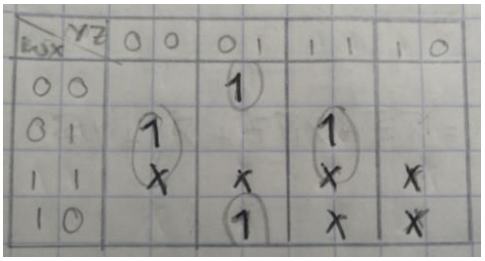
wx \ yz	00	01	11	10
00				
01		1		1
11	x	x	x	x
10			x	x

c)



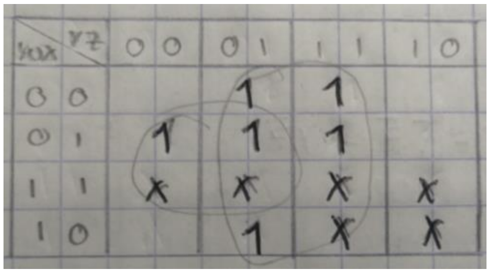
wx \ yz	00	01	11	10
00				1
01				
11	x	x	x	x
10			x	x

d)



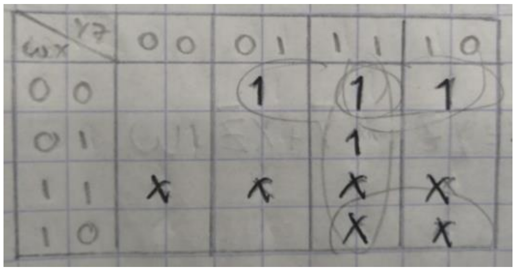
wx \ yz	00	01	11	10
00		1		
01	1		1	
11	x	x	x	x
10		1	x	x

e)



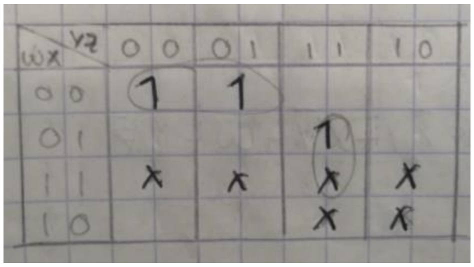
ωx \ yz	0 0	0 1	1 1	1 0
0 0		1	1	
0 1	1	1	1	
1 1	x	x	x	x
1 0		1	x	x

f)



ωx \ yz	0 0	0 1	1 1	1 0
0 0		1	1	1
0 1			1	
1 1	x	x	x	x
1 0			x	x

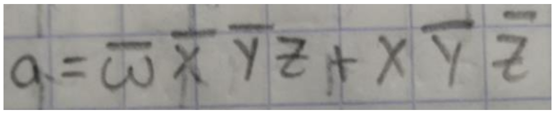
g)



ωx \ yz	0 0	0 1	1 1	1 0
0 0	1	1		
0 1			1	
1 1	x	x	x	x
1 0			x	x

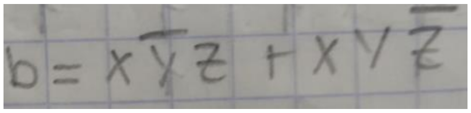
Ecuaciones de salida

a)



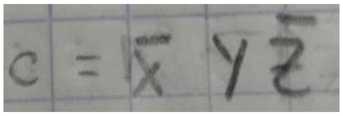
$$a = \bar{\omega}\bar{x}\bar{y}z + x\bar{y}\bar{z}$$

b)



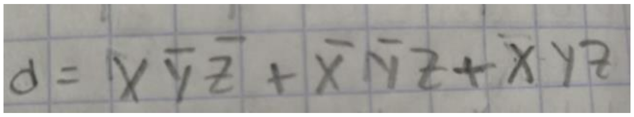
$$b = x\bar{y}z + xy\bar{z}$$

c)



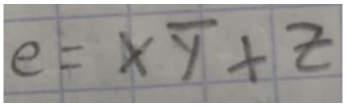
$$c = \bar{x}y\bar{z}$$

d)



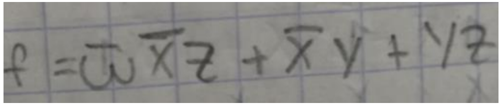
$$d = x\bar{y}\bar{z} + \bar{x}\bar{y}z + xyz$$

e)



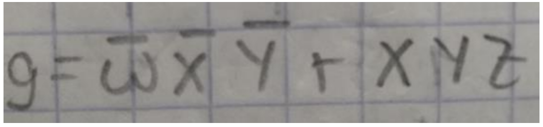
$$e = x\bar{y} + z$$

f)



$$f = \bar{\omega}\bar{x}z + \bar{x}y + yz$$

g)

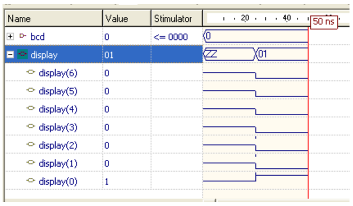


$$g = \bar{\omega}\bar{x}\bar{y} + xyz$$

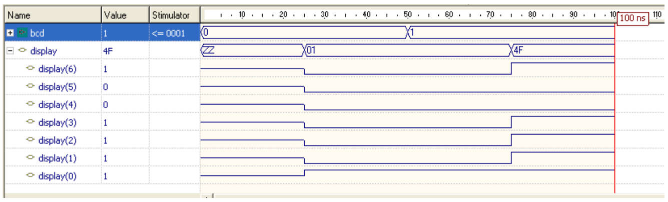
Código en VHDL

```
library ieee;
use ieee.std_logic_1164.all;
entity cod2 is
port(
    bcd : in std_logic_vector(3 downto 0);
    display : out std_logic_vector(6 downto 0)
);
end cod2;
architecture acod2 of cod2 is
begin
    process(bcd)
    begin
        if(bcd = "0000") then
            display <= "0000001";
        elsif(bcd = "0001") then
            display <= "1001111";
        elsif(bcd = "0010") then
            display <= "0010010";
        elsif(bcd = "0011") then
            display <= "0000110";
        elsif(bcd = "0100") then
            display <= "1001100";
        elsif(bcd = "0101") then
            display <= "0100100";
        elsif(bcd = "0110") then
            display <= "0100000";
        elsif(bcd = "0111") then
            display <= "0001111";
        elsif(bcd = "1000") then
            display <= "0000000";
        elsif(bcd = "1001") then
            display <= "0000110";
        else
            display <= "1111111";
        end if;
     end process;
end acod2;
```

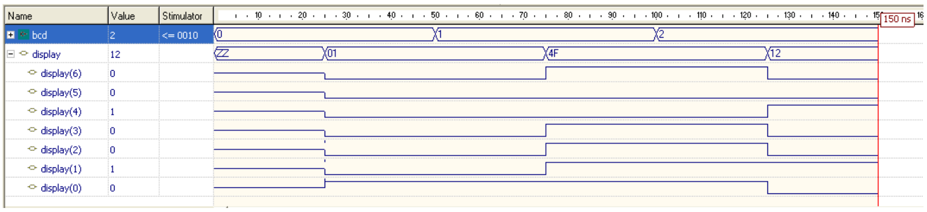
Simulación en Galaxy



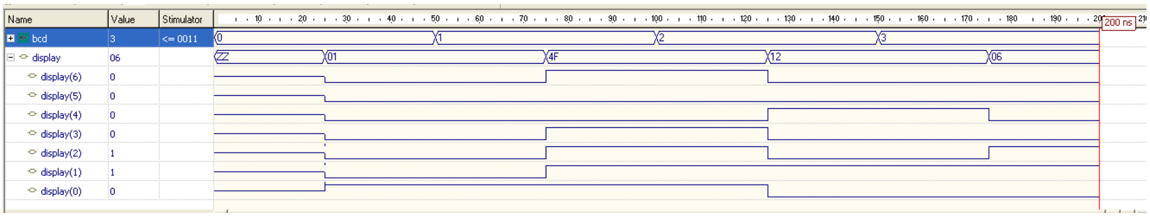
Name	Value	Stimulator
bcd	0	<= 0000
display	01	
display(6)	0	
display(5)	0	
display(4)	0	
display(3)	0	
display(2)	0	
display(1)	0	
display(0)	1	



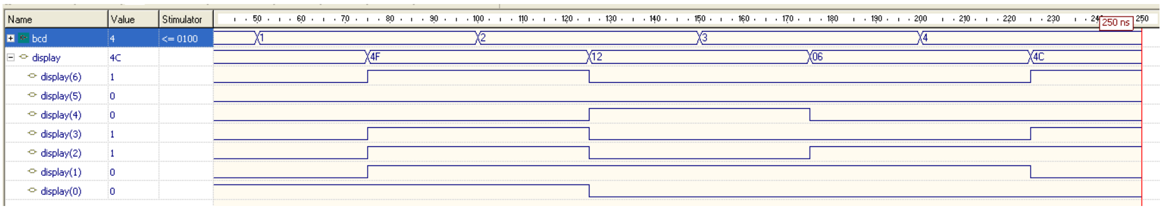
Name	Value	Stimulator
bcd	1	<= 0001
display	4F	
display(6)	1	
display(5)	0	
display(4)	0	
display(3)	1	
display(2)	1	
display(1)	1	
display(0)	1	



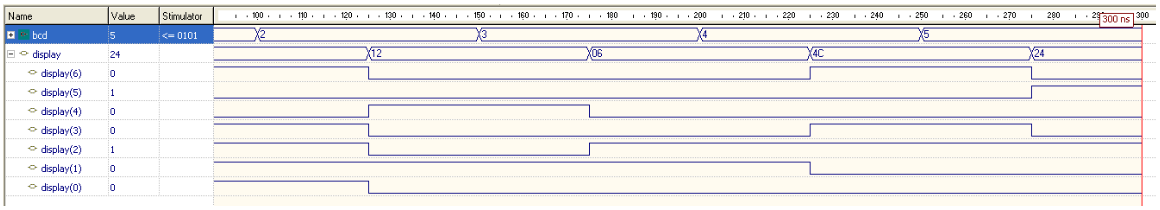
Name	Value	Stimulator
bcd	2	<= 0010
display	12	
display(6)	0	
display(5)	0	
display(4)	1	
display(3)	0	
display(2)	0	
display(1)	1	
display(0)	0	



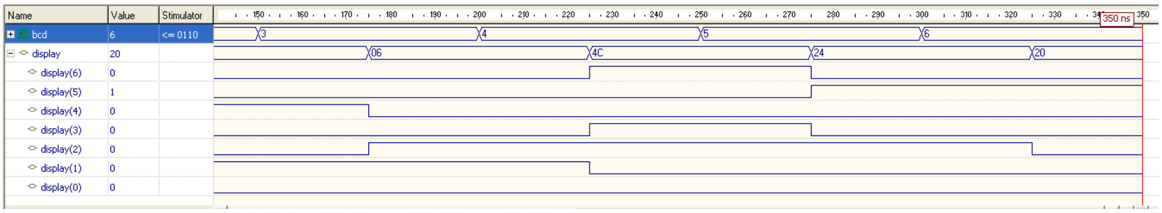
Name	Value	Stimulator
bcd	3	<= 0011
display	06	
display(6)	0	
display(5)	0	
display(4)	0	
display(3)	0	
display(2)	1	
display(1)	1	
display(0)	0	



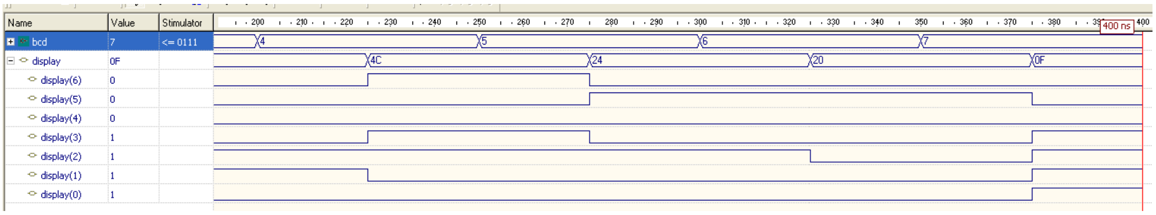
Name	Value	Stimulator
bcd	4	<= 0100
display	4C	
display(6)	1	
display(5)	0	
display(4)	0	
display(3)	1	
display(2)	1	
display(1)	0	
display(0)	0	



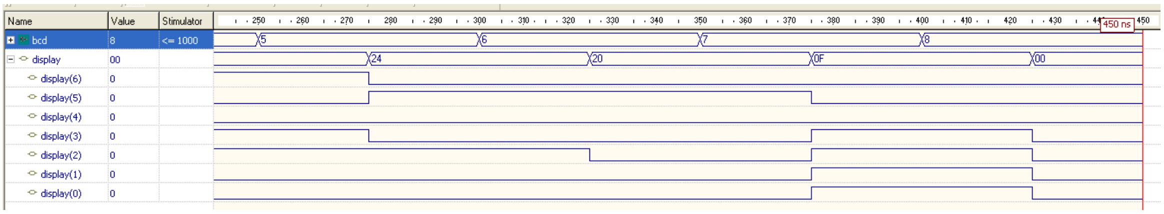
Name	Value	Stimulator
bcd	5	<= 0101
display	24	
display(6)	0	
display(5)	1	
display(4)	0	
display(3)	0	
display(2)	1	
display(1)	0	
display(0)	0	



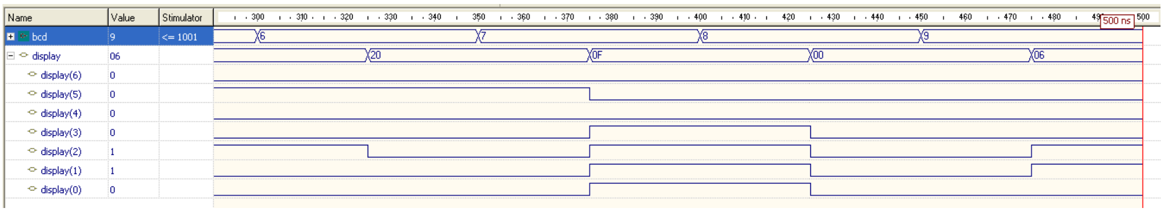
Name	Value	Stimulator
bcd	6	<= 0110
display	20	
display(6)	0	
display(5)	1	
display(4)	0	
display(3)	0	
display(2)	0	
display(1)	0	
display(0)	0	



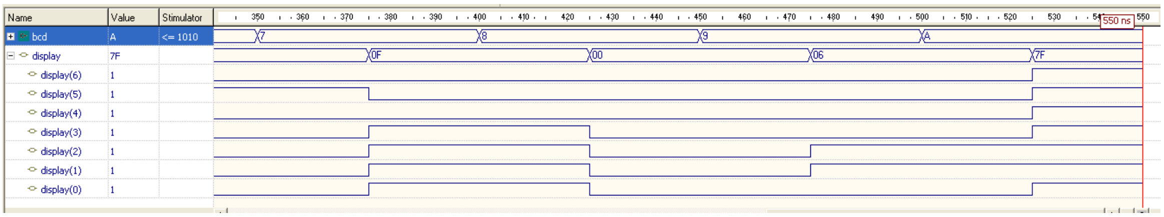
Name	Value	Stimulator
bcd	7	<= 0111
display	0F	
display(6)	0	
display(5)	0	
display(4)	0	
display(3)	1	
display(2)	1	
display(1)	1	
display(0)	1	



Name	Value	Stimulator
bcd	8	<= 1000
display	00	
display(6)	0	
display(5)	0	
display(4)	0	
display(3)	0	
display(2)	0	
display(1)	0	
display(0)	0	

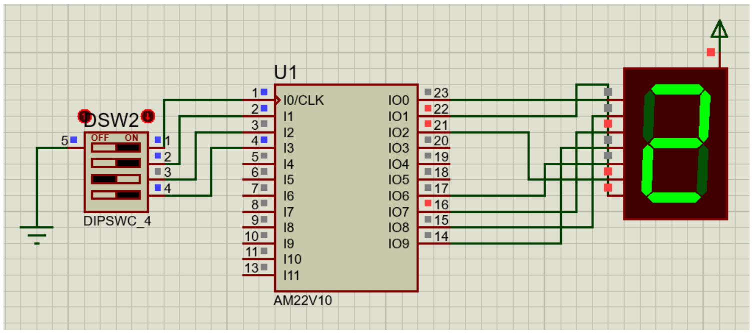


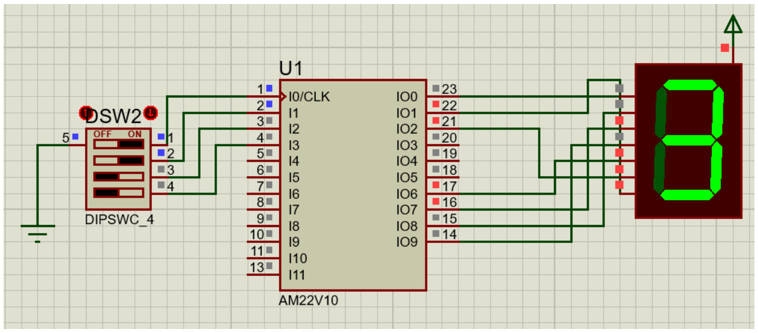
Name	Value	Stimulator
bcd	9	<= 1001
display	06	
display(6)	0	
display(5)	0	
display(4)	0	
display(3)	0	
display(2)	1	
display(1)	1	
display(0)	0	



Name	Value	Stimulator
bcd	A	<= 1010
display	7F	
display(6)	1	
display(5)	1	
display(4)	1	
display(3)	1	
display(2)	1	
display(1)	1	
display(0)	1	

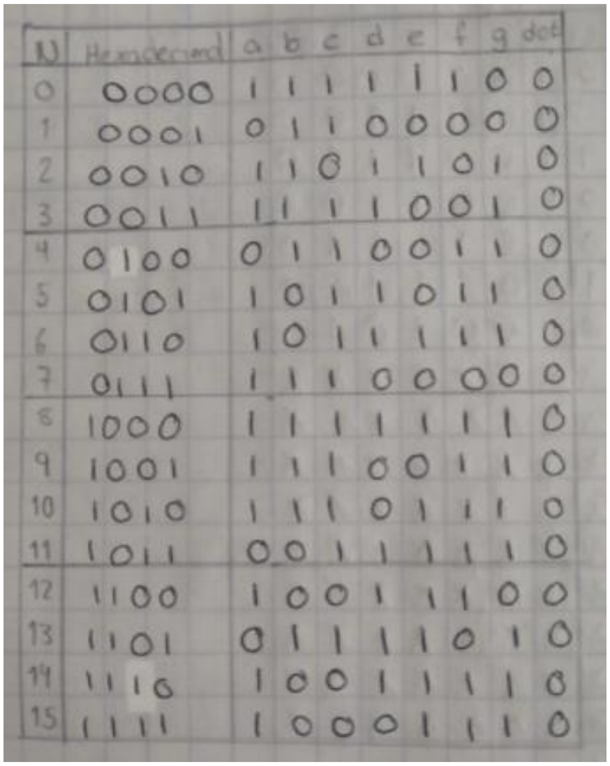
Simulación de 2 casos en Proteus





c) Hexadecimal a display de 7 segmentos de cátodo común

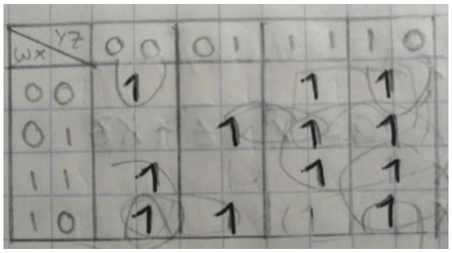
Tabla de verdad



N	Hexadecimal	a	b	c	d	e	f	g	dot
0	0000	1	1	1	1	1	1	0	0
1	0001	0	1	1	0	0	0	0	0
2	0010	1	1	0	1	1	0	1	0
3	0011	1	1	1	1	0	0	1	0
4	0100	0	1	1	0	0	1	1	0
5	0101	1	0	1	1	0	1	1	0
6	0110	1	0	1	1	1	1	1	0
7	0111	1	1	1	0	0	0	0	0
8	1000	1	1	1	1	1	1	1	0
9	1001	1	1	1	0	0	1	1	0
10	1010	1	1	1	0	1	1	1	0
11	1011	0	0	1	1	1	1	1	0
12	1100	1	0	0	1	1	1	0	0
13	1101	0	1	1	1	1	0	1	0
14	1110	1	0	0	1	1	1	1	0
15	1111	1	0	0	0	1	1	1	0

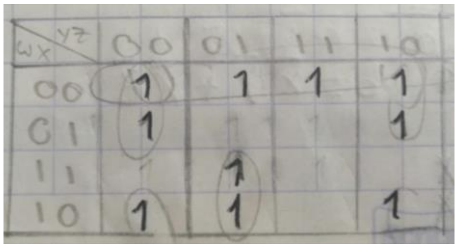
Mapas de Karnaugh

a)



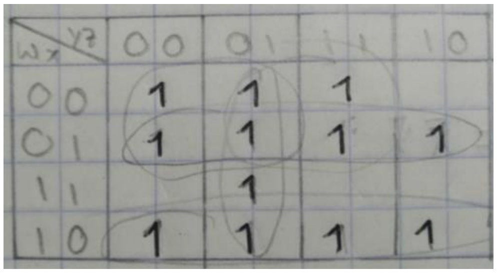
wx \ yz	00	01	11	10
00	1		1	1
01		1	1	1
11	1		1	1
10	1	1		1

b)



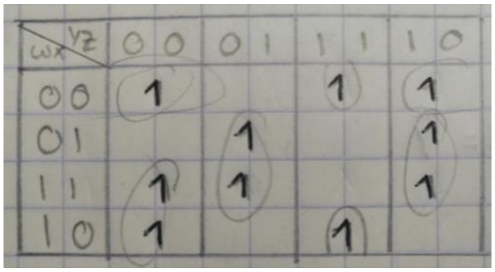
wx \ yz	00	01	11	10
00	1	1	1	1
01	1			1
11		1		
10	1	1		1

c)



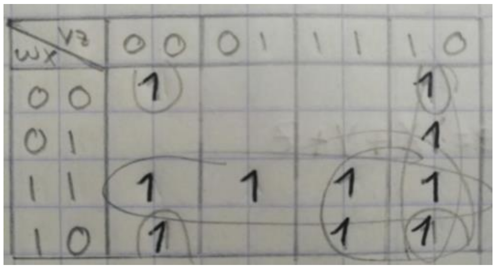
wx \ yz	00	01	11	10
00	1	1	1	
01	1	1	1	1
11		1		
10	1	1	1	1

d)



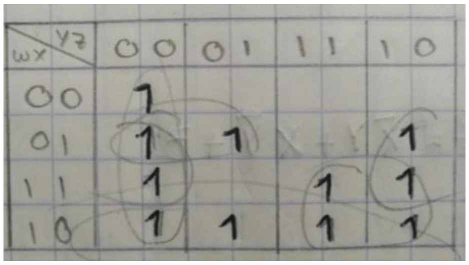
wx \ yz	00	01	11	10
00	1		1	1
01		1		1
11	1	1		1
10	1		1	

e)



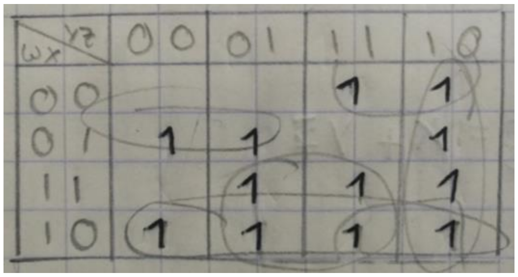
wx \ yz	00	01	11	10
00	1			1
01				1
11	1	1	1	1
10	1		1	1

f)



wx \ yz	00	01	11	10
00	1			
01	1	1		1
11	1		1	1
10	1	1	1	1

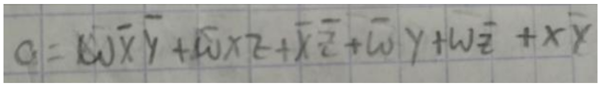
g)



wx \ yz	00	01	11	10
00			1	1
01	1	1		1
11		1	1	1
10	1	1	1	1

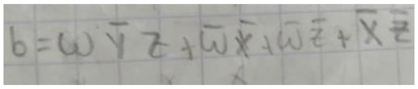
Ecuaciones de salida

a)



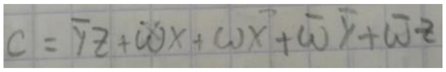
$a = w\bar{x}\bar{y} + \bar{w}xz + \bar{x}\bar{z} + \bar{w}y + w\bar{z} + x\bar{y}$

b)



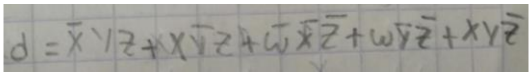
$b = w\bar{y}z + \bar{w}\bar{x} + \bar{w}\bar{z} + \bar{x}\bar{z}$

c)



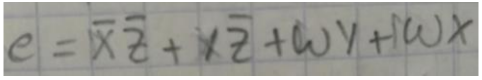
$c = \bar{y}z + \bar{w}x + w\bar{x} + \bar{w}\bar{y} + \bar{w}z$

d)



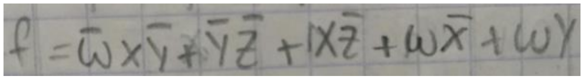
$d = \bar{x}yz + x\bar{y}z + \bar{w}\bar{x}\bar{z} + w\bar{y}\bar{z} + xy\bar{z}$

e)



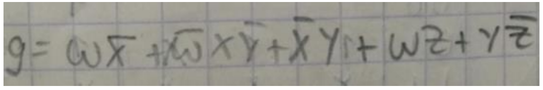
$e = \bar{x}\bar{z} + x\bar{z} + wy + wx$

f)



$f = \bar{w}x\bar{y} + \bar{y}\bar{z} + x\bar{z} + w\bar{x} + wy$

g)

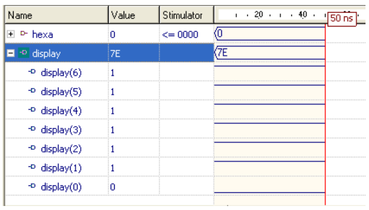


$g = w\bar{x} + \bar{w}x\bar{y} + \bar{x}y + wz + y\bar{z}$

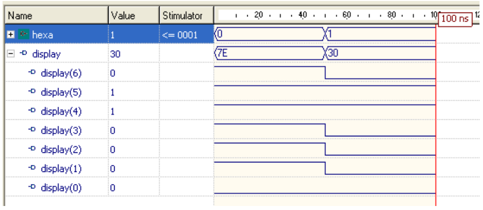
Código en VHDL

```
library ieee;
use ieee.std_logic_1164.all;
entity cod3 is
port(
        hexa : in std_logic_vector(3 downto 0);
        display : out std_logic_vector(6 downto 0)
);
end cod3;

architecture acod3 of cod3 is
begin
        process(hexa)
        begin
                case hexa is
                        when "0000" => display <= "1111110";
                        when "0001" => display <= "0110000";
                        when "0010" => display <= "1101101";
                        when "0011" => display <= "1111001";
                        when "0100" => display <= "0110011";
                        when "0101" => display <= "1011011";
                        when "0110" => display <= "1011111";
                        when "0111" => display <= "1110000";
                        when "1000" => display <= "1111111";
                        when "1001" => display <= "1110011";
                        when "1010" => display <= "1110111";
                        when "1011" => display <= "0011111";
                        when "1100" => display <= "1001110";
                        when "1101" => display <= "0111101";
                        when "1110" => display <= "1001111";
                        when "1111" => display <= "1000111";
                        when others => display <= "0000000";
                end case;
        end process;
end acod3;
```

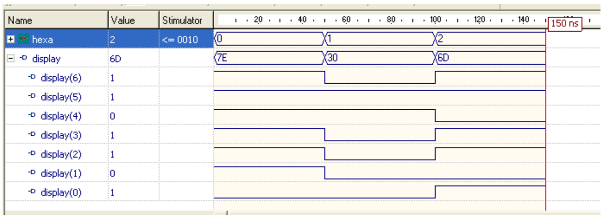
Simulación en Galaxy



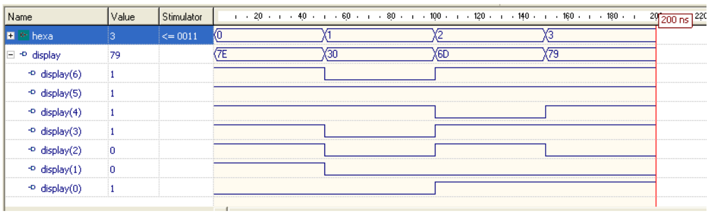
Name	Value	Stimulator
hexa	0	<= 0000
display	7E	
display(6)	1	
display(5)	1	
display(4)	1	
display(3)	1	
display(2)	1	
display(1)	1	
display(0)	0	



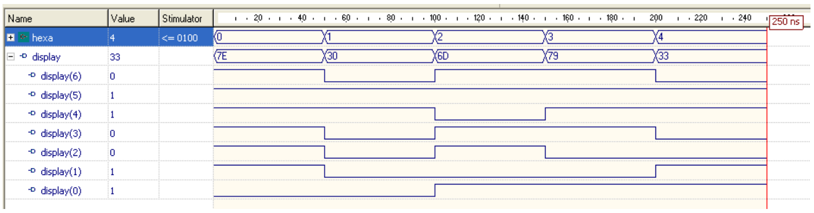
Name	Value	Stimulator
hexa	1	<= 0001
display	30	
display(6)	0	
display(5)	1	
display(4)	1	
display(3)	0	
display(2)	0	
display(1)	0	
display(0)	0	



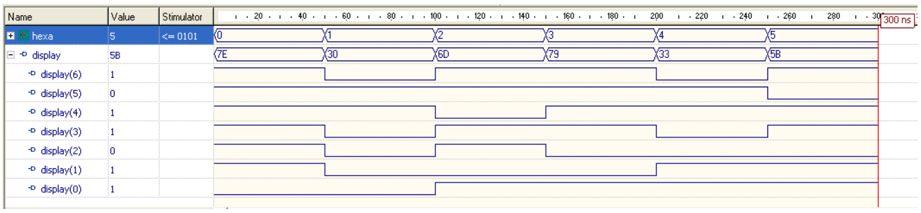
Name	Value	Stimulator
hexa	2	<= 0010
display	6D	
display(6)	1	
display(5)	1	
display(4)	0	
display(3)	1	
display(2)	1	
display(1)	0	
display(0)	1	



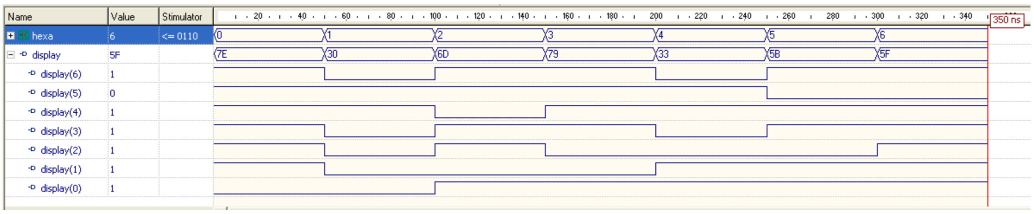
Name	Value	Stimulator
hexa	3	<= 0011
display	79	
display(6)	1	
display(5)	1	
display(4)	1	
display(3)	1	
display(2)	0	
display(1)	0	
display(0)	1	



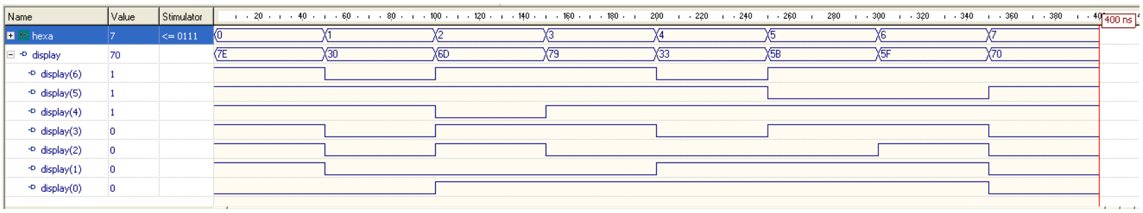
Name	Value	Stimulator
hexa	4	<= 0100
display	33	
display(6)	0	
display(5)	1	
display(4)	1	
display(3)	0	
display(2)	0	
display(1)	1	
display(0)	1	



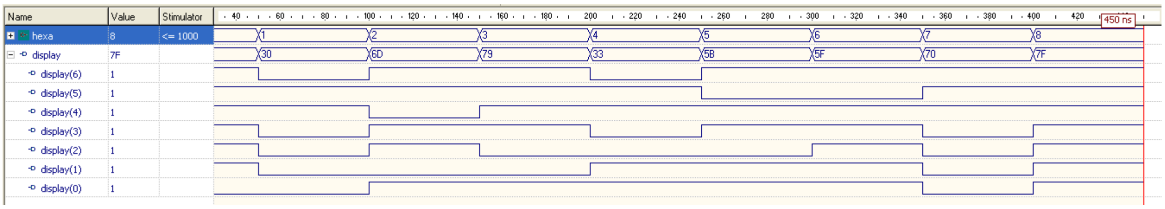
Name	Value	Stimulator
hexa	5	<= 0101
display	5B	
display(6)	1	
display(5)	0	
display(4)	1	
display(3)	1	
display(2)	0	
display(1)	1	
display(0)	1	



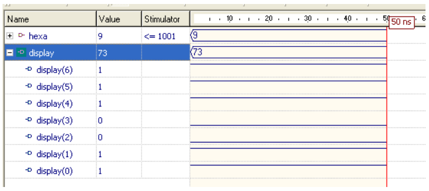
Name	Value	Stimulator
hexa	6	<= 0110
display	5F	
display(6)	1	
display(5)	0	
display(4)	1	
display(3)	1	
display(2)	1	
display(1)	1	
display(0)	1	



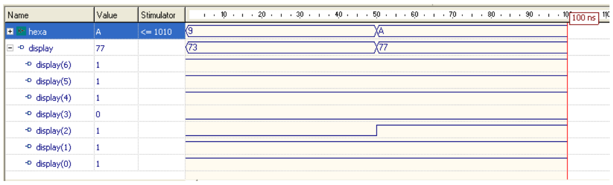
Name	Value	Stimulator
hexa	7	<= 0111
display	70	
display(6)	1	
display(5)	1	
display(4)	1	
display(3)	0	
display(2)	0	
display(1)	0	
display(0)	0	



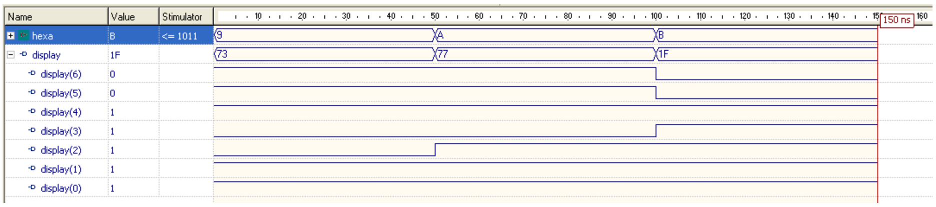
Name	Value	Stimulator
hexa	8	<= 1000
display	7F	
display(6)	1	
display(5)	1	
display(4)	1	
display(3)	1	
display(2)	1	
display(1)	1	
display(0)	1	



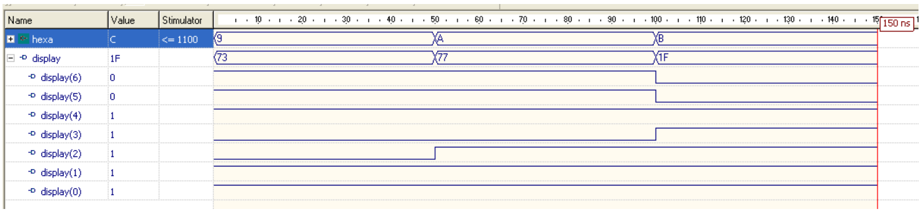
Name	Value	Stimulator
hexa	9	<= 1001
display	73	
display(6)	1	
display(5)	1	
display(4)	1	
display(3)	0	
display(2)	0	
display(1)	1	
display(0)	1	



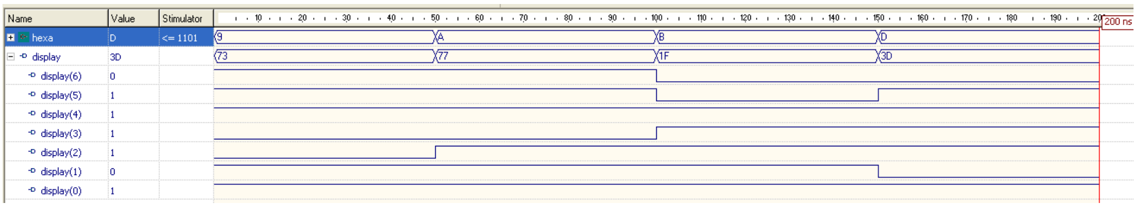
Name	Value	Stimulator
hexa	A	<= 1010
display	77	
display(6)	1	
display(5)	1	
display(4)	1	
display(3)	0	
display(2)	1	
display(1)	1	
display(0)	1	



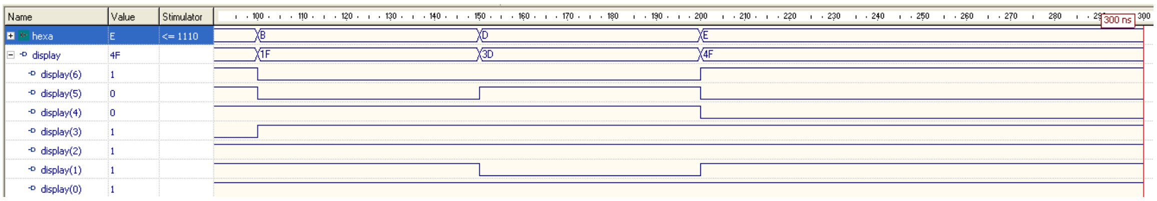
Name	Value	Stimulator
hexa	B	<= 1011
display	1F	
display(6)	0	
display(5)	0	
display(4)	1	
display(3)	1	
display(2)	1	
display(1)	1	
display(0)	1	



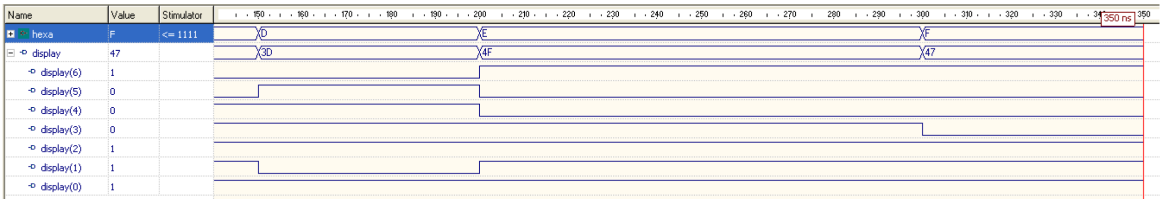
Name	Value	Stimulator
hexa	C	<= 1100
display	1F	
display(6)	0	
display(5)	0	
display(4)	1	
display(3)	1	
display(2)	1	
display(1)	1	
display(0)	1	



Name	Value	Stimulator
hexa	D	<= 1101
display	3D	
display(6)	0	
display(5)	1	
display(4)	1	
display(3)	1	
display(2)	1	
display(1)	0	
display(0)	1	

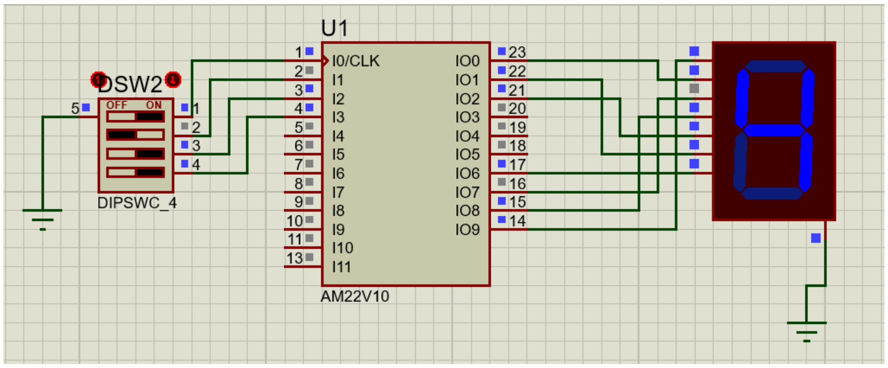


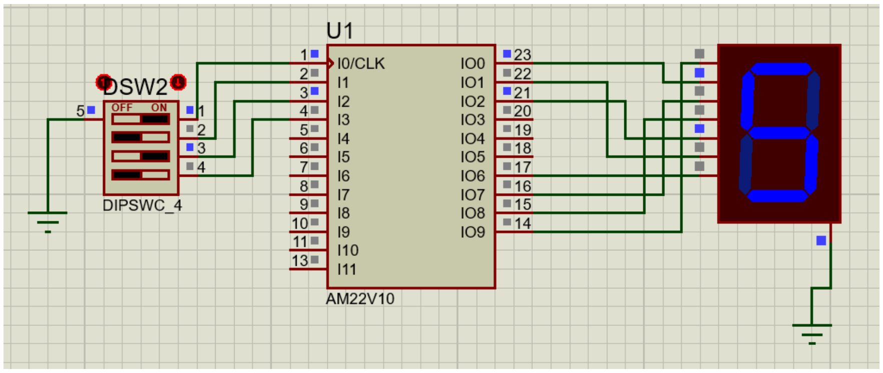
Name	Value	Stimulator
hexa	E	<= 1110
display	4F	
display(6)	1	
display(5)	0	
display(4)	0	
display(3)	1	
display(2)	1	
display(1)	1	
display(0)	1	



Name	Value	Stimulator
hexa	F	<= 1111
display	47	
display(6)	1	
display(5)	0	
display(4)	0	
display(3)	0	
display(2)	1	
display(1)	1	
display(0)	1	

Simulación de 2 casos en Proteus

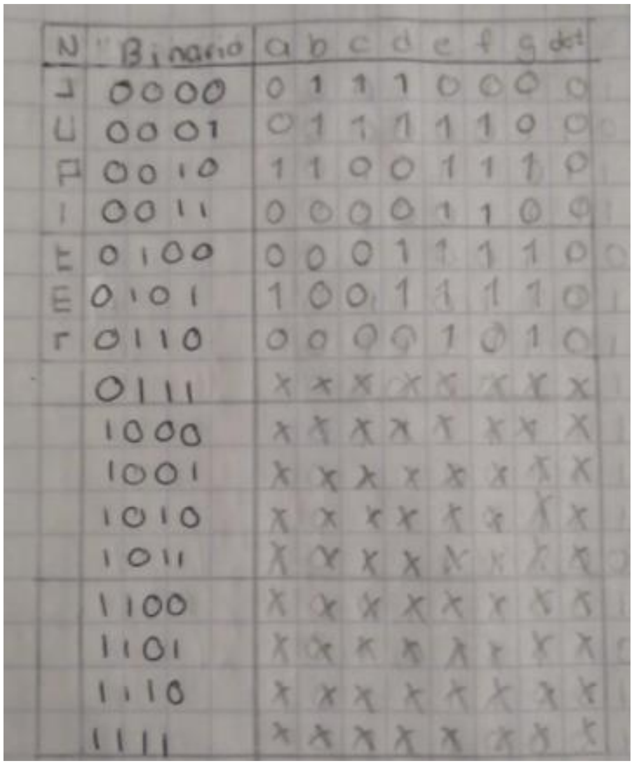




d) Binario a 7 segmentos de cátodo común

Palabra = Jupiter

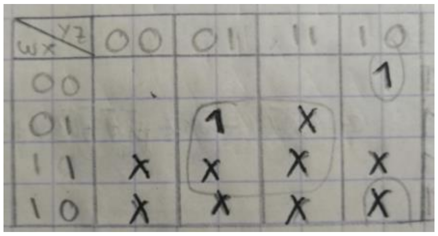
Tabla de verdad



N	Binario	a	b	c	d	e	f	g	dot
J	0000	0	1	1	1	0	0	0	0
U	0001	0	1	1	1	1	1	0	0
P	0010	1	1	0	0	1	1	1	0
I	0011	0	0	0	0	1	1	0	0
t	0100	0	0	0	1	1	1	1	0
E	0101	1	0	0	1	1	1	1	0
r	0110	0	0	0	0	1	0	1	0
	0111	X	X	X	X	X	X	X	X
	1000	X	X	X	X	X	X	X	X
	1001	X	X	X	X	X	X	X	X
	1010	X	X	X	X	X	X	X	X
	1011	X	X	X	X	X	X	X	X
	1100	X	X	X	X	X	X	X	X
	1101	X	X	X	X	X	X	X	X
	1110	X	X	X	X	X	X	X	X
	1111	X	X	X	X	X	X	X	X

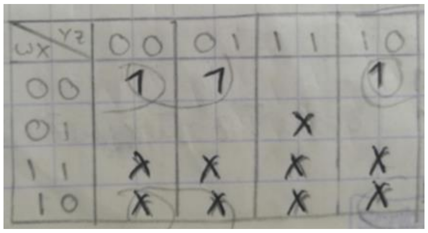
Mapas de Karnaugh

a)



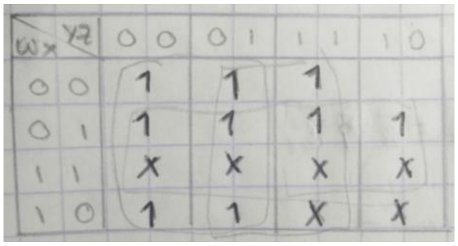
wx\yz	00	01	11	10
00				1
01		1	X	
11	X	X	X	X
10	X	X	X	X

b)



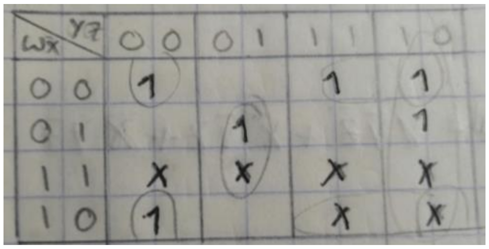
wx\yz	00	01	11	10
00	1	1		1
01			X	
11	X	X	X	X
10	X	X	X	X

c)



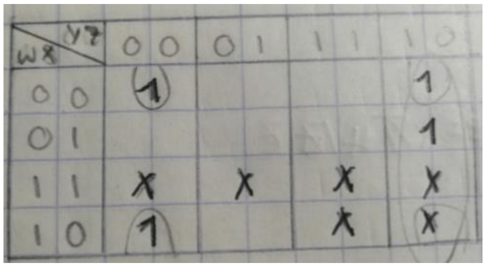
wx\yz	00	01	11	10
00	1	1	1	
01	1	1	1	1
11	X	X	X	X
10	1	1	X	X

d)



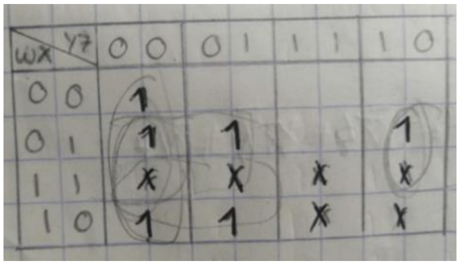
wx\yz	00	01	11	10
00	1		1	1
01		1		1
11	X	X	X	X
10	1		X	X

e)



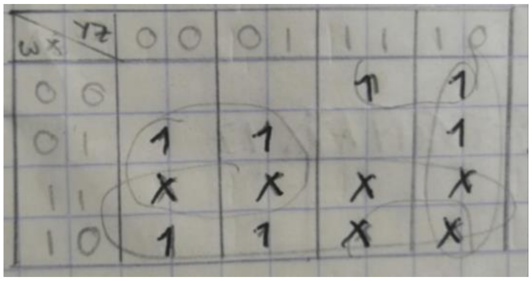
wx \ yz	00	01	11	10
00	1			1
01				1
11	X	X	X	X
10	1		X	X

f)



wx \ yz	00	01	11	10
00	1			
01	1	1		1
11	X	X	X	X
10	1	1	X	X

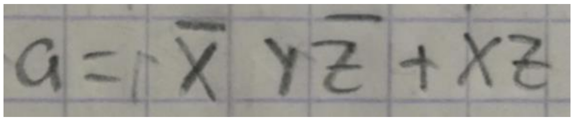
g)



wx \ yz	00	01	11	10
00			1	1
01	1	1		1
11	X	X	X	X
10	1	1	X	X

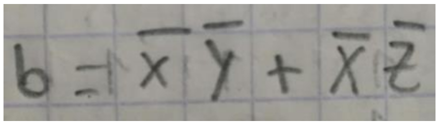
Ecuaciones de salida

a)



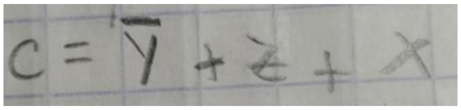
$a = \bar{X} Y \bar{Z} + XZ$

b)



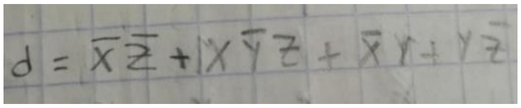
$b = \bar{x}\bar{y} + \bar{x}\bar{z}$

c)



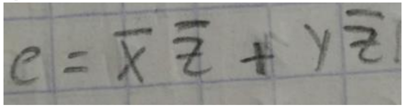
$c = \bar{y} + z + x$

d)



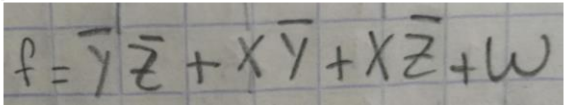
$d = \bar{x}\bar{z} + x\bar{y}z + \bar{x}y + y\bar{z}$

e)



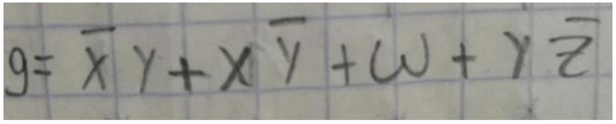
$e = \bar{x}\bar{z} + y\bar{z}$

f)



$f = \bar{y}\bar{z} + x\bar{y} + x\bar{z} + w$

g)

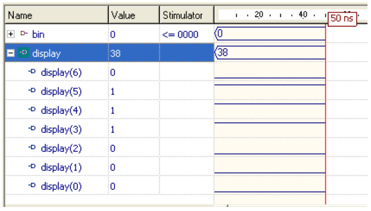


$g = \bar{x}y + x\bar{y} + w + y\bar{z}$

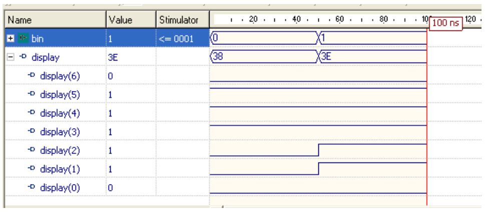
Código en VHDL

```
library ieee;
use ieee.std_logic_1164.all;

entity cod4 is
port(

        bin : in std_logic_vector(3 downto 0);
        display : out std_logic_vector(6 downto 0)
);
end cod4;
architecture acod4 of cod4 is
begin
        with bin select display <=
                "0111000" when "0000",
                "0111110" when "0001",
                "1100111" when "0010",
                "0000110" when "0011",
                "0001111" when "0100",
                "1001111" when "0101",
                "0000101" when "0110",
                "0000000" when others;
end acod4;
```

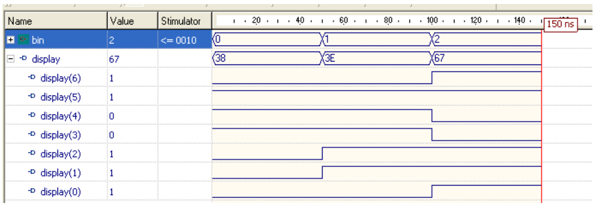
Simulación en Galaxy



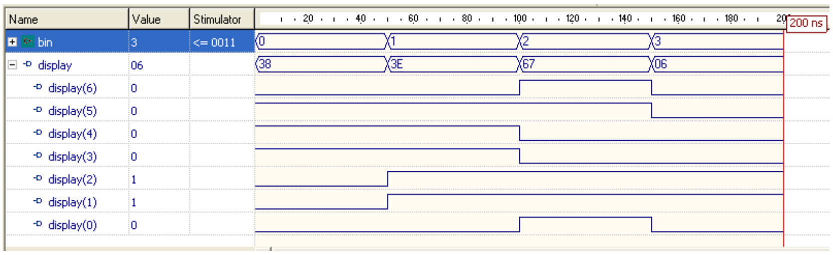
Name	Value	Stimulator
bin	0	<= 0000
display	38	
display(6)	0	
display(5)	1	
display(4)	1	
display(3)	1	
display(2)	0	
display(1)	0	
display(0)	0	



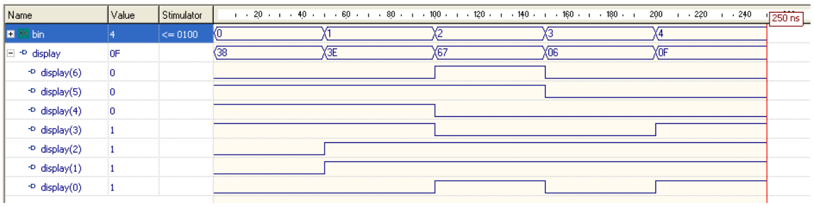
Name	Value	Stimulator
bin	1	<= 0001
display	3E	
display(6)	0	
display(5)	1	
display(4)	1	
display(3)	1	
display(2)	1	
display(1)	1	
display(0)	0	



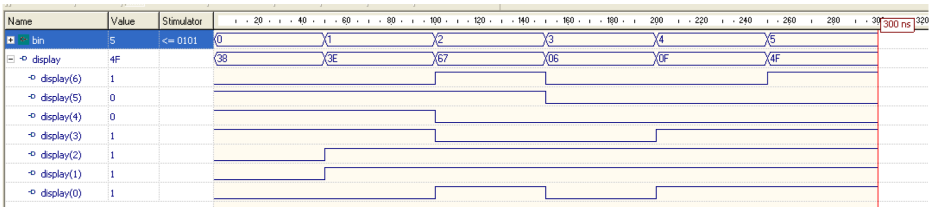
Name	Value	Stimulator
bin	2	<= 0010
display	67	
display(6)	1	
display(5)	1	
display(4)	0	
display(3)	0	
display(2)	1	
display(1)	1	
display(0)	1	



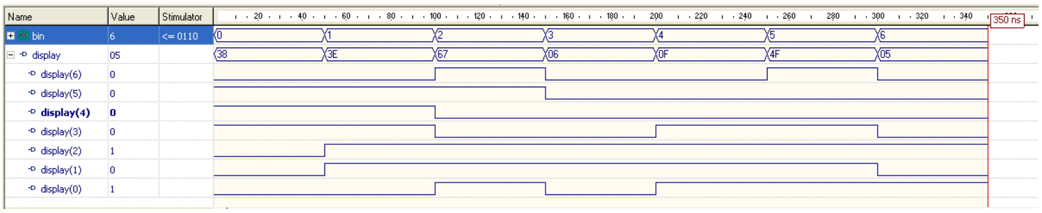
Name	Value	Stimulator
bin	3	<= 0011
display	06	
display(6)	0	
display(5)	0	
display(4)	0	
display(3)	0	
display(2)	1	
display(1)	1	
display(0)	0	



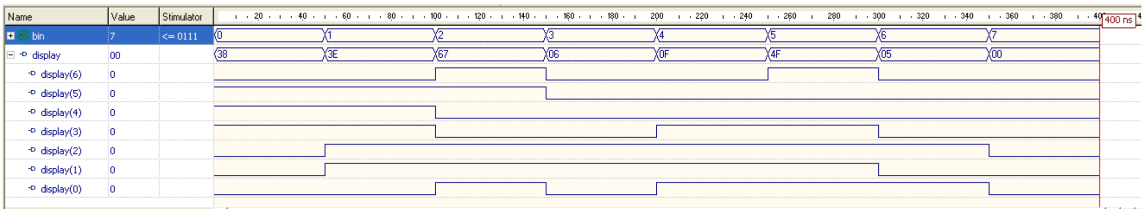
Name	Value	Stimulator
bin	4	<= 0100
display	0F	
display(6)	0	
display(5)	0	
display(4)	0	
display(3)	1	
display(2)	1	
display(1)	1	
display(0)	1	



Name	Value	Stimulator
bin	5	<= 0101
display	4F	
display(6)	1	
display(5)	0	
display(4)	0	
display(3)	1	
display(2)	1	
display(1)	1	
display(0)	1	

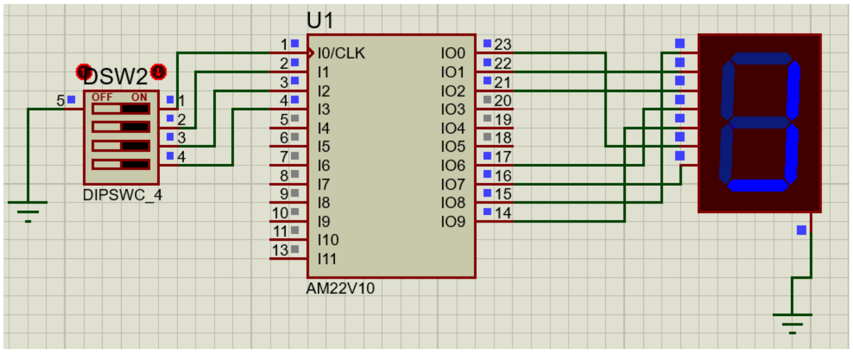


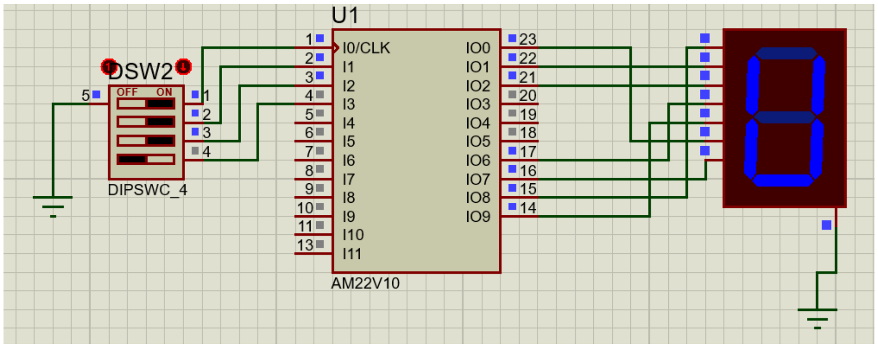
Name	Value	Stimulator
bin	6	<= 0110
display	05	
display(6)	0	
display(5)	0	
display(4)	**0**	
display(3)	0	
display(2)	1	
display(1)	0	
display(0)	1	

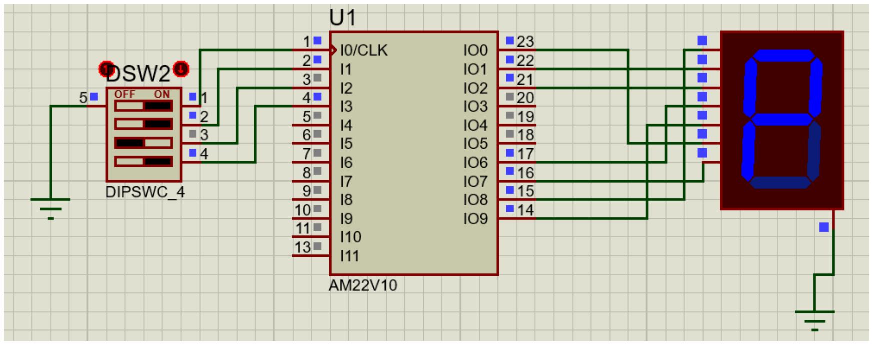


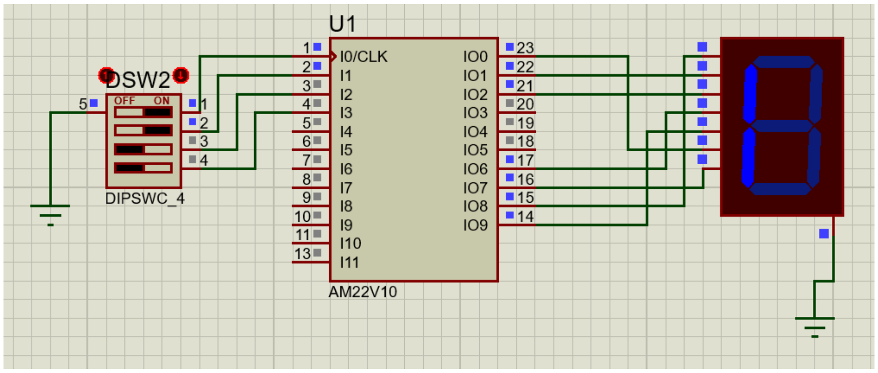
Name	Value	Stimulator
bin	7	<= 0111
display	00	
display(6)	0	
display(5)	0	
display(4)	0	
display(3)	0	
display(2)	0	
display(1)	0	
display(0)	0	

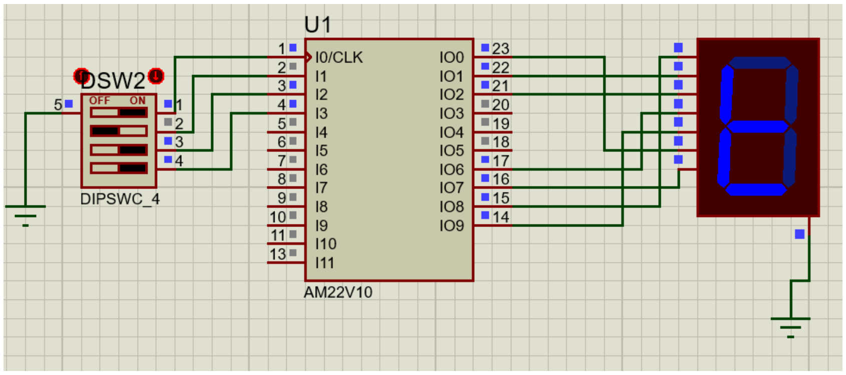
Simulación en Proteus

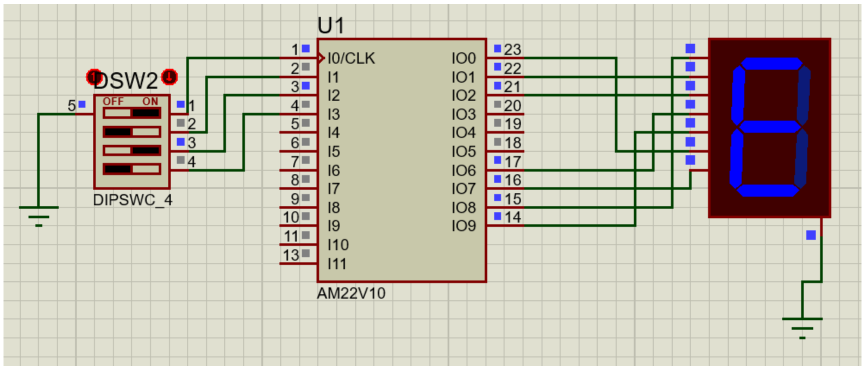


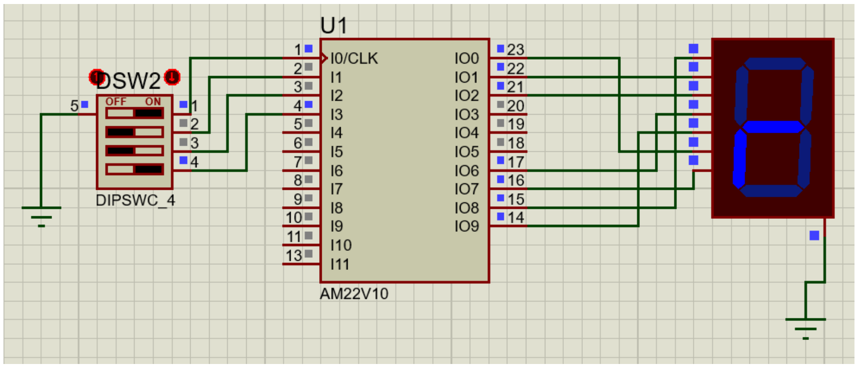

U1
DSW2
OFF
ON
DIPSWC_4
5
1
2
3
4
I0/CLK
I1
I2
I3
I4
I5
I6
I7
I8
I9
I10
I11
5
6
7
8
9
10
11
13
IO0
IO1
IO2
IO3
IO4
IO5
IO6
IO7
IO8
IO9
23
22
21
20
19
18
17
16
15
14
AM22V10


U1
DSW2
OFF
ON
DIPSWC_4
5
1
2
3
4
I0/CLK
I1
I2
I3
I4
I5
I6
I7
I8
I9
I10
I11
5
6
7
8
9
10
11
13
IO0
IO1
IO2
IO3
IO4
IO5
IO6
IO7
IO8
IO9
23
22
21
20
19
18
17
16
15
14
AM22V10


U1
DSW2
OFF
ON
DIPSWC_4
5
1
2
3
4
I0/CLK
I1
I2
I3
I4
I5
I6
I7
I8
I9
I10
I11
5
6
7
8
9
10
11
13
IO0
IO1
IO2
IO3
IO4
IO5
IO6
IO7
IO8
IO9
23
22
21
20
19
18
17
16
15
14
AM22V10


U1
DSW2
OFF
ON
DIPSWC_4
5
1
2
3
4
I0/CLK
I1
I2
I3
I4
I5
I6
I7
I8
I9
I10
I11
5
6
7
8
9
10
11
13
IO0
IO1
IO2
IO3
IO4
IO5
IO6
IO7
IO8
IO9
23
22
21
20
19
18
17
16
15
14
AM22V10


U1
DSW2
OFF
ON
5
1
2
3
4
DIPSWC_4
1 I0/CLK
2 I1
3 I2
4 I3
5 I4
6 I5
7 I6
8 I7
9 I8
10 I9
11 I10
13 I11
IO0 23
IO1 22
IO2 21
IO3 20
IO4 19
IO5 18
IO6 17
IO7 16
IO8 15
IO9 14
AM22V10


U1
DSW2
OFF
ON
5
1
2
3
4
DIPSWC_4
1 I0/CLK
2 I1
3 I2
4 I3
5 I4
6 I5
7 I6
8 I7
9 I8
10 I9
11 I10
13 I11
IO0 23
IO1 22
IO2 21
IO3 20
IO4 19
IO5 18
IO6 17
IO7 16
IO8 15
IO9 14
AM22V10