Práctica 12: Multiplexor Y Demultiplexor

Nombre: Colín Ramiro Joel No. de lista: 3

- Tabla

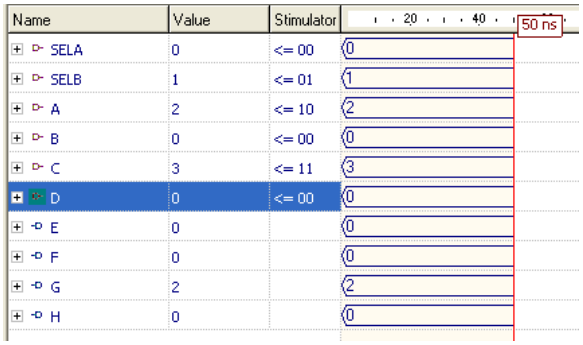
a	b	c	d	selA	selB	e	f	g	h
2	0	3	0	0	1	0	0	2	0
1	1	1	1	2	3	1	0	0	0
0	2	2	3	1	1	0	0	2	0
1	3	0	2	1	3	3	0	0	0
3	2	1	0	3	0	0	0	0	0

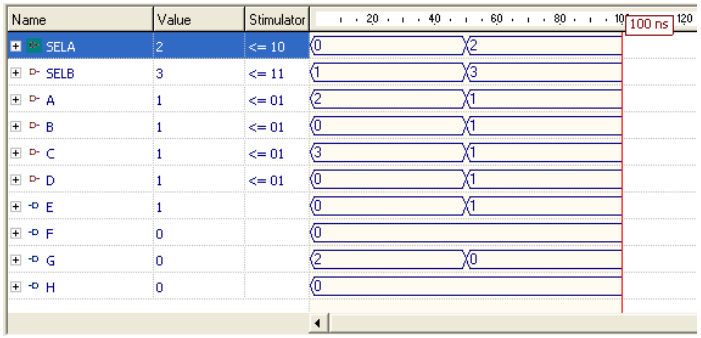
- Código en VHDL

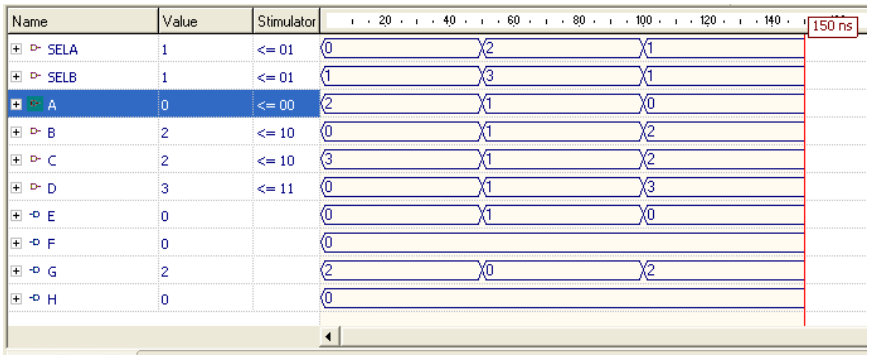
```
library ieee;
use ieee.std_logic_1164.all;
entity prac12 is
port(
	A,B,C,D: in std_logic_vector(1 downto 0);
	SELA,SELB: in std_logic_vector(1 downto 0);
	E,F,G,H: out std_logic_vector(1 downto 0)
);
end prac12;

architecture aprac12 of prac12 is

signal aux: std_logic_vector(1 downto 0);
begin
	process(A,B,C,D,SELA)
	begin
		case SELA is
			when "00" => AUX <=A;
			when "01" => AUX <=B;
			when "10" => AUX <=C;
			when others => AUX <=D;
	  end case;
	end process;
	process(AUX,SELB)
	begin
		E <= "00";
		F <= "00";
		G <= "00";
		H <= "00";
```

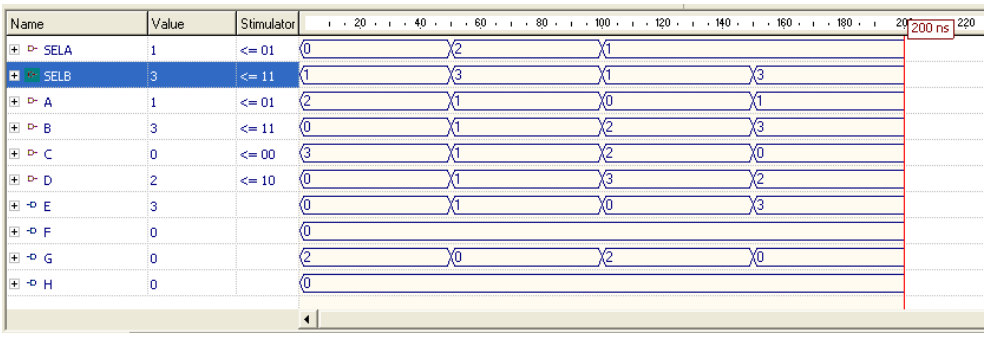
```
                if(SELB = "00")then
                        H <= AUX;
                elsif(SELB = "01")then
                        G <= AUX;
                elsif(SELB = "10")then
                        F <= AUX;
                else
                        E <= AUX;
                end if;
        end process;
end aprac12;
```

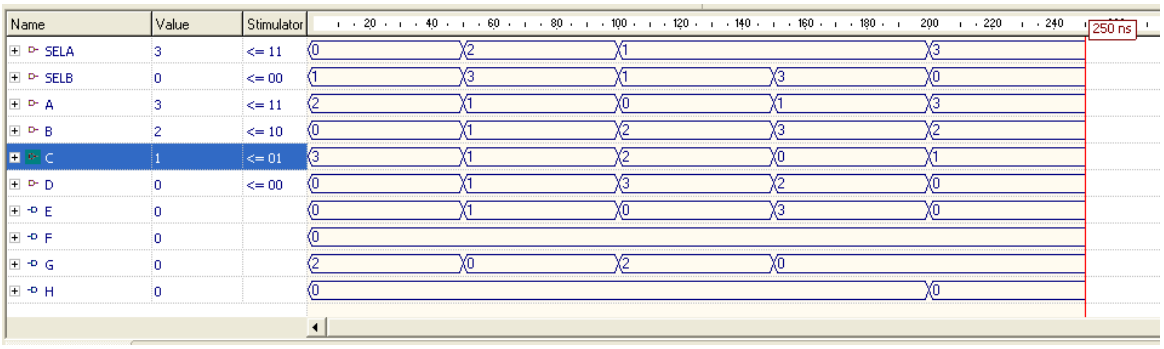
- **Simulación en VHDL**



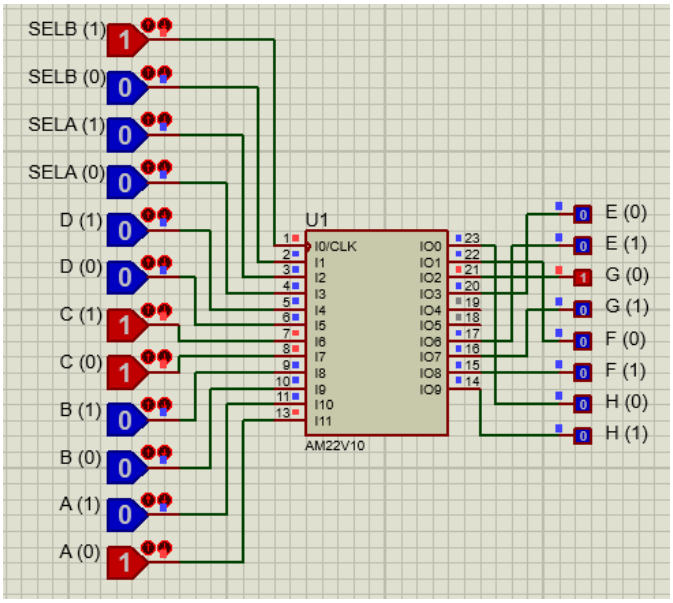


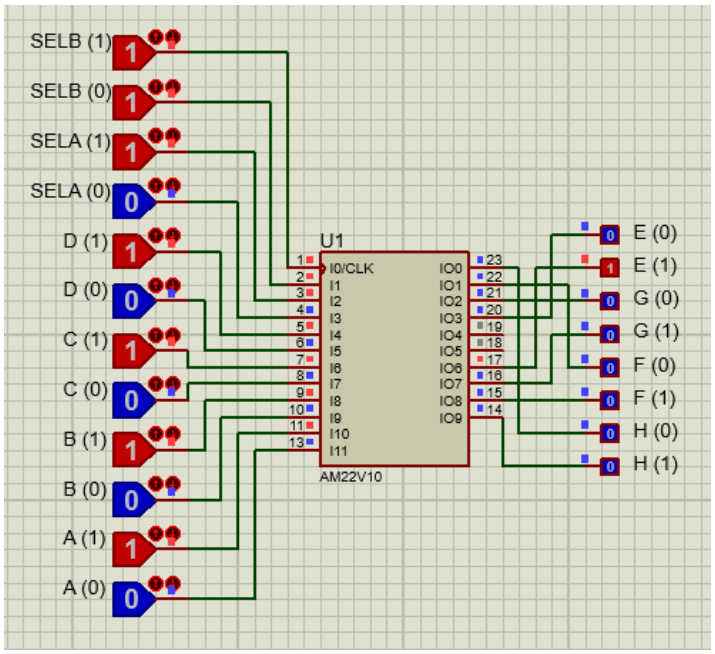


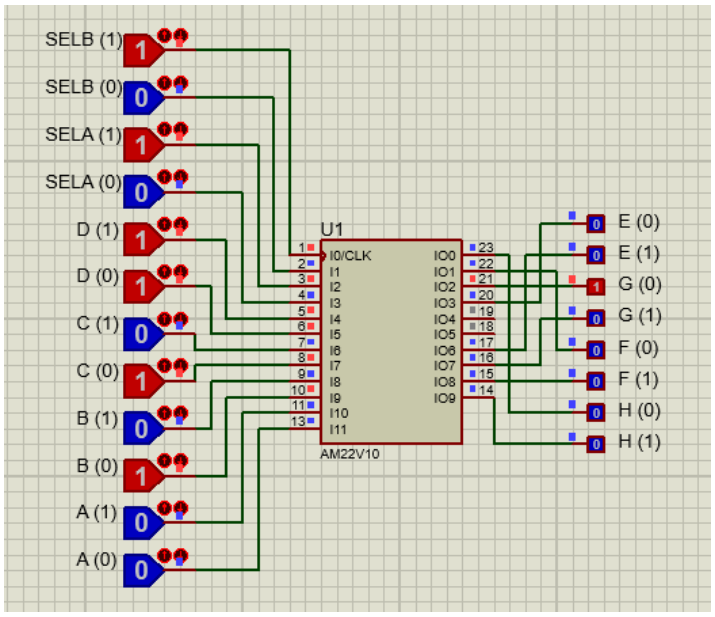




- **Simulación en Proteus**




SELB (1)
SELB (0)
SELA (1)
SELA (0)
D (1)
D (0)
C (1)
C (0)
B (1)
B (0)
A (1)
A (0)
U1
I0/CLK
I1
I2
I3
I4
I5
I6
I7
I8
I9
I10
I11
IO0
IO1
IO2
IO3
IO4
IO5
IO6
IO7
IO8
IO9
AM22V10
E (0)
E (1)
G (0)
G (1)
F (0)
F (1)
H (0)
H (1)


SELB (1)
SELB (0)
SELA (1)
SELA (0)
D (1)
D (0)
C (1)
C (0)
B (1)
B (0)
A (1)
A (0)
U1
I0/CLK
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AM22V10
E (0)
E (1)
G (0)
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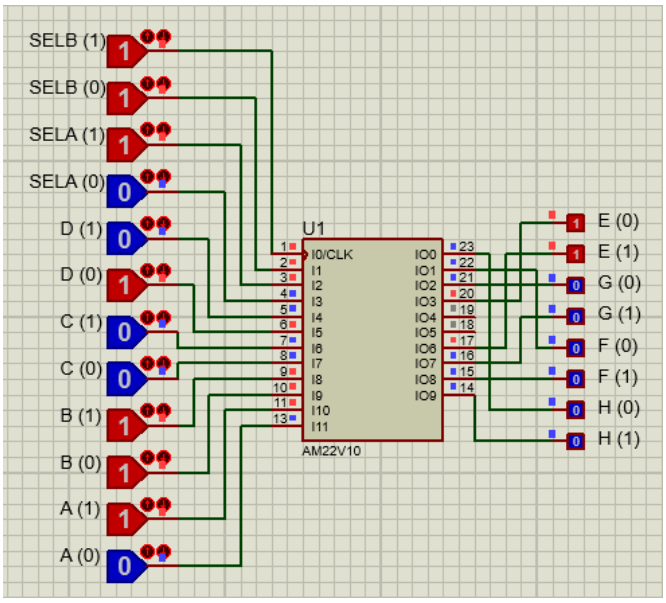
SELB (1)
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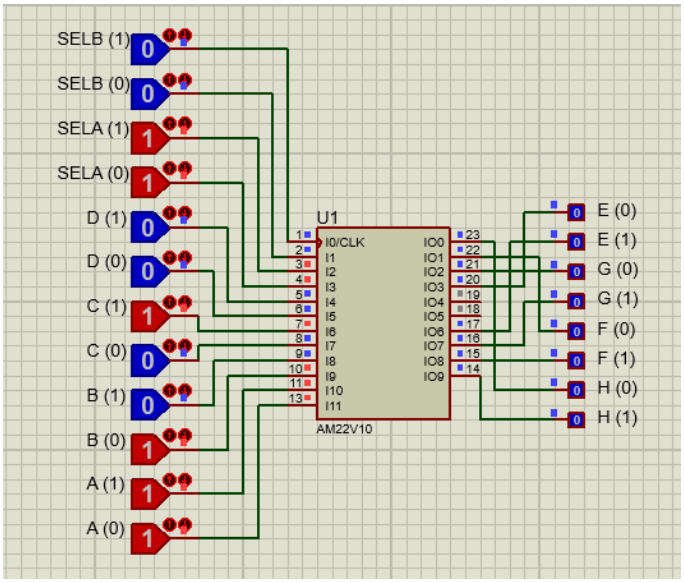
H (0)
H (1)


SELB (1)
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SELA (0)
D (1)
D (0)
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A (0)
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IO9
AM22V10
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E (1)
G (0)
G (1)
F (0)
F (1)
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H (1)