Práctica 11: Multiplexor

Nombre: Colín Ramiro Joel   No. de lista: 3

Código ejercicio 1

```vhdl
library ieee;
use ieee.std_logic_1164.all;
entity prac11 is
port(
        E0, E1, E2, E3: in std_logic;
        SEL: in std_logic_vector(2 downto 0);
        S0, S1, S2: out std_logic
);
end prac11;

architecture aprac11 of prac11 is
begin

--Multiplexor 1
        S0 <=  E0 when SEL = "00" else
                E1 when SEL = "01" else
                E2 when SEL = "10" else
                E3 when SEL = "11" else "00";

--Multiplexor 2
        with SEL select S1 <= E0 when "11",
                E1 when "10",
                E2 when "01",
                E3 when "00";

--Multiplexor 3
        process (E0, E1, E2, E3, SEL)
        begin
                        if (sel = "00") then
                    S2 <= E2;
                        elsif (sel = "01")then
                        S2 <= E0;
                        elsif (sel = "10")then
                        S2 <= E3;
                        else
                        S2 <= E1;
                        end if;
        end process;

end aprac11;
```
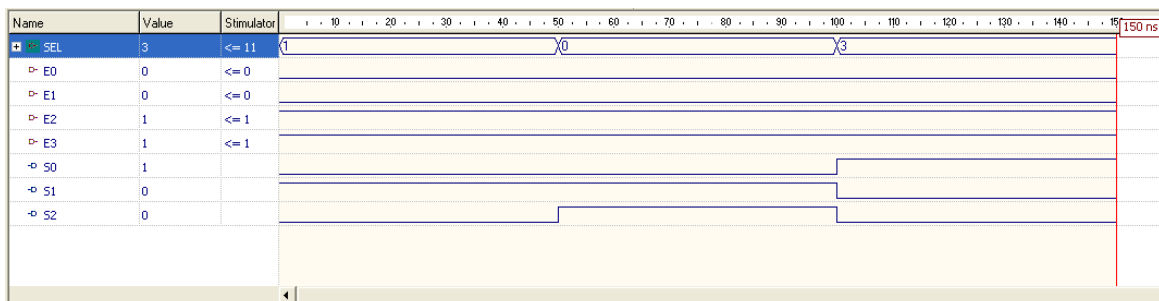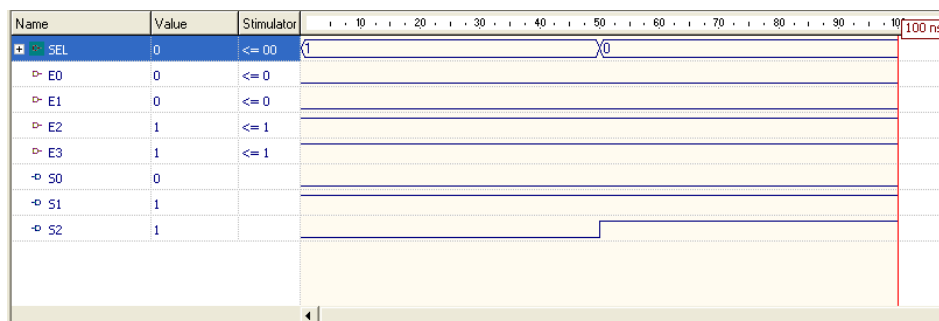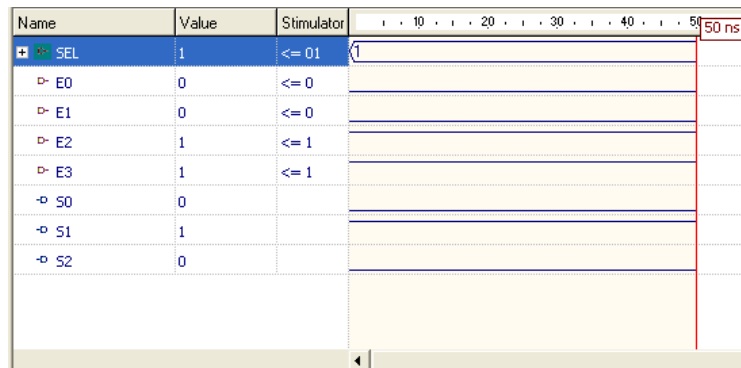
Ejercicio 2

E0	E1	E2	E3	Sal2	Sal1	Sal0
0	1	0	1	0	1	0
1	1	0	0	1	1	0
1	0	1	0	0	0	1

Respecto a la tabla :

Código ejercicio 3

```vhdl
library ieee;
use ieee.std_logic_1164.all;

entity ejer3 is
port(
        A, B: in std_logic_vector(2 downto 0);
        SEL: in std_logic;
        RES: out std_logic_vector(2 downto 0)
);
end ejer3;
architecture aejer3 of ejer3 is
begin
        process(A, B, SEL)
        begin
                if(SEL = '0') then
                        RES <= A;
                elsif(SEL = '1') then
                        RES <= B;
                else
                        RES <= "000";
                end if;
        end process;
end    aejer3;
```

Ejercicio 4

a	b	Sel
5	3	1
4	0	0

Respecto a la tabla: