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Optimizing Analog Circuit Design Through a Machine Learning-Assisted Evolutionary Algorithm

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ABSTRACT

Evolutionary algorithms (EAs) based on circuit simulation are widely employed for analogue circuit sizing because of their high accuracy and adaptability in various cases. However, most of the existing research is focused on a limited set of analogue integrated circuit design specifications. When addressing a complete specification set, the extensive number of simulations required becomes impractical for large circuits. Recent studies incorporating machine learning (ML) techniques have accelerated the optimization process but still involve high simulation costs. This paper proposes an improved and efficient ML-assisted evolutionary algorithm for analogue circuit sizing. The proposed approach integrates a machine learning model into the EA optimization process, effectively reducing the number of required simulations and improving the convergence speed. The experimental results demonstrate the efficiency of the proposed methodology in achieving reliable optimization, with a significant reduction in simulation cost and improved convergence.

1 | Introduction

In mixed-signal designs, most analogue components continue to be designed manually. Due to their sensitivity to noise interference and parameter variations, analogue circuits require careful sizing to meet multiple specifications, which is a complex and time-intensive process. As device sizes shrink in advanced process nodes, circuit sizing for sensitive analogue components becomes increasingly challenging, necessitating an automatic design tool to overcome these bottlenecks.

Evolutionary algorithms (EAs) have been extensively studied for automated circuit sizing, with circuit simulators ensuring accurate performance. The dimensions of the device are optimized to meet the desired performance metrics. However, traditional algorithms struggle with efficiency as the number of objectives increases or when new features are incorporated. Multi-objective optimization algorithms, such as those by [1–3], and [4], focus on automated circuit sizing for analogue/mixed signal circuits.

Machine learning (ML) techniques have also made significant strides in electronic design automation (EDA). For analogue circuit sizing, ML-assisted methods have been proposed to accelerate the sizing process by reducing simulation efforts [5–8]. For example, [5] employs reinforcement learning (RL) to map circuit parameters to performance outcomes, while [6] uses convolutional neural networks (CNN) to analyse transient waveforms and predict outcomes. Ref. [7] further explores deep neural networks (DNN) to maximize design improvements and expedite convergence in iterative sizing [8].

The integration of evolutionary algorithms with machine learning has emerged as a powerful approach to circuit design optimization. Ref. [9] introduced a variation-aware sizing method

using an evolutionary algorithm assisted by ML. Ref. [10] explored hybrid approaches that combine evolutionary algorithms and DNNs for the optimization of analogue design, while [11] examined the use of neural network models in the synthesizing of operational amplifiers. Furthermore, [12] proposed an efficient analogue circuit sizing method utilizing machine learning-assisted global optimization, highlighting the synergy between ML and global optimization techniques for improved design outcomes. These approaches collectively improve computational efficiency and solution accuracy in modern analogue circuit design. While these EA-ML approaches improve optimization efficiency, they still encounter challenges such as high computational costs from ML model training and inference.

Recent studies have further advanced analogue circuit sizing through knowledge transfer frameworks, constraint balancing, and Bayesian optimization approaches. Notable works include a PVT-robustness framework using transfer learning [13], a constraint-objective co-optimization strategy [14], and an evolutionary Bayesian optimizer for automated sizing [15]. These developments reflect the increasing integration of learning techniques to reduce design cost and enhance robustness.

In contrast to these studies, our work focuses on enhancing the genetic crossover stage of evolutionary algorithms through machine learning. Specifically, we propose an ML-assisted crossover strategy in which a deep neural network predicts the effectiveness of crossover masks, enabling the generation of superior offspring without introducing additional simulation cost. This targeted ML integration is the key innovation of our work.

This paper introduces an innovative methodology that integrates evolutionary algorithms with machine learning to enhance optimization efficiency. Using ML to improve genetic crossover operations within evolutionary algorithms, the proposed approach achieves faster convergence and reduces the number of required simulations compared to traditional methods. Furthermore, this methodology demonstrates the potential for broader applications in other simulation-based design processes, offering a more efficient pathway to generate optimized designs.

The remainder of this paper first reviews previous EA-based circuit sizing methods and simulation reduction strategies. Then, the proposed ML-assisted crossover approach is introduced, followed by experimental results demonstrating the efficiency of the method. Finally, the paper concludes with a summary of key findings.

2 | Evolutionary Algorithm-Based Circuit Sizing

Evolutionary algorithms are widely used for optimization tasks, including the synthesis of analogue and digital circuits. Initial populations of randomly generated designs with varying device sizes are simulated and evaluated based on their fitness. If termination conditions are not met, new samples are generated using genetic operators, such as crossover and mutation. These new samples are evaluated and integrated into the population, retaining only the fittest individuals for subsequent iterations. This iterative process continues until the optimal solutions are achieved.

The fitness measure for each sample is commonly defined as the sum of normalized distances between each performance metric and its desired specification. Designs with higher fitness scores exhibit better performance and lower costs. The calculation of these scores is based on the equation originally derived from [9]. Specifically, the cost function is defined as a weighted sum of normalized deviations from target specifications, where only underperforming metrics are penalized:

$$\text{cost}(x) = \sum_i w_i p_i(x) \tag{1}$$

$$p_i(x) = \begin{cases} 0, & \text{if } c_i \geq c_i^* \\ \dfrac{c_i^* - c_i}{c_i^*}, & \text{otherwise} \end{cases} \tag{2}$$

Here, w_i denotes the weighting coefficient for the ith performance metric, c_i is the simulated performance value, and c_i^* is its target specification. This formulation ensures that well-performing metrics do not increase the cost, while deviations below specification are penalized proportionally, encouraging convergence towards feasible and optimized solutions. In evolution, the higher fitness depicts the better individual with a lower cost. However, the random generation of new samples can produce inferior designs, requiring simulations without contributing to the overall results. Predicting and eliminating such low-potential samples can significantly accelerate convergence without compromising solution quality. This ensures an efficient optimization process, minimizes unnecessary computational overhead, and allows faster realization of high-quality design solutions.

This study aims to develop a rapid convergence circuit sizing methodology based on a standard EA flow, enhanced by ML techniques to meet performance specifications. A deep neural network (DNN)-based prediction model determines whether a sample outperforms the performance of a reference design. This model integrates into evolutionary operations, filtering out inferior samples to improve workflow efficiency. The DNN model adopted in this work comprises an input layer corresponding to design parameters, two hidden layers with 64 and 32 neurons, respectively, and a single-node output layer. ReLU activation functions are used for the hidden layers, and a sigmoid function is applied at the output to perform binary classification. Training data consists of design pairs labelled according to relative fitness. Prior to training, all input parameters are normalized to the range $[0, 1]$. The model is trained using the Adam optimizer and binary cross-entropy loss, with an 80/20 train-validation split. The average prediction accuracy on the validation set exceeds 92%, confirming the effectiveness of the DNN for crossover guidance.

3 | Proposed Circuit Sizing Methodology

Recent ML methodologies in circuit sizing aim to accelerate optimization by elucidating relationships between design parameters and circuit performance, reducing reliance on computationally expensive transistor-level simulations. However, accurately modelling complex interactions in analogue circuits requires

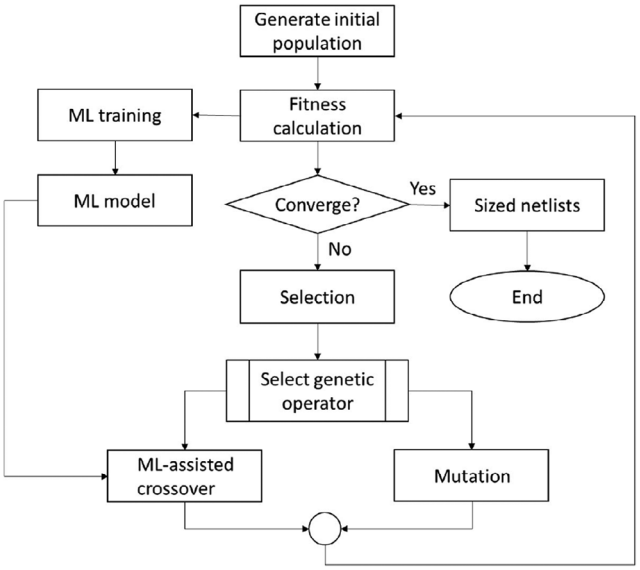

FIGURE 1 | Evolutionary algorithm workflow

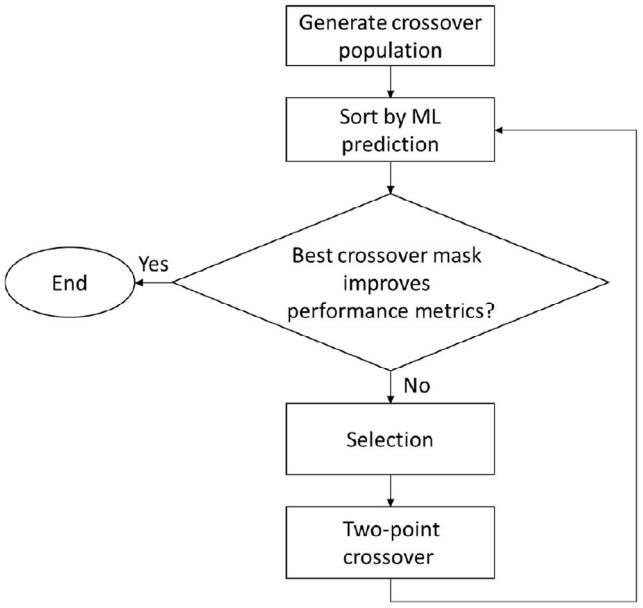

FIGURE 2 | ML-assisted crossover strategy.

extensive training, which is impractical for larger designs. To address these challenges, this study introduces a novel EA flow incorporating ML-assisted operations. The methodology minimizes simulation costs while efficiently identifying promising design candidates.

The general workflow of the evolutionary algorithm is shown in Figure 1. Central to this approach is a DNN model trained to predict whether one design outperforms another. This binary classification simplifies fitness evaluation and improves efficiency. To reduce training effort, the model uses a simplified random sampling technique that compares the fitness of paired designs within the population without requiring exhaustive datasets. This training approach ensures adaptability while reducing the complexity of data preparation.

3.1 | Evolutionary Algorithm Workflow

Each step in the proposed workflow is introduced in the following.

1. Generate initial population: Randomly create a population of circuit designs with different device parameters.
2. Fitness calculation: Run circuit simulations for each design and compare the resulting performance metrics against the given specifications to calculate a fitness value. This fitness value quantifies how well the design meets the desired objectives.
3. ML training: The DNN model is trained using the initial population and their fitness scores. Unlike existing studies applying ML models to directly predict the fitness score of each design, the ML model trained in this work compares each pair of designs from the population, and the model learns to classify which design performs better than the other. This binary classification framework establishes a solid basis for identifying superior candidates.
4. Selection: Choose a subset of designs based on fitness scores.
5. ML-assisted crossover: Use the trained ML model to intelligently combine the features of selected designs, producing superior offspring. Details of the specific crossover methodology and its implementation will be elaborated in the next section.
6. Mutation: Introduce random variations to maintain diversity and avoid local optima.

3.2 | ML-Assisted Crossover Strategy

The proposed ML-assisted crossover approach extends the capabilities of conventional approaches by utilizing the predictive insights of the DNN model to identify and merge optimal traits from parent designs. This integration ensures the retention and enhancement of high-performance characteristics in the offspring, enabling consistent improvements across generations. The proposed ML-assisted crossover strategy is shown in Figure 2. The implementation specifics are detailed below.

1. Generate crossover population: A population of crossover candidates is created by considering uniform crossover and using a set of random selection masks (masks for abbreviation). In uniform crossover, a mask is a binary string (e.g., 011001), where each bit determines whether the offspring inherits the corresponding gene from the first parent (represented by bit 0) or the second parent (represented by bit 1).
2. Sort by ML prediction: Sort the masks according to how the crossover of two designs leads to improved performance metrics, as predicted by the ML model, without the need for additional simulations. This prediction-driven sorting process ensures an efficient and effective selection of promising masks.

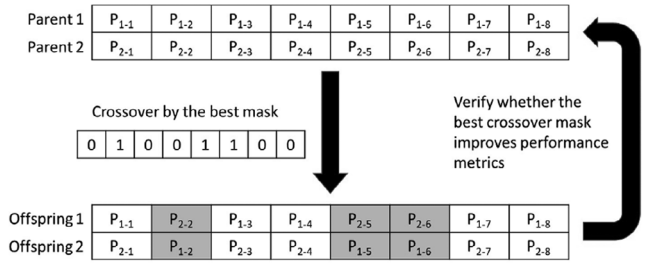

FIGURE 3 | Evaluating performance improvement in crossover mask.

3. Selection: Choose top-ranking crossover masks for further processing.
4. Two-point crossover: Randomly swap segments between the chosen masks to create new masks that inherit traits from the chosen masks while introducing genetic variation.
5. Best crossover mask improves performance metrics: Verify whether the best crossover mask improves performance metrics compared to the parent designs. This assessment relies on predictions from the DNN model, which estimates the likelihood of performance improvement without additional simulations. An evaluation example is shown in Figure 3.

Integrating ML into EA significantly improves circuit sizing efficiency and cost effectiveness. By reducing computational overhead and maintaining high optimization performance, the proposed approach addresses complex circuit sizing challenges effectively. This integration not only optimizes the use of computational resources, but also improves the adaptability of the design process to various circuit specifications. Furthermore, the predictive capacity of the ML model enables the algorithm to identify promising design candidates early, reducing unnecessary iterations. This collaboration between ML and EA accelerates progress in circuit design, creating opportunities to solve increasingly complex and large-scale challenges within the domain.

4 | Experimental Results

To systematically evaluate the adaptability and robustness of the proposed methodology, a diverse set of benchmarks was selected, covering a wide range of circuit configurations and optimization conditions. The assessment focused on two fundamental aspects: computational efficiency, quantified by the reduction in simulation costs, and the algorithm's ability to achieve rapid and reliable convergence to optimal solutions. The proposed evolutionary algorithm assisted by ML and the DNN model was implemented using Python and TensorFlow, with circuit simulations carried out using Synopsys's HSPICE. The algorithm was evaluated using two analogue operational amplifiers: a two-stage op amp and a folded-cascode op amp, both fabricated using 40-nm CMOS technology. The specifications were derived from DC, AC, and transient analyses, ensuring a comprehensive evaluation framework. All specifications were considered equally significant.

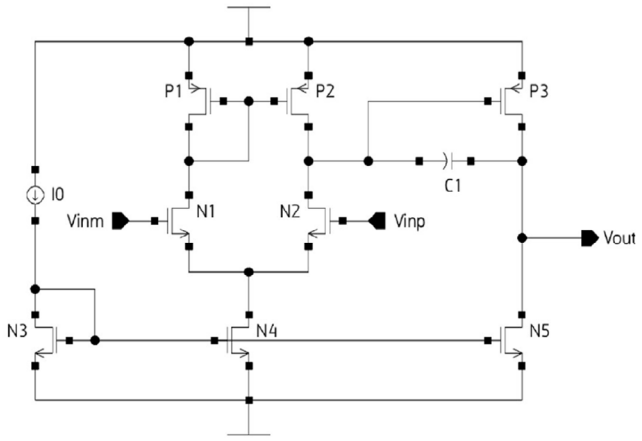

FIGURE 4 | The schematic of the two-stage operational amplifier

TABLE 1 | Design parameters and their ranges for the two-stage OPA (test case 1).

Parameter	Minimum	Maximum	Step
$W_{N1} = W_{N2}$ (μm)	0.14	50	0.01
W_{N3} (μm)	0.14	50	0.01
W_{N4} (μm)	0.14	50	0.01
W_{N5} (μm)	0.14	50	0.01
$W_{P1} = W_{P2}$ (μm)	0.14	50	0.01
W_{P3} (μm)	0.14	50	0.01
$L_{N1} = L_{N2}$ (μm)	0.04	0.4	0.01
$L_{N3} = L_{N4} = L_{N5}$ (μm)	0.04	0.4	0.01
$L_{P1} = L_{P2}$ (μm)	0.04	0.4	0.01
L_{P3} (μm)	0.04	0.4	0.01
C_{C1} (pF)	1	10	1

4.1 | Case Study 1

The first test case involves a two-stage operational amplifier shown in Figure 4, characterized by 11 design parameters. The parameter search ranges are presented in Table 1. The objective of this sizing problem is to optimize key performance metrics, including gain, unity gain frequency, slew rate, phase margin, power consumption, and area efficiency. In this work, area efficiency is calculated by summing the physical areas of all individual devices within the circuit. The objectives are presented in Table 2.

The proposed evolutionary algorithm assisted by ML was executed ten runs, successfully meeting all specified performance requirements in each instance. The algorithm converged within 260 simulations, remaining well below the allocated budget of 500 simulations. The total computation time was approximately 8 h (system time). As shown in Figure 5, compared to the EA-based reference method for analogue IC sizing, the proposed approach demonstrated superior solution quality, achieving more efficient and precise results. A cost value of 0 indicates that the design has fully met all the specified objectives.

TABLE 2 | Objective for the two-stage OPA (test case 1).

Metrics	Spec
Gain (dB)	>80
Unity gain frequency (MHz)	>5
Slew rate (V/μs)	>8
Phase margin (°)	>40
Power consumption (mW)	<0.2
Area (μm^2)	<60

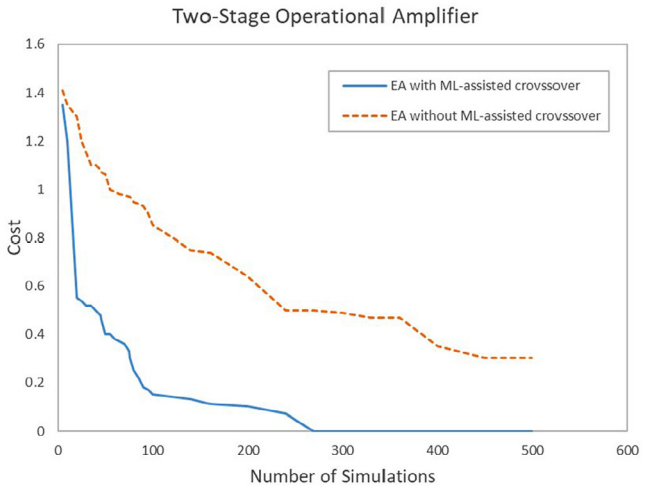

FIGURE 5 | Cost (best so far) of two algorithms within 500 simulations (average over ten runs).

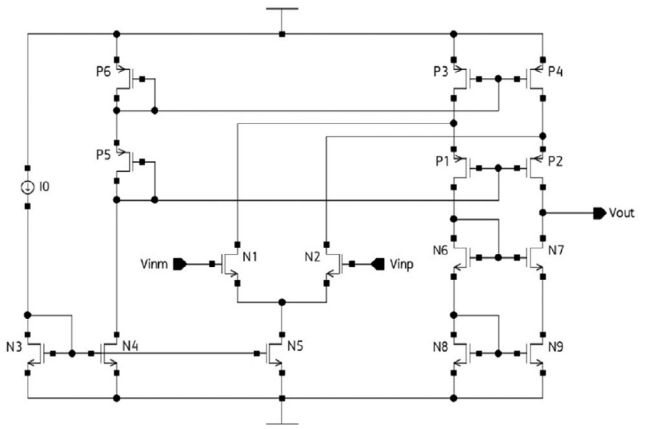

FIGURE 6 | The schematic of the folded-cascode operational amplifier.

4.2 | Case Study 2

The second test case involves a folded-cascode operational amplifier Figure 6, characterized by 12 design parameters and a greater number of devices compared to Case 1. The parameter search ranges are presented in Table 3. The objective of this sizing problem is to optimize key performance metrics while maintaining consistency with the criteria outlined in Case 1, but with adjusted targets to accommodate the specific design requirements of this scenario. This ensures a standardized evaluation framework for comparative analysis. The objectives are presented in Table 4.

TABLE 3 | Design parameters and their ranges for the folded-cascode OPA (test case 2).

Parameter	Minimum	Maximum	Step
$W_{N1} = W_{N2}$ (μm)	0.14	50	0.01
W_{N3} (μm)	0.14	50	0.01
W_{N4} (μm)	0.14	50	0.01
W_{N5} (μm)	0.14	50	0.01
$W_{N6} = W_{N7} = W_{N8} = W_{N9}$ (μm)	0.14	50	0.01
$W_{P1} = W_{P2} = W_{P3} = W_{P4}$ (μm)	0.14	50	0.01
$W_{P5} = W_{P6}$ (μm)	0.14	50	0.01
$L_{N1} = L_{N2}$ (μm)	0.04	0.4	0.01
$L_{N3} = L_{N4} = L_{N5}$ (μm)	0.04	0.4	0.01
$L_{N6} = L_{N7} = L_{N8} = L_{N9}$ (μm)	0.04	0.4	0.01
$L_{P1} = L_{P2} = L_{P3} = L_{P4}$ (μm)	0.04	0.4	0.01
$L_{P5} = L_{P6}$ (μm)	0.04	0.4	0.01

TABLE 4 | Objective for the folded-cascode OPA (test case 2).

Metrics	Spec
Gain (dB)	>60
Unity gain frequency (MHz)	>30
Slew Rate (V/μs)	>0.8
Phase margin (°)	>60
Power consumption (mW)	<2
Area (μm^2)	<200

The proposed ML-assisted evolutionary algorithm was executed ten runs, consistently satisfying all specified performance requirements. The algorithm converged within 400 simulations, well below the allocated budget of 500 simulations, with a total computation time of approximately 25 h (system time). Compared to the EA-based reference method for analogue IC sizing, as shown in Figure 7, the proposed approach demonstrated superior solution quality, achieving higher efficiency and precision. A cost value of 0 indicates that the design has successfully met all the specified objectives. This improvement was driven by predictive modelling, which facilitated efficient candidate selection and minimized unnecessary simulations. Furthermore, the ML-assisted approach accelerated the optimization process by leveraging predictive insights, reducing the number of iterations required to meet design specifications while maintaining the accuracy of the solution. A comparison between the EA with and without ML-assisted crossover shows a clear difference in convergence behaviour, highlighting the impact of the proposed strategy on optimization efficiency.

Across ten independent runs, the number of simulations until convergence ranged from 240 to 270 for the two-stage op amp

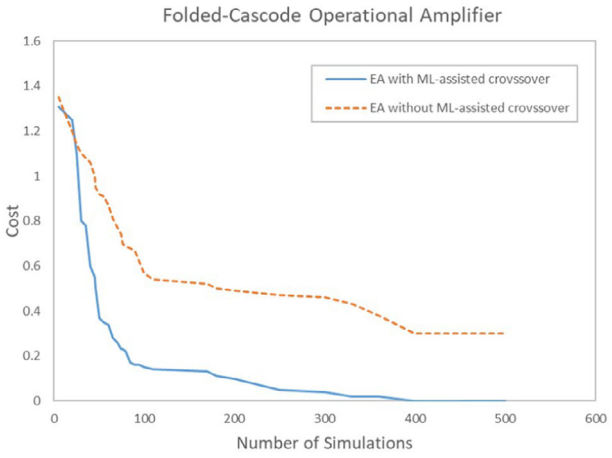

FIGURE 7 | Cost (best so far) of two algorithms within 500 simulations (average over ten runs).

and from 370 to 420 for the folded-cascode amplifier. For each case, approximately 5000 labelled design pairs were generated from the initial population to train the DNN model. The relatively higher simulation count for the folded-cascode design reflects its increased circuit complexity and larger parameter space. All experiments were conducted on a workstation equipped with an Intel Core i7-12700K CPU and 32 GB RAM, running Ubuntu 20.04. No GPU acceleration was used. Each DNN training session required less than 10 min per circuit type, confirming the practicality of the approach on standard hardware. The DNN model achieved a prediction accuracy exceeding 92% on a validation set derived from the training data, indicating effective learning of crossover quality.

5 | Conclusion

This paper introduces an ML-assisted evolutionary algorithm for analogue circuit sizing that integrates the advantages of machine learning with traditional evolutionary algorithms. The proposed approach overcomes significant limitations, lowers simulation costs, and enhances convergence speed. Experimental results demonstrate its efficiency and emphasize its potential for wider applications in optimizing analogue circuits across various design challenges. The effectiveness of the proposed ML-assisted crossover was further verified through a comparative study evaluating performance with and without the ML model, confirming its critical role in accelerating convergence.

Author Contributions

Yu-Yu Chen contributed to conceptualization, methodology, and writing original draft, and Shao-Yun Fang supervised the project and acquired funding. Both authors reviewed and approved the final manuscript.

Conflicts of Interest

The authors declare no conflicts of interest.

Data Availability Statement

The data that support the findings of this study are available on request from the corresponding author. The data are not publicly available due to privacy or ethical restrictions.

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