Classifying Analog and Digital Circuits with Machine Learning Techniques toward Mixed-Signal Design Automation

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***Abstract*—For modern system-on-chip (SoC) design, one of the most challenging and time-consuming tasks is the layout design of the mixed-signal integrated circuit (IC), which integrates both analog and digital circuits into a single chip. There is no industrial tool which can automatically identify analog and digital sub-circuits in a mixed-signal design to accelerate the layout design automation. In this paper, we first introduce a device sorting method to generate an unique sequence for circuit components. Then, we apply an unique matrix representation to encode circuit netlists. Finally, we employ machine learning algorithms to automatically classify/identify analog and digital sub-circuits. The experimental results show that the proposed method is promising based on the convolutional neural network (CNN) algorithm.**

I. Introduction

Mixed-signal circuits plays a very important role in modern system-on-chip (SoC) designs. However, it is difficult to achieve design automation due to substantial difference in circuit characteristics between digital and analog circuits. When designing such kind of sophisticated circuits, one of the most challenging and time-consuming tasks is the layout design consisting of both analog and digital circuit in the same chip. Fig. 1 shows a $\Sigma\Delta$ modulator, which is a common mixed-signal circuit for SoC applications. According to [1], noise coupling between analog and digital circuits is extremely critical in modern mixed-signal SoC designs. It has the greatest impact on circuit accuracy and performance. In order to achieve high-quality mixed-signal layouts with less noise coupling, a deterministic method for mixed-signal layout generation with separated analog and digital signal paths was then proposed in [1]. Although Lin *et al.* [1] have introduced an automatic placement and routing method to mitigate noise coupling between analog and digital signals during layout design of the mixed-signal integrated circuit (IC), they

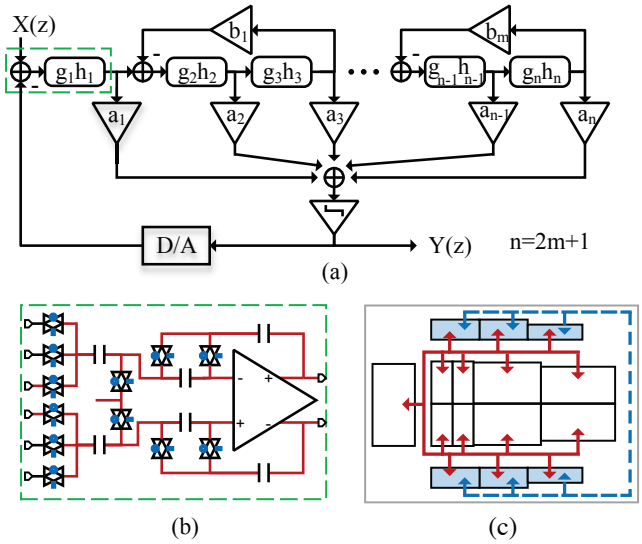


Fig. 1: Analog and digital signal separation for achieving qualified mixed-signal layout design [1]. (a) A generic n^{th}-order $\Sigma\Delta$ modulator. (b) The schematic of the first integrator of the generic n^{th}-order modulator in (a). (c) A desired mixed-signal layout topology with separated analog and digital signal paths for the integrator in (b).

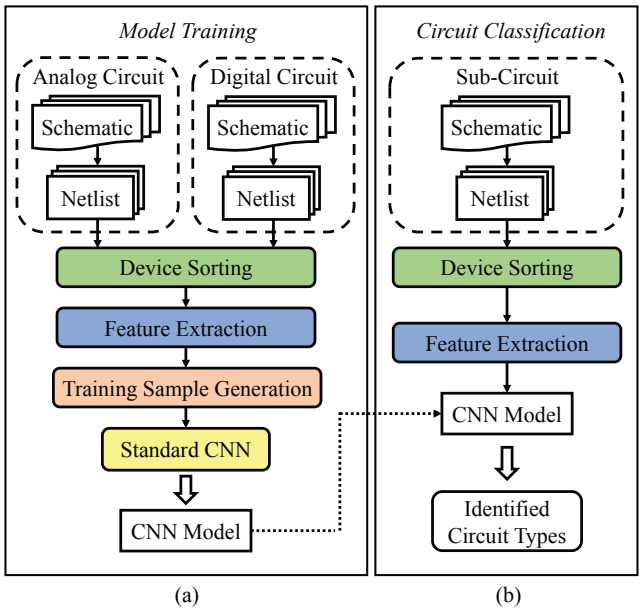
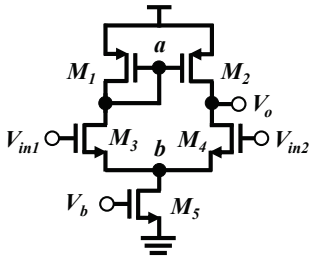


Fig. 2: Overview of analog and digital circuit classification with machine learning techniques. (a) Model training flow. (b) Circuit classification flow.

978-1-5386-5153-7/18/$31.00



name	D	G	S	B	model	width	length
M_1	a	a	vdd	vdd	P	W=1μ	L=1μ
M_2	V_o	a	vdd	vdd	P	W=1μ	L=1μ
M_3	a	V_{in1}	b	gnd	N	W=1μ	L=1μ
M_4	V_o	V_{in2}	b	gnd	N	W=1μ	L=1μ
M_5	b	V_b	gnd	gnd	N	W=1μ	L=1μ

Device/Net order based on parsing sequence:

$M_1 > M_2 > M_3 > M_4 > M_5$

$a > vdd > V_o > V_{in1} > b > gnd > V_{in2} > V_b$

Initial circuit matrix based on parsing sequence:

	a	vdd	V_o	V_{in1}	b	gnd	V_{in2}	V_b
M_1	1	1	0	0	0	0	0	0
M_2	1	1	1	0	0	0	0	0
M_3	1	0	0	1	1	0	0	0
M_4	0	0	1	0	1	0	1	0
M_5	0	0	0	0	1	1	0	1

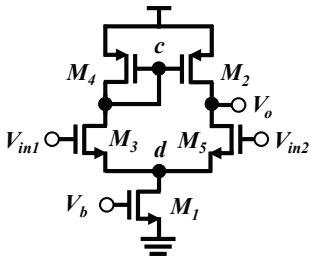
Circuit matrix partitioning and rearrangements

	a	b	vdd	V_o	V_{in1}	gnd	V_{in2}	V_b			
M_3	1	1	0	0	1	0	0	0	2	0	1
M_2	1	0	1	1	0	0	0	0	1	2	0
M_4	0	1	0	1	0	0	1	0	1	1	1
M_1	1	0	1	0	0	0	0	0	1	1	0
M_5	0	1	0	0	0	1	0	1	1	0	2

Final circuit matrix with unique device/net order:

	a	b	vdd	V_o	V_{in1}	gnd	V_{in2}	V_b			
M_1	1	0	1	0	0	0	0	0	1	1	0
M_2	1	0	1	1	0	0	0	0	1	2	0
M_3	1	1	0	0	1	0	0	0	2	0	1
M_4	0	1	0	1	0	0	1	0	1	1	1
M_5	0	1	0	0	0	1	0	1	1	0	2

(a)



name	D	G	S	B	model	width	length
M_2	V_o	c	vdd	vdd	P	W=1μ	L=1μ
M_5	V_o	V_{in2}	d	gnd	N	W=1μ	L=1μ
M_1	d	V_b	gnd	gnd	N	W=1μ	L=1μ
M_3	c	V_{in1}	d	gnd	N	W=1μ	L=1μ
M_4	c	c	vdd	vdd	P	W=1μ	L=1μ

Device/Net order based on parsing sequence:

$M_2 > M_5 > M_1 > M_3 > M_4$

$V_o > c > vdd > V_{in2} > d > gnd > V_b > V_{in1}$

Initial circuit matrix based on parsing sequence:

	V_o	c	vdd	V_{in2}	d	gnd	V_b	V_{in1}
M_2	1	1	1	0	0	0	0	0
M_5	1	0	0	1	1	0	0	0
M_1	0	0	0	0	1	1	1	0
M_3	0	1	0	0	1	0	0	1
M_4	0	1	1	0	0	0	0	0

Circuit matrix partitioning and rearrangements

	c	d	V_o	vdd	V_{in2}	gnd	V_b	V_{in1}			
M_2	1	0	1	1	0	0	0	0	1	2	0
M_5	0	1	1	0	1	0	0	0	1	1	1
M_1	0	1	0	0	0	1	1	0	1	0	2
M_3	1	1	0	0	0	0	0	1	2	0	1
M_4	1	0	0	1	0	0	0	0	1	1	0

Final circuit matrix with unique device/net order:

	c	d	V_o	vdd	V_{in2}	gnd	V_b	V_{in1}			
M_3	1	1	0	0	0	0	0	1	2	0	1
M_2	1	0	1	1	0	0	0	0	1	2	0
M_5	0	1	1	0	1	0	0	0	1	1	1
M_4	1	0	0	1	0	0	0	0	1	1	0
M_1	0	1	0	0	0	1	1	0	1	0	2

(b)

Fig. 3: A device sorting method based on circuit matrix partitioning and rearrangements [7]. After device sorting, the same MOS differential amplifier with different device/net names and netlist files, as shown in (a) and (b), will result in unique device/net orders, which is independent of the device/net names and netlist files.

assumed that the analog and digital sub-circuits had been manually specified by designers before automatic placement and routing. Nevertheless, it is still very time-consuming for designers to manually specify analog and digital sub-circuits in the complex circuit netlist. The automatic classification and identification of analog and digital sub-circuits in a large-scale mixed-signal IC is still an open problem.

In this paper, we employ machine learning techniques to automatically classify and identify analog and digital sub-circuits by introducing a device sorting method for unique sequence of circuit components and encoding circuit netlists with unique matrix representation for effectively applying machine learning algorithms. By training with a sufficient data set, the proposed method can achieve 97.2% accuracy in classifying analog and digital sub-circuits. It should be noted that our work is different from [2]–[6] which were focused on identifying analog building blocks or extract the structural features in analog circuits. Those works did not classify analog

and digital sub-circuits.

The rest of this paper is organized as follows. Section II introduces our method based on machine learning to classify analog and digital sub-circuits. Section III reports the experimental results, and finally Section IV concludes this paper.

II. Proposed Method

In order to identify analog and digital sub-circuits in a large-scale mixed-signal design, first of all, we need to train a model which can correctly identified circuit types. Based on the trained model, analog and digital sub-circuits can be classified and identified by machine. With the information of analog and digital sub-circuits, an automatic placement and routing tool may apply different methods for different types of sub-circuits and avoid noise coupling between them [8]. Consequently, the design cycle of a mixed-signal design can be further reduced. Fig. 2 gives an overview of classifying analog and digital sub-circuits based on the machine learning techniques, including a model training flow and a circuit classification flow.

A. Device Sorting

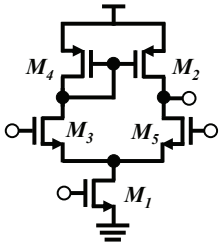
Device sorting produces a unique sequence of devices and nets in a netlist, which is independent of the names of devices/nets in a schematic and the sequence in a netlist description file. In order to avoid such dependency, we apply the device sorting method based on circuit matrix partitioning and rearrangement [7] for a netlist. Inputing a netlist file with m devices and n nets, it first generates an m-by-n initial circuit matrix based on the parsing sequence of devices and nets. A matrix element is 1 if the corresponding device and net are connected. Otherwise, the matrix element is 0. After a sequence of circuit matrix partitioning and rearrangements, a unique device/net order can be obtained. Fig. 3 demonstrates the detailed processing steps for two different netlist files of the same circuit, resulting in the same device/net orders.

B. Feature Extraction

Feature extraction converts circuit structures into a matrix representation for identifying sub-circuit types using the convolutional neural network (CNN) algorithm. Inputting a circuit netlist and the device order resulting from the aforementioned device ordering method, we apply a matrix representation based on the terminal connection index (TCI) [8]. A TCI is a universal coding scheme which describes the interconnection relationship between terminals of each device. For example, the interconnection relationship between the drain, gate, and source of two MOS devices, M_i and M_j, can be coded with the TCI, as shown in Table I, where $tci_{i\to j}^{p\to q}$ denotes the TCI if there is a connection from terminal p of M_i to terminal q of M_j. Based on the TCI in Table I, Fig. 4 gives an example circuit schematic, and the corresponding matrix representation. The numbers in the matrix indicate the summation of all TCI between M_i and M_j. The matrix representation will be the input data when applying the machine learning techniques.

TABLE I: An example coding scheme for two MOS devices, M_i and M_j, where D, G, and S denote DRAIN, GATE, and SOURCE terminals, respectively [8].

$tci_{i\to j}^{p\to q}$		Terminal of M_i		
		D	G	S
Terminal of M_j	D	1	8	64
	G	2	16	128
	S	4	32	256



(a)

To M_j

From M_i	M_3	M_2	M_5	M_4	M_1
M_3	0	2	256	3	64
M_2	8	0	1	280	0
M_5	256	1	0	0	64
M_4	9	274	0	0	0
M_1	4	0	4	0	0

(b)

Fig. 4: (a) A circuit schematic. (b) The corresponding matrix representation based on the TCI in Table I.

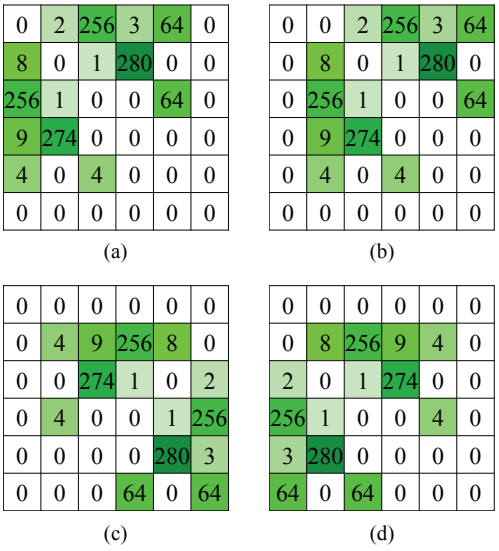


Fig. 5: Data augmentation with matrix transformations. (a) The original matrix. (b) Matrix shifting. (c) Matrix rotation. (d) Matrix flipping.

C. Training Sample Generation

Based on the introduced matrix representation of a circuit netlist, various training samples for both analog and digital sub-circuits can be obtained for training and testing data sets. Each sample sub-circuit is tagged with either an analog or a digital type. The machine will first learn from the samples during model training, and then determine whether a sub-circuit in a mixed-signal design is analog or digital based

on the trained model. In order to avoid overfitting problem in machine learning, we shall also augment the data set by shifting, rotating, and flipping the original matrix representing a sub-circuit, as demonstrated in Fig. 5.

III. Experimental Results

We implemented the introduced sub-circuit identification method using the Python programming language based on the GPU version of TensorFlow, and performed our experiments on a 2.6 GHZ Intel machine under the Linux operating system with the NVIDIA GTX 1080Ti graphic card. We employed CNN as the machine learning kernel to achieve our goal since CNN is one of the most effective deep learning techniques for classification problems.

TABLE II: The size of training and testing dataset.

Circuit Type	# Training Data	# Testing Data
Analog	86888 (52.3%)	36564 (51.9%)
Digital	79367 (47.7%)	33905 (48.1%)

Table II shows the summary of our data set, including both training and testing data, which contains a large number of analog and digital sub-circuits. Each sub-circuit in the data set is represented by a matrix based on the proposed matrix representation. The matrix size is 42-by-42 because the largest sub-circuit in the data set contains 42 devices. We adopted zero padding to a matrix if the corresponding sub-circuit contains less than 42 devices. Based on the data set, we first tuned the hyperparameters of the CNN for model training, including learning rate, and the numbers of layers and iterations by optimizing the mean squared error (MSE) loss. Based on our empirical study, we found that the combination of four convolution layers and two max-pooling layers can result in the best performance.

We then applied the CNN with fine-tuned hyperparameters to conduct our experiment. Table III shows our experimental results. We compare three different methods, including (1) the proposed approach without applying device sorting, (2) the proposed approach without feature extraction, and (3) the proposed approach with both device sorting and feature extraction. For (1), the device order may depend on the names of devices/nets and the sequence in a netlist file. For (2), without feature extraction, instead of representing the sophisticated relationship between two devices by the coding scheme in Table I, we only consider TRUE/FALSE relationship between two devices. If there is a connection between two devices, the corresponding matrix element in the matrix representation of the circuit would be true, Otherwise, it is false. According to the experimental results in Table III, the proposed approach with both device sorting and feature extraction can achieve the best accuracy.

After the model is trained and tested, we further apply the trained model to identify the sub-circuit types in the $\Sigma\Delta$ modulator, as seen in Fig 1. The digital sub-circuits in the $\Sigma\Delta$ modulator include inverters, buffers, comparators,

TABLE III: The comparison of different approaches.

Our Approaches	Testing Accuracy (%)	Runtime (seconds)	
		Training	Testing
(1) w/o Device Sorting	72.3 ± 0.9	701.2	1.4
(2) w/o Feature Extraction	87.1 ± 1.7	703.1	1.4
(3) w/ both Device Sorting & Feature Extraction	97.2 ± 1.4	702.5	1.4

and so on, while analog sub-circuits include bias circuits, operational amplifiers, and so forth. By using our model to identify the sub-circuit types, it takes only 1.5 seconds, and the results compared with manually assignment are exactly the same. Consequently, the proposed analog/digital sub-circuit classification and identification based on the machine learning techniques can rapidly recognize the sub-circuit types and accelerate mixed-signal IC design process.

IV. Conclusions and Future Work

When designing mixed-signal ICs, one of the most challenging and time-consuming tasks is the layout design, which integrates both analog and digital circuits into a single chip. Currently, there is still no industrial tool which can automatically identify and extract analog and digital sub-circuits in a mixed-signal design to accelerate the layout design flow. In this paper, we apply machine learning techniques to automatic circuit classification and identification of analog and digital sub-circuits, and hence the mixed-signal IC design flow for SoC. The experimental results show that the proposed method based on the CNN algorithm is promising. Future work lies in the advancement of accuracy by increasing data and applying reinforcement learning.

Acknowledgement

This work is partly supported by the Ministry of Science and Technology (MOST), Taiwan, under Grant No. 104-2628-E-194-001-MY3, and AnaGlobe Technology, Inc., Taiwan.

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