Design Optimization of Analog Integrated Circuits by Using Artificial Neural Networks

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Abstract— **This paper presents a computer-aided design (CAD) tool for automated sizing and optimization of analog integrated circuits (ICs). This tool uses artificial neural networks (ANNs) in order to deduce the device sizes that optimize the performance objectives while satisfying the constraint specifications. Neural networks can learn and generalize from data allowing model development even when component formulas are unavailable. The training data are obtained by various simulations in the HSPICE design environment with TSMC 0.18 µm CMOS process parameters. To evaluate the tool, one practical example is presented in 0.18 µm CMOS technology. The simulation results verify effectiveness of the proposed method for analog circuits sizing.**

Keywords- computer-aided design; analog integrated circuits; neural networks; multilayer perceptron; optimization

I. INTRODUCTION

Although a great deal of effort has been recently devoted to the development of CAD tools for the automatic design of integrated circuits, most of this effort has been directed to digital design. The design of the analog part of a circuit is still a time-consuming task. This is due to the complex relations that exist between design parameters and circuit performances.

The typical starting point of an analog design is a circuit topology and a set of parameters obtained from the designer's experience. Then, several simulations and redesigns are carried out until an acceptable circuit is achieved. This redesign process is a very time-consuming task. In addition, a designer's experience is required to interpret the results obtained from the simulation and to modify the design parameters in the proper direction.

The increasing demand of application-specific IC's (ASIC's) that are entirely or partly analogic, makes necessary the development of CAD tools, which decrease the design time, increase the design accuracy and allow nonexperts to design complex analog circuits [1].

Analog circuit design is generally achieved through the following steps.

1) Topology selection
2) Parametric optimization
3) Layout generation

First, designer selects an appropriate circuit topology among various possible alternative architectures and topologies, to achieve higher performances for a particular application. The second step consists of assigning values to circuit parameters (widths and lengths of the MOS transistors, resistors and capacitors values as well as bias voltages and currents) so that the circuit performances are met while a set of specification constraints are satisfied. The optimized circuit then needs to be transformed into a layout.

Even if the topology of the circuit to be designed is fixed, finding the optimal set of circuit parameters values is not an easy task, since all circuit performances and specifications rely on it. The parametric optimization is complicated due to the conflicting design objectives and performance constraints, which are generally implicit nonlinear functions of circuit parameters. Complex trade-offs between these requirements has to be made before a near-optimal solution is reached [2].

Neural networks are information processing systems inspired by the ability of human brain to learn from observation and to generalize by abstraction. In this paper, artificial neural networks (ANNs) are proposed to accurately model the circuit performance functions. In other words, a neural network is used in order to find a set of circuit parameters (or design variables) such that the design objectives are optimized while satisfying performance constraints for different Op-Amp topologies.

The paper is organized as follows. Section II reviews recent efforts in parametric optimization. Section III describes design procedure which uses neural network for circuits sizing. Simulation results are provided in Section IV to show the efficiency, effectiveness and advantages of the proposed approach. Finally, Section V presents some concluding remarks.

II. PREVIOUS EFFORTS

In recent years, several prototype design automation (DA) systems have been proposed to automate the design of cell-level analog circuits. Most of these systems concern parametric optimization by using optimization-based design approach.

The optimization-based design approach uses recent advances in the optimization theory and algorithms, and relates these to the parametric optimization of analog ICs.

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The synthesis problem is formulated as one of mathematical programming. The circuit performances are considered to be the objective functions, which are to be minimized or maximized subject to a set of specification constraints. Optimization-based design approach can be broadly classified into two categories: a) Simulation-based optimization, b) Analytical equation based optimization. Historically, the very first attempts towards analog DA were based on numerical optimization. Systems such as DELIGHT.SPICE [3], ECSTACY [4], ADOPT [5], and ASTRX/OBLX [6] consider the sizing of the individual transistors in a given circuit topology as an optimization problem [7].

Typically, these systems employ optimization algorithms, which iteratively adjust the individual transistor sizes in order to meet the constraints and objectives specified by the user. A simulator is used within the optimization loop to assess the performance of the circuit during each iteration. This design approach is referred to as simulation-based optimization.

The time consuming and expensive simulator inside the optimization loop is avoided by using simplified analytical models that predict circuit performances and this approach is referred to as analytical equation based optimization [8]. A number of prototypes have evolved out in recent times, which use this technique, e.g., OPASYN [9], STAIC [10], FPAD [2], FASY [1]; however, the major problem of this approach is low accuracy that is caused by non-linearity approximations used in the hand equations and high-order effects in advanced MOS transistor models [11], [12].

The main goal here is to propose a new approach that uses the advantages of artificial neural networks to optimize the performance of analog integrated circuits and to overcome previous efforts limitations. The proposed approach has the following specifications.

- It uses training data including device/circuit data to model highly nonlinear and complex circuit performance functions; consequently, using approximately analytical equations with low accuracy is no more needed.

- Using this approach causes to avoid a simulator in the optimization loop and therefore avoid the cost of repeated simulation, and speed up the approach in order to make it interactive.

III. Design Procedure

This section describes the modeling procedure.

1) A reference circuit simulator **(**HSPICE**)** is used to generate a set of base points, called the training set and these data points are considered to be as input-output data of network. Input data include circuit specifications (DC gain, Unity-gain frequency, Phase margin, Slew rate, Power dissipation, etc) and output data include circuit parameters (widths and lengths of the MOS transistors, resistors and capacitors values as well as bias voltages and currents).

2) A neural network model (Multilayer Perceptron) is employed to model the circuit performance functions of interest and optimize the parameters of the circuit. The approximate number of neurons in the input, hidden and output layers are chosen according to [13] and then they are modified by tries and errors to lead to the efficient structure for the network.

3) The parameters of the model are tuned in an automatic way, by means of a learning process based on the back propagation technique. The computational expense of the proposed approach is nearly equal to computational expense of neural network learning procedure.

4) In order to evaluate optimization approach, by using variables obtained from previous steps, the multistage Op-Amp circuit is simulated by using HSPICE program in 0.18 μm CMOS technology.

IV. Simulation Results

In order to validate the proposed analog circuit design approach, one detailed design example is presented. This example involves the design of a three-stage CMOS operational amplifier (nested miller compensated Op-Amp) circuit.

Design of a three-stage Op-Amp

The voltage gain can be further increased by additional gain stages. In this case, Fig. 1 depicts the schematic of a three-stage CMOS Op-Amp (NMC) which is an extended version of miller compensated Op-Amp, is used to achieve the stability. Theoretically, NMC can be extended to infinite number of stages. Nevertheless, no more than four stages have been reported because of the reduction of bandwidth, impractical large DC gain and higher power dissipation required [14]. Hence, only three-stage NMC amplifier is discussed in this section. The design variables for this circuit are the length (L), width (W) and overdrive voltage of all transistors and compensation capacitors C_{m1} and C_{m2}. The supply voltages Vdd and Vss and load capacitance (C_L) are taken as constants specified by the user. In order to get the independent design variables, which are to be varied during the optimization process, it is assumed perfect matching between transistors, as required by symmetry of the circuit. Thus, the independent design variables of the circuit topology shown in Fig. 1 are: X_N, X_P, W_1, L_1, W_3, L_3, W_5, L_5, W_6, L_6, W_7, L_7, W_9, L_9, W_{10}, L_{10}, W_{11}, L_{11}, C_{m1} and C_{m2}.

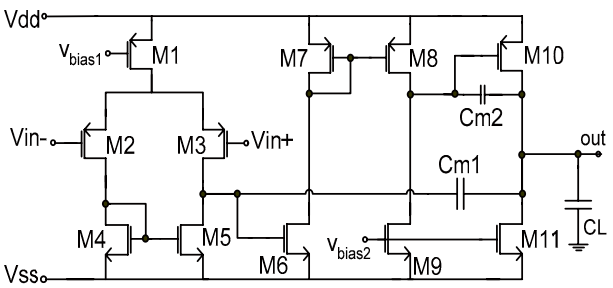

Figure 1. Schematic of the three-stage CMOS operational amplifier

First, 200 base points were generated using HSPICE program, and the parameters of a 0.18 µm CMOS technology, (150 for training set and 50 for the testing set). Then, a neural network 5-8-14-20 (Fig. 2) was employed. The simulation of neural network was performed in the MATLAB environment and the three-stage Op-Amp shown in Fig. 1 was optimized for a set of circuit specification shown in Table I. The circuit size vector and the performance characteristics are computed by means of ANN approach and optimization results are shown in Table II and III.

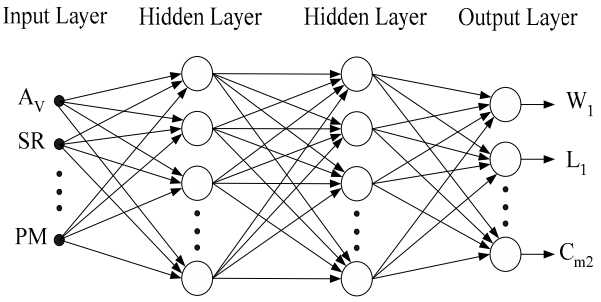

Figure 2. The structure of applied MLP

TABLE I. SPECIFICATION OF THREE-STAGE CMOS OP-AMP

Electrical parameters	Expected
Supply voltages (V)	±0.75
Load capacitance: C_L (pF)	100
DC gain: A_0 (dB)	> 100
Gain-band width: GBW (MHz)	> 0.1
Phase margin: PM (deg.)	> 60
Slew rate: SR (V/µsec)	> 0.1
Power dissipation (µW)	< 500

TABLE II. OPTIMUM VALUES OBTAINED BY ANN

Parameter	Value	Unit
$(W/L)_1$	55.17	µm/µm
$(W/L)_{2,3}$	6.06	µm/µm
$(W/L)_{4,5}$	33.2	µm/µm
$(W/L)_6$	3	µm/µm
$(W/L)_{7,8}$	8.62	µm/µm
$(W/L)_9$	0.84	µm/µm
$(W/L)_{10}$	84	µm/µm
$(W/L)_{11}$	3.7	µm/µm
V_{bias1}	+.25	V
V_{bias2}	-0.15	V
C_{m1}	78	pF
C_{m2}	17	pF

TABLE III. SIMULATION RESULTS IN MATLAB AND HSPICE

Performance specification	Value in MATLAB	Value in HSPICE
A_0 (dB)	107.7	104
GBW (MHz)	0.2	0.19
PM (deg.)	64	61
SR (V/µsec)	0.18	0.14
Pdiss. (µW)	70	61.25
Output swing (V)	1.35	1.22
Total area (µm^2)	492.15	492.15

The training process of neural network for optimization of three-stage Op-Amp (Fig. 1) is shown in Fig. 3. More clearly, after 134 epochs, the minimum error is reached (less than 10^{-2}) and performance goal is met.

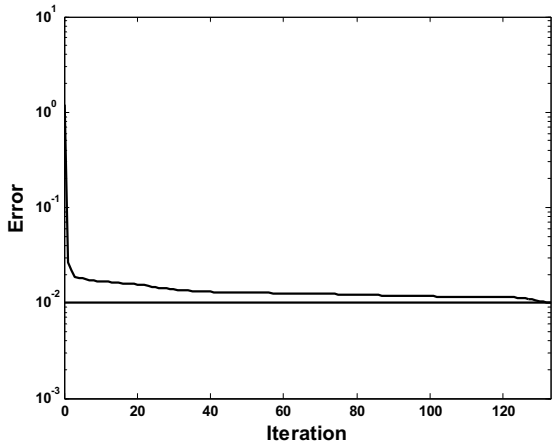

Figure 3. Training process of ANN for three-stage CMOS Op-Amp

Furthermore, the obtained output results from the optimization approach (ANN) are used in order to simulate three-stage Op-Amp by using HSPICE program in 0.18 µm CMOS technology and simulation results are shown in Table III and Fig. 4.

The obtained results by using MATLAB and HSPICE, confirm that all the specifications are fully satisfied and output results obtained from optimization approach match reasonably with the results obtained from HSPICE simulations. This substantiates the validity of presented approach for parametric optimization of multistage Op-Amps.

Moreover, a comparison is presented between the results of proposed approach in this work and references [14], [15] in Table IV.

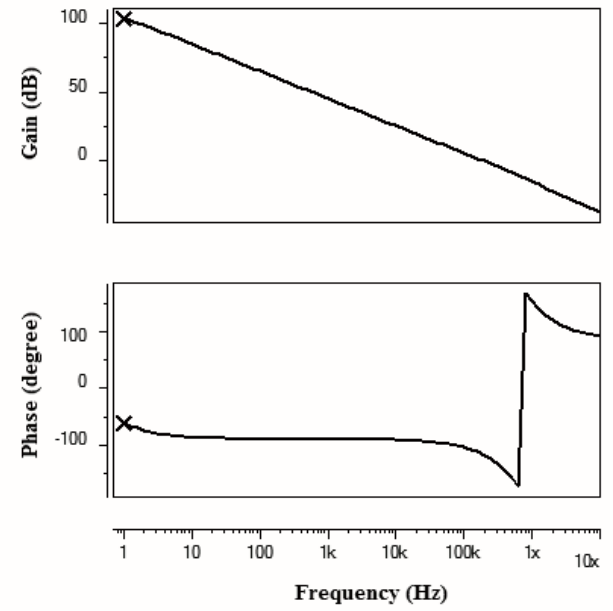

Figure 4. Frequency response of the three-stage Op-Amp

TABLE IV. COMPARISON WITH PREVIOUS WORKS

Performance specification	[14]	[15]	This work
A_0 (dB)	100	100	104
GBW (MHz)	0.59	0.22	0.19
PM (deg.)	43	68	61
SR (V/μsec)	0.23	0.22	0.14
Pdiss. (μW)	400	345	61.25
Total area (μm^2)	230	*	492.15
C_L (pF)	100	100	100
FOM_S	147	63	310
FOM_L	57	63	228
Process (μm)	0.8	0.35	0.18

Also, two Figure of Merits (FOM) are indicated in Table IV as a criterion for comparing the total performance of the amplifiers. One FOM is in small signal is given by:

$FOM_S = GBW \times CL / Power$

And another FOM is in large signal is given by:

$FOM_L = SR \times CL / Power$

The larger FOM indicates better topology for compensation in multistage amplifiers.

As it can be seen, the results obtained by this work are better than other works in the most specifications.

V. CONCLUSION

This paper has presented a CAD tool for automatic design of analog integrated circuits. Artificial neural networks has been applied in order to determine the device sizes in the analog integrated circuits. To evaluate the proposed method, one example was presented. Training data were obtained by various simulations in HSPICE with TSMC 0.18 μm CMOS process parameters. Optimization approach was performed in MATLAB environment and also the circuit was simulated by using HSPICE program in 0.18 μm CMOS technology. The simulation results confirm effectiveness and robustness of proposed method to design and optimize multistage operational amplifiers. Note finally that, the proposed approach is a general method and can be applied to design of other Op-Amp topologies and cell level analog blocks, together with concerning more parameters of the circuit like amount of doping of semiconductor.

REFERENCES

[1] A. Torralba, J. Chavez, and L. G. Franquelo, "FASY: A fuzzy logic based tool for analog synthesis," IEEE Trans. Computer-Aided Design, vol. 15, no. 7, pp. 785−793, July 1996.

[2] M. Fares and B. Kaminska, "FPAD: A fuzzy nonlinear programming approach to analog circuit design," IEEE Trans. Computer-Aided Design, vol. 14, no. 7, pp. 785−793, July 1995.

[3] W. Nye, D. C. Riley, A. Sangiovanni, and A. L. Tits, "DELIGHT.SPICE: An optimization-based system for the design of integrated circuits," IEEE Trans. Computer-Aided Design, vol. 7, no. 4, pp. 501−519, April 1988.

[4] J. M. Shyu and A. Sangiovanni-Vincetelli, "ECSTASY: A new environment for IC design optimization," in Proc. IEEE Inter. Conf. Computer-Aided Design (ICCAD), pp. 484−487, 1988.

[5] J. C. Lai, J. S. Kueng, H. J. Chen, and F. J. Fermandez, "ADOPT – A CAD tool for analog circuit design," IEEE Circ. Devices, vol. 18, no. 2, pp. 29−30, March 1988.

[6] E. S. Ochotta, R. A. Rutenbar, and L. R. Carley, "Synthesis of high performance analog circuits in ASTRX/OBLX," IEEE Trans. Computer-Aided Design, vol. 15, no.

[7] B. Suho and A. Dutta, "Automatic synthesis of CMOS operational amplifiers: A fuzzy optimization approach," 15th International Conference on VLSI Design, 2002.

[8] A. Jafari, M. Zekri, S. Sadri, and A. Mallahzadeh, "Design of analog integrated circuits by using genetic algorithm," 2th International Conference on computer engineering and applications , pp. 578−581, March 2010.

[9] H. Y. Koh, C. H. Sequin, and P. R. Gray, "OPASYN: A compiler for CMOS operational amplifiers," IEEE Trans. Computer-Aided Design, vol. 9, no. 2, pp. 113−125, February 1990.

[10] J. P. Harvey, M. I. Elmasry, and B. Leung, "STAIC: An interactive framework for synthesizing CMOS and BiCMOS analog circuits," IEEE Trans. Computer-Aided Design, vol. 11, no. 11, pp. 1402-1417, November 1992.

[11] M. Taherzadeh, R. Lotfi, H. Zare and O. Shoaei, "Design optimization of analog integrated circuits using simulation-based genetic algorithm", Proc. Signal Circuits and systems Conf, (SCS), pp.73-76, 2003.

[12] B. Sahu and A. Dutta, "A fuzzy logic based approach for parametric optimization of MOS operational amplifiers," ELSEVIER, Microelectronic Journal, no-42, PP.137-148, 2009.

[13] Q. J. Zhang, "Neural Networks for RF and Microwave Design," Artech House, 2000.

[14] K. Leung and P. Mok, "Analysis of Multistage Amplifier-Frequency Compensation," IEEE Trans. Circuits and System, vol. 48, no. 9, pp. 1041−1056, September 2001.

[15] A. D. Grasso, "Analytical comparison of frequency compensation techniques in three-stage amplifiers," International journal of circuit theory and applications, pp. 53−80, December 2006.