

Active Reversed Nested Miller Compensation for Three-Stage Amplifiers

A.D. Grasso, G. Palumbo and S. Pennisi

University of Catania

DIEES - Dipartimento di Ingegneria Elettrica Elettronica e dei Sistemi

Viale Andrea Doria, 6, I-95125 CATANIA – ITALY

Phone: +39-095-7382318; Fax: +39-095-330793; e-mail: [agrasso, gpalumbo, spennisi]@diees.unict.it

Abstract—A novel frequency compensation technique for three-stage amplifiers is introduced. Compared to the traditional reversed nested Miller compensation strategy, the proposed one exploits two active stages already included in the amplifier topology, thus no extra circuitry for its implementation is needed. The technique allows to remove the right-half-plane zero and generates a left-half-plane zero, improving the phase margin. Design equations using the phase margin as design parameter are carried out. The proposed technique is used to design, using a standard CMOS 0.35- μm technology, a 2-V three-stage amplifier driving a 500-pF load. The amplifier dissipates 0.24 mW at DC and achieves a 1.75-MHz gain-bandwidth product.

power consumption. Design equations which allow setting the values of the compensation network elements, for the desired phase margin, are carried out.

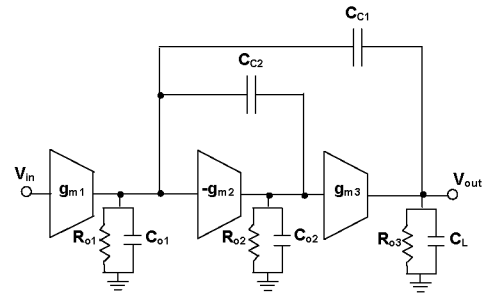


Figure 1. Reversed nested miller compensation topology.

I. INTRODUCTION

The operational transconductance amplifier (OTA) is a basic building block widely used in many applications. With the scale down of transistor dimensions and supply voltages, multistage amplifiers have become increasingly important because they can provide DC-gains in excess of 100 dB and large output swings in low voltage conditions. Nevertheless, the design of such amplifiers is a challenging task since the increased number of high impedance nodes (and, in turn, of low frequency poles) may result in instability. Therefore, many compensation techniques have recently been proposed [1]-[9]. In particular, when the amplifier is made up of three gain stages and the second is the only inverting one, the most suitable option is the reversed nested Miller compensation (RNMC) [1], [6] whose topology is shown in Fig. 1. Unfortunately, the basic RNMC technique exhibits an undesired right-half-plane (RHP) zero which limits the maximum achievable bandwidth. Then, some solutions to remove the RHP zero have been suggested [7]-[9].

In this paper we present a power efficient compensation technique which uses two additional transconductance stages to remove the RHP zero. The compensation network can be implemented without using extra transistors, thus optimizing

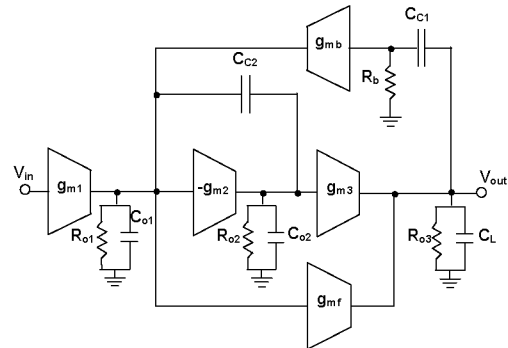


Figure 2. Proposed compensation topology.

II. PROPOSED COMPENSATION TECHNIQUE

The proposed solution is shown in Fig. 2 where g_{mi} , R_{oi} and C_{oi} are the i -th stage transconductance, resistance and equivalent output capacitance, respectively. The compensation is realized by the capacitor C_{C2} connected across the second stage, capacitor C_{C1} connected in series with an additional stage, whose transconductance and input resistance are equal to g_{mb} and R_b , respectively, and the

feedforward stage g_{mf} . Assuming $C_{C1}, C_{C2} \gg C_{o1}, g_{m1}R_{o1} \gg 1, i=1, \dots, 3$, and, as will be clear later, $g_{mb}=1/R_b$, the open-loop transfer function of the circuit in Fig. 2 is expressed by

$$A_v(s) = A_0 \frac{1+s \left[\frac{C_{C1}}{g_{mb}} + \left(\frac{g_{mf}}{g_{m2}g_{m3}} - \frac{1}{g_{m2}} \right) C_{C2} \right] + s^2 \frac{g_{mf} - g_{m3}}{g_{m2}g_{m3}g_{mb}} C_{C1}C_{C2}}{\left(1 + \frac{s}{\omega_{p1}} \right) \left[1 + s \frac{(g_{m2} + g_{mf} - g_{m3})C_{C1} + g_{m2}C_L}{g_{m2}g_{m3}C_{C1}} C_{C2} + s^2 \frac{C_{C2}C_L}{g_{mb}g_{m3}} \right]} \quad (1)$$

where $A_0 = g_{m1}R_{o1}g_{m2}R_{o2}g_{m3}R_{o3}$ is the DC gain and $\omega_{p1} \equiv 1/(C_{C1}R_{o1}g_{m2}R_{o2}g_{m3}R_{o3})$ is the dominant pole. Consequently, the gain-bandwidth product is, as usual, $GBW = g_{m1}/C_{C1}$. The function exhibits two other nondominant poles and two zeroes that can be made both negative by setting $g_{mf} > g_{m3}$. In particular, setting $g_{mf} = g_{m3}$ the s^2 term in the numerator of (1) is set equal to zero and the transfer function is rewritten as

$$A_v(s) = A_0 \frac{1 + s \frac{C_{C1}}{g_{mb}}}{\left(1 + \frac{s}{\omega_{p1}} \right) \left(1 + s \frac{C_{C1} + C_L}{g_{m3}C_{C1}} C_{C2} + s^2 \frac{C_{C2}C_L}{g_{mb}g_{m3}} \right)} \quad (2)$$

and only a LHP zero $z = g_{mb}/C_{C1}$ is left.

Let us now develop some design equations for the proposed compensation technique introducing the phase margin as additional design parameter. Using (2) and (A4) in the Appendix and assuming that $C_{C1} \ll C_L$, the phase margin Φ can be expressed as

$$\tan(\Phi - \Phi_z) = \frac{g_{m3}g_{mb}C_{C1}^2 - g_{m1}^2C_{C2}C_L}{g_{m1}g_{mb}C_{C2}C_L} \quad (3)$$

where $\Phi_z = \tan^{-1}(g_{m1}/g_{mb})$ is the contribution due to the LHP zero. Using (3), the design equation for the compensation capacitor C_{C1} is expressed by

$$C_{C1} = \sqrt{\frac{g_{m1}g_{mb} \tan(\Phi - \Phi_z) + g_{m1}^2}{g_{m3}g_{mb}}} C_{C2}C_L \quad (4)$$

Since capacitor C_{C2} is not connected to the load capacitor, closed-loop stability is achieved for all practical C_{C2} values [1]. Therefore, considering (3) and the expression of GBW , it follows that the lower the value of C_{C2} the better is the amplifier performance. This aspect can be also noted considering the denominator of (2) where the contribution of the pair of complex and conjugate poles to the phase margin is reduced by increasing their pole frequency (diminishing C_{C2}).

The value of g_{mb} cannot be set arbitrarily. In particular, using (2) and (A6) in the Appendix, to ensure asymptotic stability g_{mb} must satisfy the constraint

$$g_{mb} > \frac{C_L}{C_L + C_{C1}} g_{m1} \cong g_{m1} \quad (5)$$

Moreover, it should be noted that if (5) is satisfied, the frequency of the LHP zero is greater than the GBW .

III. SIMULATION RESULTS

The analyzed compensation strategy was exploited to design a three-stage amplifier using a triple-metal double-poly 0.35- μm CMOS process, supplied by AMS. Figure 3 shows the schematic of the OTA used in simulations with Spectre. The input stage is made up of transistors M1-M8 implementing a folded cascode stage. The second inverting stage is made up of common source M9-M10. The last non-inverting stage is realized by transistors M11-M14. In particular, the feedforward transconductance stage g_{mf} is realized through M14 whose gate is connected to the output of the first stage, thus implementing a pseudo class AB output stage which is capable of driving the load capacitor, C_L , with a current much higher than the output branch quiescent current. Finally, the g_{mb} compensation stage in Fig. 2, is simply realized by transistor M6 of the folded cascode input stage.

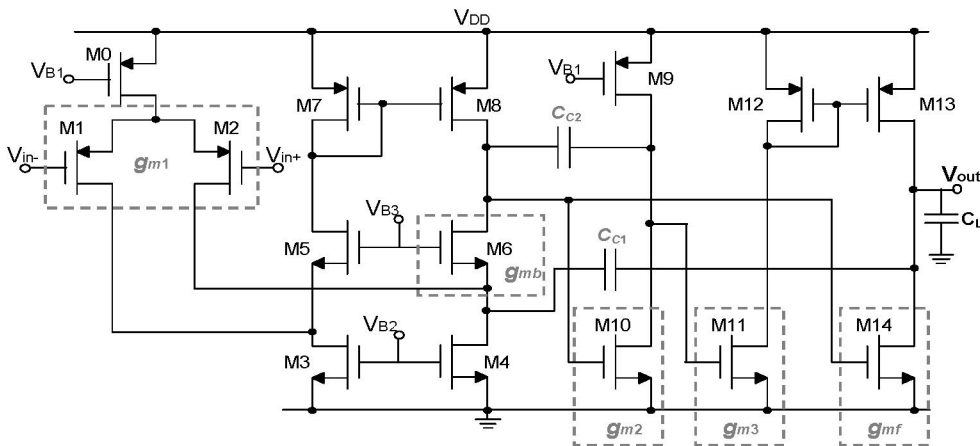


Figure 3. Simplified schematic of the OTA with the proposed compensation network used in simulations.

TABLE I. TRANSISTORS ASPECT RATIOS.

Transistor	Value
M0	100/0.7
M1, M2	20/0.7
M3, M4, M5, M6	120/0.7
M7, M8	60/0.7
M9	100/0.7
M10, M11, M14	40/0.7
M12, M13	60/0.7

Therefore, the proposed compensation strategy does not entail extra circuitry for its implementation, since the transistors of the basic OTA topology are exploited.

Transistors aspect ratios are reported in Table I. The OTA was powered with a 2-V supply and the total current dissipation is 120 μ A. The load capacitance was set equal to 500 pF. The stage transconductances are $g_{m1}=130 \mu\text{A/V}$, $g_{m2}=g_{m3}=g_{mf}=438 \mu\text{A/V}$, $g_{mb}=429 \mu\text{A/V}$ and the compensation capacitors are $C_{C1}=11.5 \text{ pF}$ and $C_{C2}=0.5 \text{ pF}$.

Figure 4 shows the OTA open-loop frequency response. The GBW and the phase margin are equal to 1.75 MHz and 59° , respectively. The basic RNMC amplifier shown in Fig. 1 was designed using the same transistors aspect ratios and quiescent currents (i.e. the same transconductances). The frequency response is shown in Fig. 4 as well. It can be seen that the phase margin reduces to 40° , therefore to achieve a phase margin of 60° a greater value of C_{C1} should be used. The time response of the amplifier in unity-gain configuration to a 500-mV_{pp} input step is shown in Fig. 5.

The OTA main performance parameters are summarized in Table II. To provide a performance comparison between the proposed compensation technique and other reported compensation topologies two figures of merit, $FOM_S=(GBW \cdot C_L)/\text{Power}$ and $FOM_L=(SR \cdot C_L)/\text{Power}$, are commonly used [4], [5]. The higher the value of the figures of merit, the better is the amplifier performance. The values of the figures of merit of different three-stage amplifiers are reported in Table III. It can be seen that the proposed compensation techniques outperforms all the other previously reported nested and reversed-nested Miller topologies.

TABLE II. MAIN PERFORMANCE PARAMETERS.

Parameter	Value
Power Supply	2V
Total Bias Current	120 μ A
Loading Capacitance	500 pF
DC Gain	117 dB
Gain-bandwidth Product	1.75 MHz
Phase Margin	59°
Gain Margin	12 dB
Positive/Negative Slew Rate	1.37/1.67 V/ μ s
Positive/Negative 1% Settling Time	472/459 ns

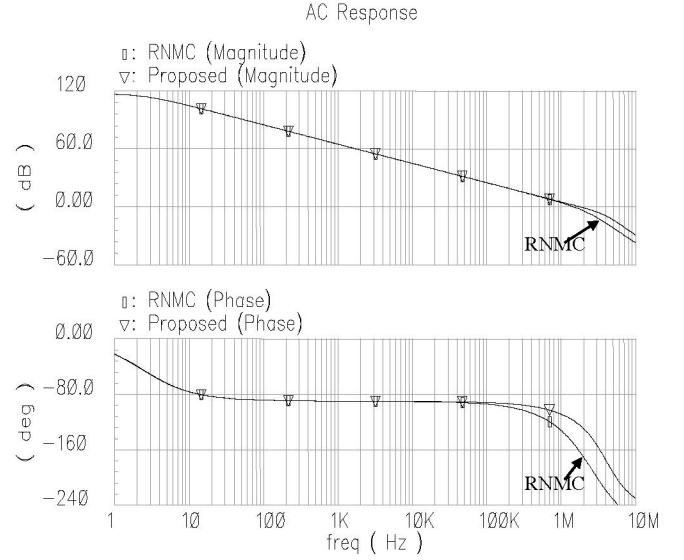


Figure 4. Open-loop frequency response.

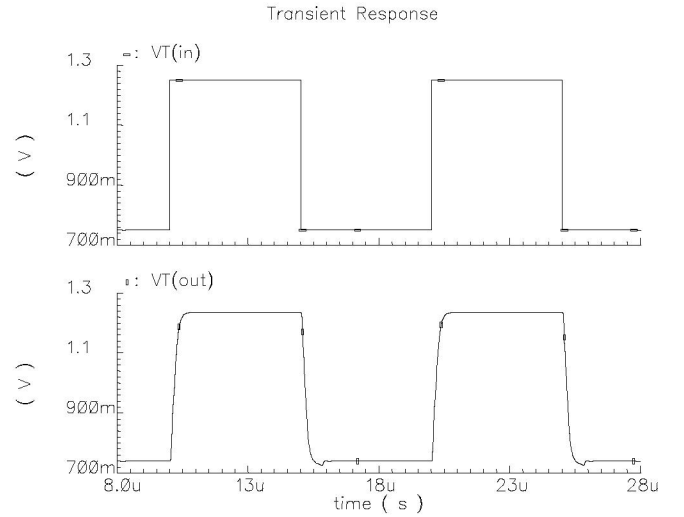


Figure 5. Unity-gain buffer transient response .

IV. CONCLUSION

A novel compensation technique for three-stage OTAs with only the second stage inverting is developed. Design equations introducing the phase margin as main design parameter were carried out. The proposed compensation strategy can be implemented using the transistors of the basic OTA topology, thus optimizing power consumption. Simulation results on a 2-V three-stage amplifier driving a 500-pF load are given to confirm the advantages of the compensation strategy. The proposed amplifier is currently being fabricated using a standard 0.35- μ m process supplied by AMS and measurement will be executed in the near future.

TABLE III. PERFORMANCE COMPARISON OF DIFFERENT AMPLIFIERS.

	RNMC with VB [7] ^a	RNMC with CB [7] ^a	RNMC with VB and NR [8]	NFRNMC [9] ^a	CFRNM [9] ^a	AFFC [4]	ACBC _F [5]	This work^a
C_L (pF)	10	10	15	120	120	120	500	500
GBW (MHz)	4.5	4.5	19.46	2.5	2.5	4.5	1.9	1.75
SR (V/ μ s) ^b	2.3	2.3	13.8	–	–	1.49	1	1.52
$Power$ (mW@ V_{DD})	0.083@1.5	0.083@1.5	1.4@3	0.36@2	0.40@2	0.40@2	0.324@2	0.24@2
FOM_S (MHz·pF/mW)	542	542	209	833	750	1350	2932	3645
FOM_L (V/ μ s·pF/mW)	277	277	149	–	–	447	1543	3166

a. simulated
b. average value

V. APPENDIX

Let $A_v(s)$ represent the open-loop transfer function of a generic three-stage amplifier

$$A_v(s) = A_0 \frac{1 + s b_1 + s^2 b_2}{\left(1 + \frac{s}{\omega_{p1}}\right)(1 + s a_1 + s^2 a_2)} \quad (A1)$$

The phase margin Φ is expressed by [1]

$$\Phi = 180^\circ - \tan^{-1}\left(\frac{GBW}{\omega_{p1}}\right) - \tan^{-1}\left(\frac{a_1 GBW}{1 - a_2 GBW^2}\right) + \tan^{-1}\left(\frac{b_1 GBW}{1 - b_2 GBW^2}\right) \quad (A2)$$

Since $\omega_{p1} \ll GBW$, (A2) can be approximated by

$$\Phi = \tan^{-1}\left(\frac{1 - a_2 GBW^2}{a_1 GBW}\right) + \tan^{-1}\left(\frac{b_1 GBW}{1 - b_2 GBW^2}\right) \quad (A3)$$

Finally, denoting Φ_z the contribution of the numerator of (A1), the following relation is obtained

$$\tan(\Phi - \Phi_z) = \frac{1 - a_2 GBW^2}{a_1 GBW} \quad (A4)$$

Now let us develop a general expression for the stability of a generic three-stage amplifier whose open-loop transfer function can be expressed as (A1). Neglecting the zeroes, the closed-loop transfer function in unity-gain configuration is given by

$$A_{v,cl}(s) = A_0 \frac{1}{1 + s \frac{1}{GBW} + s^2 \frac{a_1}{GBW} + s^3 \frac{a_2}{GBW}} \quad (A5)$$

Since the order of the numerator of (A5) is less than the order of its denominator, the stability is determined only by the denominator [5], [9]. Therefore, by applying the Routh-Hurwitz stability criterion [10] on (A5), the following relation is carried out

$$a_1 > a_2 GBW \quad (A6)$$

It is worth noting that (A6), which states a condition for the unconditional stability, expresses a constraint on the maximum intrinsically achievable gain-bandwidth product of the amplifier.

REFERENCES

- [1] G. Palumbo, S. Pennisi, *Feedback Amplifiers: theory and design*, Kluwer Academic Publishers, Boston, 2002.
- [2] G. Palumbo, S. Pennisi, "Design Methodology and Advances in Nested-Miller Compensation", *IEEE Trans on Circuits and Systems - part I*, Vol. 49, No. 7, pp. 893-903, July 2002.
- [3] K. N. Leung, P. K. T. Mok, "Analysis of Multistage Amplifier-Frequency Compensation", *IEEE Trans on Circuits and Systems - part I*, Vol. 48, No. 9, pp. 1041-1056, September 2001.
- [4] H. Lee, P. K. T. Mok, "Active-Feedback frequency-compensation technique for low-power multistage amplifiers," *IEEE J. Solid-State Circuits*, Vol. 38, pp. 511-520, March 2003.
- [5] X. Peng, W. Sansen, "AC Boosting Compensation Scheme for Low-Power Multistage Amplifiers", *IEEE J. Solid-State Circuits*, Vol. 39, pp. 2074-2077, November 2004.
- [6] R. G. H. Eschauzier, J. H. Huijsing, *Frequency Compensation Techniques for Low-Power Operational Amplifiers*, Kluwer Academic Publishers, Boston, 1995.
- [7] R. Mita, G. Palumbo, S. Pennisi, "Design Guidelines for Reversed Nested Miller Compensation in Three-Stage Amplifiers", *IEEE Trans on Circuits and Systems - part II*, Vol. 50, No. 5, pp. 227-233, May 2003.
- [8] K.-P. Ho, C.-F. Chan, C.-S. Choy, K.-P. Pun, "Reversed Nested Miller Compensation with Voltage Buffer and Nulling Resistor" *IEEE J. Solid-State Circuits*, Vol. 38, pp. 1735-1738, October 2003.
- [9] F. Zu, S. Yan, J. Hu, E. Sanchez-Sinencio, "Feedforward Reversed Nested Miller Compensation Techniques for Three-Stage Amplifiers," *Proc. IEEE ISCAS '05*, Vol. 1, pp. 2575-2578, May 2005.
- [10] T. Kailath, *Linear Systems*, Prentice-Hall, New Jersey, 1980.