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RESEARCH ARTICLE

Novel Methods for Improved Particle Swarm Optimization in Designing the Bandgap Reference Circuit

TRANG HOANG^{1,2}, THANG NGUYEN QUOC^{1,2,3},
LIHONG ZHANG³, (Senior Member, IEEE), AND TRUNG Q. DUONG^{3,4}, (Fellow, IEEE)

¹Department of Electronics, Faculty of Electrical and Electronics Engineering, Ho Chi Minh City University of Technology (HCMUT), Ho Chi Minh City, Vietnam

²Vietnam National University Ho Chi Minh City, Ho Chi Minh City, Vietnam

³Department of Electrical and Computer Engineering, Faculty of Engineering and Applied Science, Memorial University of Newfoundland, St. John's, NL A1B 3X9, Canada

⁴School of Electronics, Electrical Engineering and Computer Science, Queen's University Belfast, BT7 1NN Belfast, U.K.

Corresponding author: Trang Hoang (hoangtrang@hcmut.edu.vn)

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ABSTRACT Bandgap reference (BGR) circuits play a crucial role as voltage reference generators for other components within a variety of analog integrated circuits. Therefore, their power supply rejection ratio (PSRR), which represents the BGR's ability to maintain a stable output in the presence of supply ripples, has a substantial impact on the overall circuit performance and is consequently worthy of attention. In this work, the design of a 65nm-CMOS BGR circuit and the computational approach to optimize its PSRR value are presented. Our proposed BGR circuit incorporates a modification in the op-amp structure to enhance the PSRR parameter. Detailed explanations of the proposed op-amp's differential gain calculation and the PSRR parameter formula are provided. Additionally, we employ the particle swarm optimization (PSO) algorithm to maximize PSRR while satisfying other specifications. Four distinct approaches for utilizing the inertia weight parameter of the PSO algorithm are explored: two newly developed techniques (PSO - local exploitation orienter (PSO-LEO) and PSO - global exploration orienter (PSO-GEO)) together with two conventional approaches. A comprehensive comparative analysis reveals the superiority of our proposed PSO-GEO technique. Ultimately, our 65 nm CMOS bandgap circuit exhibits exceptional performance, featuring a temperature coefficient of 6.4056 ppm/°C and a PSRR of 99.9896 dB at 1 kHz. In conclusion, this work contributes substantially through op-amp architecture modification, PSRR optimization via the PSO algorithm, and introducing new inertia weight parameter utilization strategies and analyzing them.

INDEX TERMS Analog circuit optimization, bandgap reference circuit, PSO algorithm, power supply rejection ratio.

I. INTRODUCTION

Bandgap reference (BGR) circuits, whose purpose is to provide a precise reference voltage or bias current to other blocks, have become one of the core modules in several analog circuits [1]. One of the first and most popular BGR topologies was introduced by Brokaw in 1974. In this topology, zero-temperature-coefficient (zero-TC) voltage

is generated by taking the sum of the proportional-to-absolute-temperature (PTAT) voltage and a complementary-to-absolute-temperature (CTAT) one [2]. However, the Brokaw topology cannot work if the supply voltage is below 1.5 V, and it also cannot generate a reference voltage below 1.2 V [3]. Several sub-1V BGR structures are proposed in [4], [5], and [6] to remedy these problems.

Thanks to the ability to produce a PVT-independent voltage, especially under the sub-1V power supply, BGR has been integrated into data converters and power management

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circuits as a reference voltage generator [7]. In analog devices, the stability of the reference voltage generated by the BGR block plays a vital role in the performance of the whole circuit. By way of illustration, the output voltage of the low-dropout regulator (LDO) linearly depends on the reference voltage [8]. Consequently, the ripple of BGR's output voltage directly affects the accuracy of LDO's output, which may affect the performance of the IC that uses LDO as the power supply. Due to the importance of the voltage reference's accuracy to the whole circuit's operation, studies on BGR mainly focus on optimizing its ripple rejection ability, which is quantified by the power supply rejection ratio (PSRR).

In the BGR topology introduced in [2], an op-amp is required to generate a temperature-independent current. Additionally, the op-amp has a notable impact on the PSRR of the BGR circuit. The higher the gain of the op-amp, the higher the value of the PSRR [9]. In [2], the op-amp is realized as a five-transistor operational transconductance amplifier (OTA). Nevertheless, the differential gain of five-transistor OTA typically has a value of less than 25 dB [10]. To achieve a higher gain, OTA can be cascaded with a common-source amplifier to form a multi-stage amplifier. However, to ensure the feedback loop's stability, the multi-stage amplifier requires a large capacitor and high bias current for phase compensation [10]. To overcome this issue, in this work, a differential amplifier with cascode load, which can achieve a higher gain without the requirement of high bias current or large coupling capacitor, is proposed to be used as an op-amp in the BGR circuit. The small-signal calculations for the proposed op-amp's differential gain are presented in this paper. For further optimization purposes, the formula representing the dependency of the PSRR parameter on the op-amp's gain and the transistors is also presented. These are the first contributions of this study.

Another aspect under consideration in this research concerns the optimization procedure. Given the significance of the PSRR parameter, our objective is to maximize its value while concurrently ensuring the satisfaction of other specifications. This endeavor may not be straightforward. Due to the complexity of the relationship between the CMOS device's geometry parameters and electrical specifications and the intricate trade-offs between specifications, it often entails a significant number of iterations involving device resizing and simulation to attain an optimal solution that not only maximizes (or minimizes) a specific parameter but also ensures compliance with all constraints [11]. The more complex the circuit is, the greater the time and effort required for the optimization process. In order to address the time and labor-intensive nature of analog IC sizing, there has been a growing trend in utilizing optimization algorithms for the automated circuit sizing process [12]. Equation-based optimization methods, such as deterministic, statistical, and gradient-based approaches, have been adopted in circuit sizing problem-solving [13], [14], [15]. However,

when applied to complex circuit sizing challenges, these methods encounter significant limitations. First, they require mathematical functions describing the relationship between transistors dimensions and circuit performance metrics. These functions are often complex and challenging to derive accurately. Second, equation-based methods typically require the optimization problems to be convex, which means that both the objective and constraint functions must be convex. To tackle these challenges, approximations can be used to simplify the mathematical formulation process and transform a non-convex optimization problem to a convex form. However, these approximations may neglect the high-order effects in CMOS circuits, which become more pronounced as the technology node shrinks [16]. Therefore, equation-based methods may exhibit reduced effectiveness in the field of analog circuit design. As a promising alternative to equation-based methods, Bayesian optimization can handle non-convex problems and requires no explicit knowledge of the circuit model. However, Bayesian optimization is limited due to its inherent inability to evaluate its non-convex multi-modal acquisition function in high-dimensional scenarios [17]. This limitation necessitates the use of supplementary algorithms to identify the peak value of the acquisition function and strike a balance between exploration and exploitation, leading to a significant increase in computational costs [17], [18], [19].

To address the limitations of conventional methods, researchers have developed several modern computational strategies inspired by natural phenomena, known as nature-inspired algorithms. These novel approaches offer a rapid and cost-effective means of finding quasi-optimal solutions for large-scale complex problems, without the need for mathematical descriptions [20]. One prominent algorithm within these categories is the particle swarm optimization (PSO) algorithm. PSO has a history of practical applications in various real-world scenarios, thanks to its appealing attributes, which encompass robustness, straightforward representation, a reduced number of tunable parameters, the ease of executing parallel computations, and swift computational performance [21], [22], [23], [24]. Specifically, compared to other nature-inspired algorithms such as simulated annealing, genetic algorithm and differential evolution, PSO offers several distinct advantages. Firstly, its parallel computing capability allows PSO to reach a solution faster, needing fewer iterations than simulated annealing [25]. Secondly, PSO is simpler to adjust than simulated annealing and genetic algorithm, as it has fewer adjustable parameters [24], [26]. Thirdly, PSO does not necessitate the intricate encoding, decoding, and genetic operators that genetic algorithm does, which makes the programming and optimization process easier [26]. Additionally, unlike other nature-inspired algorithms such as genetic algorithm and differential evolution, PSO's processing time is less sensitive to population size. Finally, the PSO algorithm significantly amplifies the impact of the best solution within the population, accelerating convergence

and outperforming both genetic algorithm and differential evolution in this regard [27]. Due to these notable benefits, the PSO algorithm has been selected in this study to address the aforementioned problem of optimizing the PSRR parameter in the design of BGR circuits.

Our proposed PSO-based solution comprises two primary components. The first component, termed the “circuit block”, encompasses the BGR’s schematic drawing, which serves as the input for generating the circuit netlist, and the circuit simulator, employed to simulate the circuit’s behavior based on the netlist. The second component, called the “optimization block”, involves the definition of the fitness function, which represents the goal of optimization, and the implementation of the PSO algorithm in the Python programming language. Over iterative cycles, the PSO algorithm progressively reduces the value of the fitness function to achieve convergence. Serving as a communication channel between these two blocks is a scripting program coded in Ocean language. This program translates the positions of PSO particles into the geometric dimensions of transistors employed in the BGR circuit. Subsequently, it performs simulations to acquire essential data, which are then relayed to the optimization core for the calculation and evaluation of the fitness function.

In the PSO algorithm, the inertia weight parameter is utilized to regulate particle movement, where higher values encourage exploration and lower values promote exploitation. Previous research indicates that dynamically reducing this parameter during iterations can enhance PSO’s performance compared to a fixed setting [21]. However, within the field of analog IC design optimization, there is a notable absence of investigations related to PSO’s inertia weight reduction. The authors in [22] and [28] have exclusively introduced the linear decremental inertia weight PSO method for area minimization in two-stage operational amplifiers, but these studies lack comparisons with the conventional PSO approach. To address the limited utilization of the PSO inertial weight reduction method in the field of analog IC design, in this paper, we introduce two innovative exponential inertia weight reduction techniques, denoted as PSO - local exploitation orienter (PSO-LEO) and PSO - global exploration orienter (PSO-GEO). These techniques are applied to tackle the BGR optimization problem, alongside the pre-existing fixed and linear decremental methods. Then, to rectify the absence of comparative analysis, five criteria for comparison between the four aforementioned PSO approaches, namely success rates, best fitness values achieved, mean value, standard deviation, and convergence rate, are performed. The comparison result reveals that our proposed PSO-GEO, with its global search capability across the entire design space, excels in discovering the global optimum solution, compared to PSO-LEO and the other two methods.

The subsequent sections of this paper are structured as follows: Section II delineates the schematic design of the BGR circuit and the requisite calculations. Section III

TABLE 1. Important notations and definitions.

Notation	Definition
1. Notations related to the design variables	
w_{m1_pcasc}	Geometric width of transistors in the 1 st cascode stage
w_{m2_pcasc}	Geometric width of transistors in the 2 nd cascode stage
w_{pbias}	Geometric width of M1A_PBIAS
w_{nbias}	Geometric width of M3A_NBIAS, M3B_NBIAS, M _{tail}
w_{pdiff}	Geometric width of M2, M5
w_{ndiff}	Geometric width of M1, M4
l_{ndiff}	Geometric width of M1, M4
2. Notations related to the small-signal calculation	
g_1, r_1	Transconductance, channel resistance of transistors in the 1 st cascode stage
g_{1b}, r_{1b}	Transconductance, channel resistance of M1B_PBIAS
R_b	Resistance of M3B_NBIAS
g_A	Transconductance of M3A_NBIAS
R_{ts}	Resistance of M1A_PBIAS + M2A_PBIAS
r_{eQ1}, r_{eQ2}	Small signal resistance of Q1 and Q2
R_X	$R_{CTAT} \parallel r_{eQ1}$
R_Y	$R_{CTAT} \parallel (R_{PTAT} + r_{eQ2})$
3. Notations related to the PSO algorithm implementation	
ω	Inertia weight
$\omega_{max}, \omega_{min}$	Maximum, minimum value of inertia weight
c_1, c_2	Acceleration coefficients
T	Total number of iterations
α	Local exploitation orienter decrement constant
β	Global exploration orienter decrement constant
P_{best}	The best fitness value that a particle has found so far
G_{best}	The best position found so far by the entire swarm.

provides an overview of the PSO algorithm. In Section IV, we detail the formulation of the problem for optimizing BGR design and using the PSO-based solution. Additionally, this section elucidates the implementation of four distinct approaches for inertia weight reduction within the PSO framework, encompassing the established fixed inertia weight method, the linearly decreasing method, and our newly introduced PSO-LEO and PSO-GEO techniques. In Section V, the optimization outcomes obtained using these four distinct approaches are presented. A comprehensive comparative analysis of these results is performed, and the circuit’s performance is evaluated relative to prior studies. Finally, Section VI concludes the paper. To assist the reader throughout this paper, essential definitions and notations are given in Table 1.

II. BANDGAP REFERENCE CIRCUIT DESIGN

The schematic of the proposed BGR circuit is depicted in Figure 1. The circuit comprises four terminals, namely VDDIO, VSS, V_{REF} , V_{casc} , and Out_{opamp}, which serve as input/output connections. The operational principle of the BGR circuit, as well as its constituent subcircuits, namely the bandgap core, self-bias circuit, and startup circuit, will be elucidated in the subsequent subsections for comprehensive understanding.

A. BANDGAP CORE

The schematic of the bandgap core block is illustrated in Figure 1. In this circuit, cascode current source (whose first and second stages are rounded by dashed rectangular) is

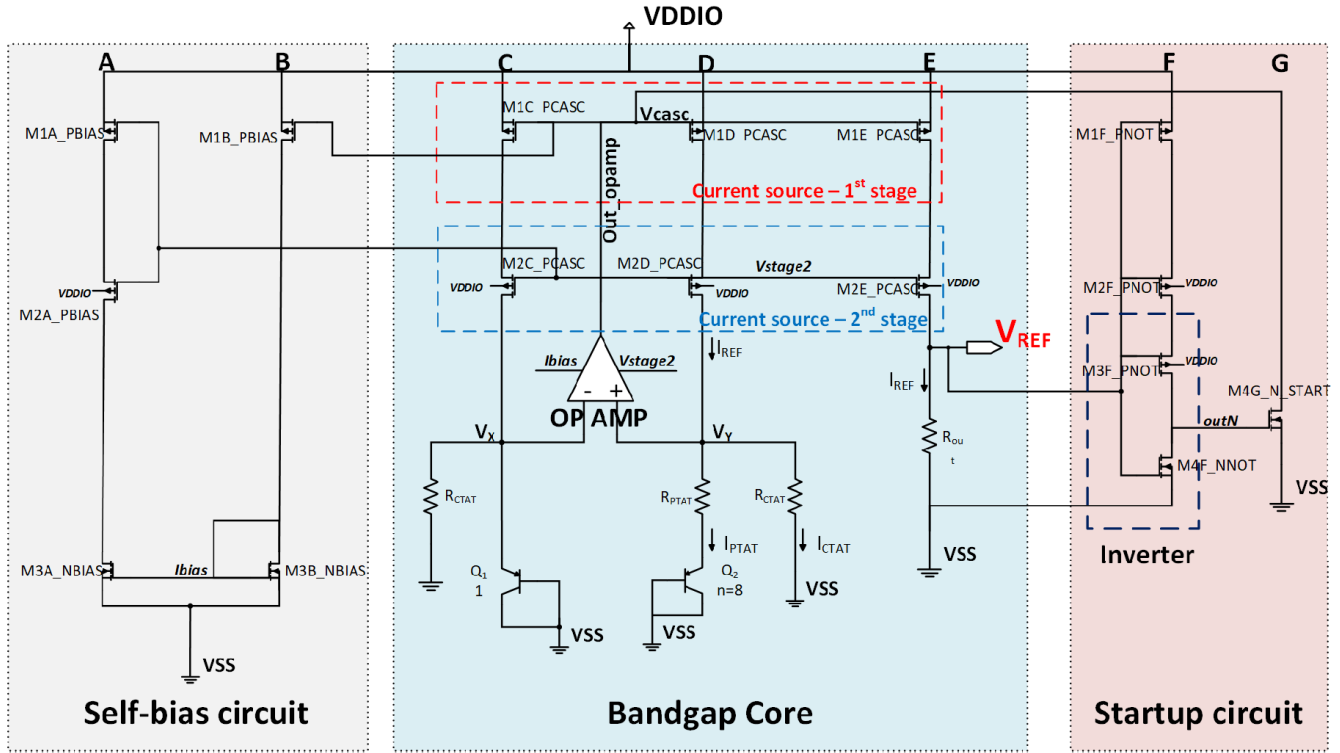


FIGURE 1. Proposed BGR circuit.

employed to ensure the similarity of the current flowing through branches C, D, and E.

The base-emitter voltage difference of the diode-connected PNP BJT used in this circuit can be expressed as (1):

$$V_{EB} = V_T \ln \left(\frac{I_C}{I_S} \right) = \frac{kT}{q} \ln \left(\frac{I_C}{bT^{4+m} e^{-\frac{E_g}{kT}}} \right), \quad (1)$$

where $k = 1.38 \times 10^{-23}$ J/K is Boltzmann constant, $q = 1.6 \times 10^{-19}$ C is the elementary charge, T is the absolute temperature, I_C is the collector current of BJT, I_S is the saturation current of BJT, $m \approx 3/2$ and $E_g = 1.12$ eV is the bandgap energy of silicon.

Taking the partial derivative of (1) with respect to T , we have:

$$\begin{aligned} \frac{\partial V_{EB}}{\partial T} &= \frac{\partial}{\partial T} \frac{kT}{q} \ln \left(\frac{I_C}{bT^{4+m} e^{-\frac{E_g}{kT}}} \right) \\ &+ \frac{kT}{q} \frac{\partial}{\partial T} \left(\ln \left(\frac{I_C}{bT^{4+m} e^{-\frac{E_g}{kT}}} \right) \right) \\ \Rightarrow \frac{\partial V_{EB}}{\partial T} &= \frac{V_{EB} - (4+m)V_T - E_g/q}{T}. \end{aligned} \quad (2)$$

At a temperature of 300 K, $\partial V_{EB}/\partial T$ is approximately -1.5 mV/K, indicating a negative trend. This characteristic enables V_{EB} to serve as a basis for generating a complementary-to-absolute-temperature (CTAT) quantity.

In Figure 1, the bandgap core has two BJTs Q1 and Q2. The emitter area of Q2 is n times larger than Q1. For layout purposes, in this proposed circuit, we choose $n=8$. The difference between the V_{EB} of Q1 and Q2 is:

$$\Delta V_{EB} = V_{EB1} - V_{EB2} = \frac{kT}{q} \ln(n) \quad (3)$$

$$\Rightarrow \frac{\partial(\Delta V_{EB})}{\partial T} = \frac{k}{q} \ln(n) > 0. \quad (4)$$

It was recognized from (4) that if two BJTs are working at unequal current densities, the difference between their base-emitter voltages is proportional to absolute temperature (PTAT). In the proposed BGR circuit, the op-amp is employed in the bandgap core to make a voltage drop on R_{PTAT} equal to ΔV_{EB} .

By applying V_{EB} and ΔV_{EB} on resistors, CTAT and PTAT current can be generated, respectively. To have a zero-temperature-coefficient, PTAT and CTAT quantities are added together:

$$\begin{aligned} I_{REF} &= \frac{V_{EB1}}{R_{CTAT}} + \frac{V_T \ln(n)}{R_{PTAT}} \\ &= \frac{1}{R_{CTAT}} \left(V_{EB1} + \frac{R_{CTAT}}{R_{PTAT}} \times \frac{kT}{q} \ln(n) \right). \end{aligned} \quad (5)$$

To be temperature-independent, I_{REF} must satisfy the condition expressed in (6):

$$\frac{\partial I_{REF}}{\partial T} = 0 \Leftrightarrow \frac{R_{CTAT}}{R_{PTAT}} = -\frac{\partial V_{EB1}}{\partial T} \frac{q}{k \times \ln(n)}. \quad (6)$$

To calculate R_{CTAT}/R_{PTAT} , it is necessary to calculate $\partial V_{EB1}/\partial T$. This was achieved through a DC simulation, where a constant current of $I_E = 11 \mu A$ was applied to the BJT emitter terminal, and the base-emitter voltage difference V_{EB} was recorded while the temperature ranged from $-40^\circ C$ to $125^\circ C$. The simulation results provided $\partial V_{EB1}/\partial T \approx -1.800 \text{ mV}/^\circ C$.

After having $\partial V_{EB1}/\partial T$ value, R_{CTAT}/R_{PTAT} can be calculated based on Equation 6:

$$\frac{R_{CTAT}}{R_{PTAT}} = -\frac{\partial V_{EB1}}{\partial T} \frac{q}{k \times \ln(n)} \approx 10.045 \quad (7)$$

From (5), we have:

$$\begin{aligned} R_{CTAT} &= \frac{1}{I_{REF}} \left(V_{EB1} + \frac{R_{CTAT}}{R_{PTAT}} \times \frac{kT}{q} \ln(n) \right) \\ &= \frac{1.2426 \text{ V}}{30 \mu A} \approx 41.42 \text{ k}\Omega \end{aligned} \quad (8)$$

From (7) and (8), we have:

$$R_{PTAT} = \frac{R_{CTAT}}{R_{CTAT}/R_{PTAT}} \approx 4.123 \text{ k}\Omega \quad (9)$$

To create a zero-TC voltage V_{REF} , current I_{REF} is passed through a resistor R_{out} . To let $V_{REF} = 0.8 \text{ V}$, the value of R_{out} is:

$$R_{out} = \frac{V_{REF}}{I_{REF}} = \frac{0.8 \text{ V}}{30 \mu A} = 26.667 \text{ k}\Omega \quad (10)$$

From the TSMC 65nm library, rppolywo_m is chosen as the resistor for use in bandgap core, since its slight variation with PVT conditions, and it can reach a high resistance value (about $40 \text{ k}\Omega$) with a suitable size ($W/L = 1 \mu m/50 \mu m$).

Table 2 presents the width and length of the devices employed in the bandgap core. To maintain uniformity in the current flowing through each branch, the transistors M1C_PCASC, M1D_PCASC, and M1E_PCASC are matched, as well as the transistors M2C_PCASC, M2D_PCASC, and M2E_PCASC. The widths of the transistors in the cascode current source are presented as variables for the further optimization process.

B. OP-AMP CIRCUIT

The op-amp plays a crucial role in the BGR circuit by enforcing the condition $V_X = V_Y$. This condition, in turn, facilitates the generation of PTAT current that flows through R_{PTAT} . Another function of the op-amp is to increase the value of PSRR, which will be proved in the subsequent section.

Figure 2 illustrates the configuration of a differential amplifier with cascode load. This topology offers distinct advantages over the traditional two-stage op-amp design.

TABLE 2. Size of devices used in bandgap core.

Device	Size (W/L)
M1C_PCASC	w_m1_pcasc/1.5 μm
M1D_PCASC	w_m1_pcasc/1.5 μm
M1E_PCASC	w_m1_pcasc/1.5 μm
M2C_PCASC	w_m2_pcasc/1.0 μm
M2D_PCASC	w_m2_pcasc/1.0 μm
M2E_PCASC	w_m2_pcasc/1.0 μm
Q1	Emitter area = $10 \mu m \times 10 \mu m$
Q2	Emitter area = $10 \mu m \times 10 \mu m$, n = 8
R_{CTAT}	1 $\mu m/55 \mu m$
R_{PTAT}	2 $\mu m/12.12 \mu m$
R_{out}	1 $\mu m/36.41 \mu m$

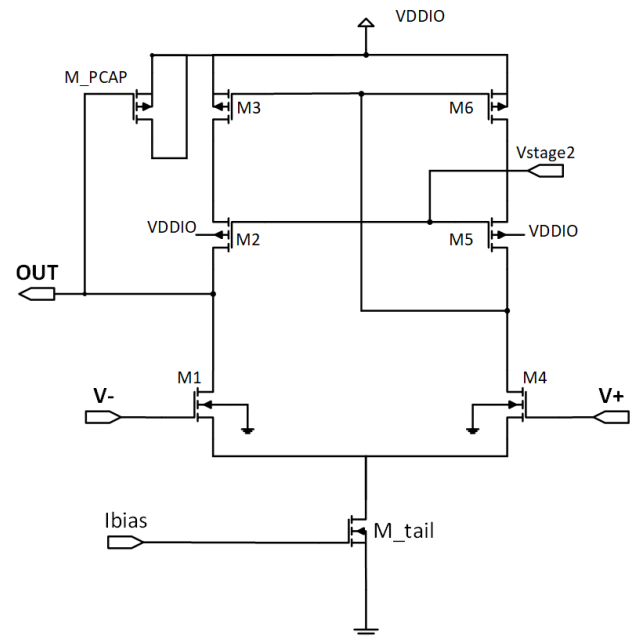


FIGURE 2. Proposed op-amp circuit.

Firstly, it enables the attainment of higher gain by utilizing MOSFETs of the same size and bias current. Secondly, it requires a reduced capacitor size to enhance the phase margin, thereby improving overall performance.

The proposed op-amp design employs matched MOSFETs within each stage, namely M1 and M4, M2 and M5, and M3 and M6. Additionally, the M_PCAP transistor is incorporated as a capacitor element to enhance the op-amp's phase margin and gain margin.

The small-signal model for the proposed op-amp is illustrated in Figure 3. In Figure 3, $g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{2I_D}{|V_{GS}| - V_{TH}}$ is the transconductance of each MOSFET, and $r_o = \frac{\partial V_{DS}}{\partial I_D} = \frac{1}{\lambda I_D} \sim \frac{1}{L \times I_D}$ is the channel resistance of each MOSFET.

Applying the superposition theorem, the formula to determine the differential gain of the op-amp can be calculated.

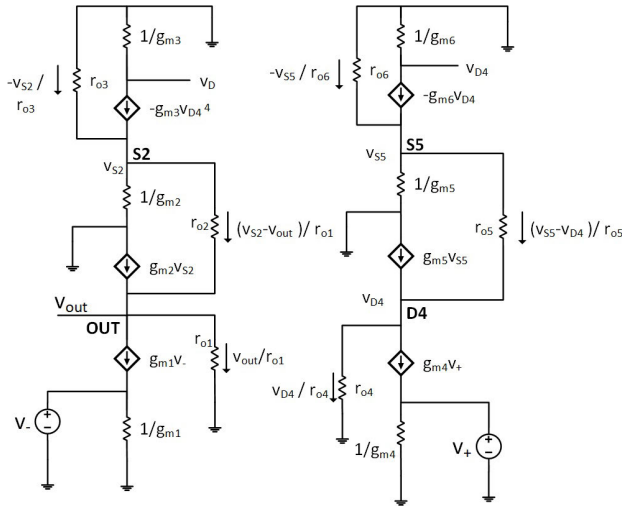


FIGURE 3. Small-signal model for proposed op-amp.

- Let $v_+ = \frac{v_d}{2}$ and $v_- = 0$

Applying KCL at node S5 and D4 respectively:

$$\begin{cases} -g_{m6}v_{D4} - \frac{v_{S5}}{r_{o6}} = g_{m5}v_{S5} + \frac{v_{S5} - v_{D4}}{r_{o5}} \\ g_{m5}v_{S5} + \frac{v_{S5} - v_{D4}}{r_{o5}} = g_{m4}v_+ + \frac{v_{D4}}{r_{o4}} \end{cases} \quad (11)$$

$$\Rightarrow v_{D4} = -\frac{g_{m4}v_+}{g_{m6} + \frac{1}{r_{o4}} + \frac{-g_{m6} + 1/r_{o5}}{1 + g_{m5}r_{o6} + \frac{r_{o6}}{r_{o5}}}}$$

Applying KCL at node S2 and OUT respectively:

$$\begin{cases} g_{m2}v_{S2} + \frac{v_{S2} - v_{out}^+}{r_{o2}} = \frac{v_{out}^+}{r_{o1}} \\ -\frac{v_{S2}}{r_{o3}} - g_{m3}v_{D4} = g_{m2}v_{S2} + \frac{v_{S2} - v_{out}^+}{r_{o2}} \end{cases}$$

$$\Rightarrow v_{out}^+ = \frac{-g_{m3}}{\frac{1}{r_{o1}} + g_{m3} \times \frac{1 + r_{o2}/r_{o1}}{1 + g_{m2}r_{o2}}} v_{D4}$$

$$\Rightarrow v_{out}^+ = \frac{g_{m3}}{\frac{1}{r_{o1}} + g_{m3} \times \frac{1 + r_{o2}/r_{o1}}{1 + g_{m2}r_{o2}}} \frac{g_{m4}}{g_{m6} + \frac{1}{r_{o4}} + \frac{-g_{m6} + 1/r_{o5}}{1 + g_{m5}r_{o6} + \frac{r_{o6}}{r_{o5}}}} v_+$$

Since $\frac{1}{r_o} \ll g_m$, we can make an approximation:

$$v_{out}^+ \approx \frac{g_{m3}}{\frac{1}{r_{o1}} + g_{m3} \times \frac{1 + r_{o2}/r_{o1}}{g_{m2}r_{o2}}} \times \frac{g_{m4}}{g_{m6} + \frac{-g_{m6}}{g_{m5}r_{o6}}} v_+$$

Since $g_{m3} = g_{m6}$ and $g_{m4} = g_{m1}$, we have:

$$v_{out}^+ \approx \frac{g_{m1}}{\frac{1}{r_{o1}} + \frac{g_{m3}}{g_{m2}} \left(\frac{1}{r_{o1}} + \frac{1}{r_{o2}} \right)} v_+ \quad (12)$$

- Let $v_+ = 0$ and $v_- = -\frac{v_d}{2}$

From Equation (11) $\Rightarrow v_{D4} = 0$

KCL at node S2 and node OUT respectively:

$$\begin{cases} -\frac{v_{S2}}{r_{o3}} = g_{m2}v_{S2} + \frac{v_{S2} - v_{out}^-}{r_{o2}} \\ g_{m2}v_{S2} + \frac{v_{S2} - v_{out}^-}{r_{o2}} = g_{m1}v_- + \frac{v_{out}^-}{r_{o1}} \end{cases}$$

$$\Rightarrow v_{out}^- = \frac{-g_{m1}}{\frac{1}{r_{o1}} + \frac{1}{g_{m2}r_{o2}r_{o3} + r_{o2} + r_{o3}}} v_-$$

Since $g_{m2}r_{o2}r_{o3} \gg r_o$, we have:

$$v_{out}^- = -g_{m1}g_{m2}r_{o2}r_{o3} \times v_- \quad (13)$$

Take the sum of Equation (12) and Equation (13), we have:

$$v_{out} \approx g_{m1} \left(g_{m2}r_{o2}r_{o3} + \frac{1}{\frac{1}{r_{o1}} + \frac{g_{m3}}{g_{m2}} \left(\frac{1}{r_{o1}} + \frac{1}{r_{o2}} \right)} \right) \times \frac{v_d}{2}.$$

Differential gain of proposed op-amp is equal to:

$$A_d = \frac{v_{out}}{v_d} \approx \frac{g_{m1}}{2} \left(g_{m2}r_{o2}r_{o3} + \frac{1}{\frac{1}{r_{o1}} + \frac{g_{m3}}{g_{m2}} \left(\frac{1}{r_{o1}} + \frac{1}{r_{o2}} \right)} \right). \quad (14)$$

Based on Equation (14), it can be deduced that an increase in either g_{m1} or r_{o1} leads to a higher differential gain A_d . Therefore, enhancing the geometrical size of transistors M1 and M4, which concurrently augments both g_{m1} and r_{o1} , proves to be an effective approach for amplifying A_d .

Table 3 presents the geometrical size of MOSFETs employed in the op-amp. The width and length of some devices are presented as variables for further optimization process.

TABLE 3. Size of devices in op-amp.

Device	Size (W/L)
M_tail	$w_{nbias} / 1.5 \mu m$
M1, M4	w_{ndiff} / l_{ndiff}
M2, M5	$w_{pdiff} / 1.0 \mu m$
M3, M6	$5 \mu m / 1.5 \mu m$
M_PCAP	$15 \mu m / 15 \mu m$

C. STARTUP CIRCUIT

The proposed BGR topology exhibits two distinct operating points, both satisfying $V_X = V_Y$. The first operating point, determined in the preceding section and referred to as the “expected operating point”, features non-zero values for I_{REF} , V_{REF} , V_X , V_Y . The second operating point, known as the “degenerated operating point” is characterized by $I_{REF} = 0$, $V_X = V_Y = 0$, $V_{REF} = 0$. Therefore, a startup circuit is employed to transition the bandgap core from the degenerated operating point to the expected operating point.

TABLE 4. Size of devices in Startup and Self-bias circuit.

Device	Size (W/L)
M1F_PNOT	0.4 μm / 6 μm
M2F_PNOT	0.4 μm / 6 μm
M3F_PNOT	0.4 μm / 6 μm
M4F_NNOT	1 μm / 2 μm
M4G_N_START	0.2 μm / 0.06 μm
M1A_PBIAS	w_pbias / 0.4 μm
M2A_PBIAS	w_m2_pcasc / 1.5 μm
M3A_NBIAS	w_nbias / 1.5 μm
M1B_PBIAS	w_m1_pcasc / 1.5 μm
M3B_NBIAS	w_nbias / 1.5 μm

During the startup phase, when $V_{\text{REF}} = 0$, $V_{\text{outN}} \neq 0$, M4G_N_START turns on, V_{casc} experiences a voltage drop from VDDIO to a lower voltage level. This deliberate voltage reduction facilitates the transition of the BGR circuit from the degenerated operating point to the expected operating point. Once this transition is complete and $V_{\text{REF}} \neq 0$, M4G_N_START deactivates, rendering the startup circuit's impact negligible on the overall behavior of the BGR circuit.

D. SELF-BIAS CIRCUIT

The self-bias circuit block serves the purpose of generating a voltage for node V_{stage2} and bias current for the op-amp. In this circuit configuration, the gate-source voltage of M1B_PBIAS and M1C_PCASC are equal, resulting in an approximate equivalence between the drain current $I_{\text{D,M1B_PBIAS}}$ and the reference current I_{REF} . By employing transistors M3A_NBIAS and M3B_NBIAS as a current mirror, the current I_{REF} is replicated to transistor M2A_PBIAS. To ensure that the voltage V_{stage2} remains consistently lower than VDDIO, transistor M1A_PBIAS functions as a resistor, preventing a direct connection between the source terminal of M2A_PBIAS and VDDIO.

To achieve accurate amount of current flow in each branch of the self-bias circuit, it is imperative that all MOSFETs (excluding M1A_PBIAS) operate in the saturation region. This condition guarantees that the current values in each branch closely approximate the desired reference current I_{REF} .

Table 4 presents the geometrical size of MOSFETs employed in the startup circuit, together with the self-bias block. The width and length of some devices are given as variables for further optimization process.

E. PSRR CALCULATION FOR PROPOSED BGR

To calculate the PSRR value of the proposed BGR circuit, the small signal model, which is illustrated in Figure 4, is employed. By applying Kirchhoff's law, the influence of ripple at the supply voltage on the output voltage can be computed:

$$\frac{V_{\text{REF}}}{v_{\text{dd}}} = R_{\text{out}} \times \frac{g_1 r_1 (R_b + r_{1b}) + R_b R_{\text{ts}} g_{1b} g_A r_{1b}}{A_{\text{op}} (R_Y - R_X) r_{1b} (g_1 r_1 + R_b R_{\text{ts}} g_{1b} g_A)}.$$

Algorithm 1 Standard PSO Algorithm's Pseudo-Code

```

1 Initialize a swarm of  $N$  particles
2 for (!Stop_condition) do
3   fitness[i] = fitness_calculation()
4   Pbest[i] = (fitness[i] < Pbest_val[i]) * fitness[i] +
               (fitness[i] > Pbest_val[i]) * Pbest[i]
5   Gbest = min1 ≤ i ≤ N (Pbest[i])
6   position[i], velocity[i] = update()
7 return Gbest's position and fitness value

```

PSRR = 20

$$\log \left(\frac{v_{\text{dd}}}{v_{\text{REF}}} \right) = -20 \log \left(R_{\text{out}} \frac{g_1 r_1 (R_b + r_{1b}) + R_b R_{\text{ts}} g_{1b} g_A r_{1b}}{A_{\text{op}} (R_Y - R_X) r_{1b} (g_1 r_1 + R_b R_{\text{ts}} g_{1b} g_A)} \right). \quad (15)$$

According to (15), the PSRR value is influenced not only by the transistors within the cascode current source but also by the devices in the self-bias circuit and the gain of the op-amp. Hence, in this study, to achieve a high value of the PSRR parameter, two techniques are applied: first, enhancing the op-amp's gain by implementing the cascode topology, as discussed in Section II-B; and second, utilizing the optimization algorithm that considers the geometrical sizes of devices in the cascode current source, self-bias circuit, and op-amp circuit as design variables. The details of the optimization process are elaborated in Section III and Section IV.

III. OVERVIEW OF PSO ALGORITHM

A. STANDARD PSO ALGORITHM

PSO is one of the algorithms constructed to search for solutions to optimization problems in a given search space. It is a type of population-based algorithm, inspired by the group behavior of birds when searching for food: during the foraging process, each bird with predetermined inertia tends to adjust its trajectory toward the location with the highest amount of food it has previously discovered, while also aiming towards positions with the most abundant food that the others in group have found so far. The PSO algorithm has many vital applications in various fields that require solving optimization problems.

Algorithm 1 summarizes the standard PSO algorithm. In this algorithm, the first step is to randomly initialize a set of N different coordinates for the design variable vector. In PSO, this set is called **swarm**, and each coordinate is called a **particle**. Later, the fitness function's value of each particle is calculated from the position, and then, it is evaluated: the newly calculated fitness value is compared with the fitness value of *Pbest* (the best fitness value that a particle has found

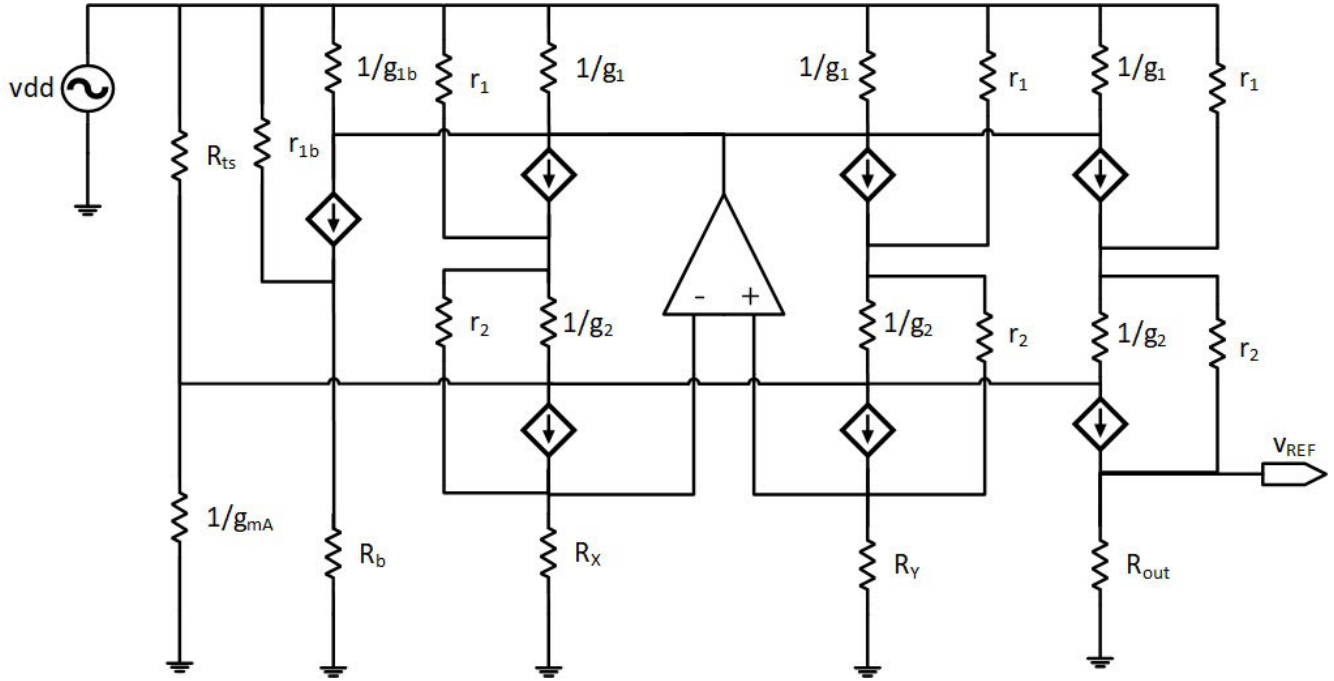


FIGURE 4. Small-signal model for proposed BGR circuit.

so far). Suppose that the current fitness value of the particle is smaller than the present value of Pbest's fitness function. In that case, the current fitness value and coordinate are recorded as the new Pbest's fitness value and coordinate. Following this, if there exists any particle in the swarm whose Pbest's fitness is smaller than that of the current Gbest (the best position found so far by the entire swarm), Gbest is replaced by this Pbest.

After the fitness function evaluation phase, the position and velocity of each particle (the amount of location change after an iteration) are updated according to Gbest and Pbest.

$$P_i^{t+1} = P_i^t + V_i^{t+1}. \quad (16)$$

$$V_i^{t+1} = \underbrace{\omega V_i^t}_{\text{inertia}} + \underbrace{c_1 r_1 (P_{\text{best}}^t - P_i^t)}_{\text{cognitive}} + \underbrace{c_2 r_2 (G_{\text{best}}^t - P_i^t)}_{\text{social}} \quad (17)$$

Equation (16) shows the mathematical expression used to calculate the position P_i^{t+1} of particle i at iteration $t+1$. The current position equals the sum of the previous position P_i^t and the velocity at the current iteration V_i^{t+1} . Equation (17) delineates the influential factors governing the modification of the particle's velocity: the property of keeping the velocity unchanged (inertia term), the previous particle's knowledge (cognitive term), and the influence from the social (social term). In (17), ω is the inertia weight, c_1 and c_2 are the acceleration coefficients, r_1 and r_2 stand for random numbers between 0 and 1. The values of ω , c_1 , and c_2 are chosen based on experience.

After updating the particles' position and velocity based on Equation (16) and (17), the stopping criteria are evaluated. If it is satisfied, the algorithm will stop. If not, the algorithm

returns to the fitness calculation phase, with the new position of each particle in the swarm.

PSO is a theoretically well-founded algorithm for this study due to its many advantages. First, it uses real-valued representations, avoiding the need for complex binary conversions common in other heuristic algorithms such as genetic algorithm. Second, its simple arithmetic operations make it easy to understand and implement. Third, its swarm behavior is particularly well-suited for large search spaces, enabling exploration at different scales and communication between particles that share information about their best solutions [29].

B. OVERVIEW OF PSO'S IMPROVEMENT METHODS

Despite numerous advantages, the PSO algorithm also has some drawbacks. One notable drawback is its vulnerability to early convergence, especially when dealing with complex optimization problems with multiple extremes. This phenomenon occurs due to two main inextricably intertwined factors: the inherent characteristics of the functions being optimized and the rapid loss of particle diversity, which can weaken the global search capability of the algorithm. To improve the performance of PSO algorithm, several innovative PSO variants have been proposed. These variants aim to enhance the capability of PSO to explore the search area and evade local optima, especially for specific problem instances. Generally, approaches to improving the traditional PSO algorithm can be categorized into two primary strategies: (1) hybridizing two existing algorithms,

TABLE 5. Constraints for BGR circuit design.

Metrics	Constraint	Unit
V_{REF}	$798 \leq V_{REF} \leq 802$	mV
TC	≤ 8	ppm/ $^{\circ}$ C
Loop gain @ DC	≥ 40	dB
Phase margin	≥ 60	degree
Gain margin	≥ 20	dB
Power	≤ 1000	μ W

and (2) introducing new strategy of tuning the parameters inside the algorithm.

In pursuit of the first strategy, the gravitational particle swarm optimization algorithm (GPSOA) [30], which hybridizes the PSO with the gravitational search algorithm (GSA), and the quantum-behaved PSO [31], which combines quantum mechanics with the standard PSO algorithm, were proposed. In GPSOA, particle behavior is influenced not only by kinematic parameters such as ω, c_1, c_2 , but also by gravitational interactions among them. In QPSO algorithm, each particle's position not only relies on previous position and current velocity, but also depends on the potential field of the particle. These two novel approaches have demonstrated better global search capability compared to the original PSO, particularly in addressing the multi-objective optimization problem of designing the wind-thermal power system [30] or choosing a suitable learning rate for deep belief network [32].

Although hybridization strategies offer several advantages, they come with certain drawbacks. One significant issue arises when combining two algorithms: the increase in the number of parameters that need to be tuned. As the parameter count rises, evaluating the contribution of each parameter to the hybrid algorithm's operation becomes challenging, making effective tuning difficult. Consequently, the second strategy, which involves introducing innovative methods to adjust the algorithm's metrics, is preferred. Various techniques can be applied in this strategy, such as modifying the particle's update formula, altering the particle's velocity, and adjusting the utilization of c_1 and c_2 values [21]. In this study, recognizing the pivotal role of the inertia weight parameter in PSO's global and local search abilities, we have focused on devising new methods for its incorporation after each iteration. These methods are elaborated in Subsection IV-C.

IV. CIRCUIT OPTIMIZATION PROCESS

A. PROBLEM FORMULATION

The objective of our design is to maximize the PSRR parameters. In order to guarantee the overall performance of our circuit, it is crucial that other relevant parameters meet the specified requirements, as outlined in Table 5.

The process of sizing all transistors to optimize one parameter, while ensuring the constraint satisfaction of others, is time-consuming and demands the expertise and experience of designers to achieve optimal results. By approaching this

process as an optimization problem and leveraging artificial intelligence techniques to address it, the process of finding an optimal solution becomes more efficient and less dependent on the designer's expertise. In this modeling framework, the objective function represents a crucial specification, while the remaining specifications are treated as constraints.

By modeling the PSRR parameter as the objective function, other specifications as constraint functions, and the geometrical size as design variables, the design problem can be formulated as an optimization problem in canonical form as presented in (18).

Maximize : PSRR(\mathbf{x})

subject to : $798 \text{ mV} \leq V_{REF} \leq 802 \text{ mV}$,

$TC \leq 8 \text{ ppm}/^{\circ}\text{C}$,

Loop gain @ DC $\geq 40 \text{ dB}$,

Phase margin $\geq 60^{\circ}$,

Gain margin $\geq 20 \text{ dB}$,

Power dissipation $\leq 1000 \mu\text{W}$. (18)

In (18), $\mathbf{x} = [w_pbias, w_ndiff, w_m1_pcasc, l_ndiff, w_pdiff, w_m2_pcasc, w_nbias]$ is the vector of design variables. The boundary of each variable is chosen based on experience.

The optimization problem (18) consists of both upper-bound constraint functions (function < number) and lower-bound constraint functions (function > number) with different boundaries. It is hard to evaluate the satisfaction of these constraints automatically. Therefore, for convenience purposes, we modify these constraint functions to a unique form shown in (19).

Maximize : PSRR(\mathbf{x})

subject to : $798 \text{ mV} - V_{REF} \leq 0$,

$V_{REF} - 802 \text{ mV} \leq 0$,

$TC - 8 \text{ ppm}/^{\circ}\text{C} \leq 0$,

$40 \text{ dB} - \text{Loop gain @ DC} \leq 0$,

$60^{\circ} - \text{Phase margin} \leq 0$,

$20 \text{ dB} - \text{Gain margin} \leq 0$,

$1000 \mu\text{W} - \text{Power dissipation} \leq 0$. (19)

B. PROPOSED PSO-BASED ALGORITHM FOR BGR CIRCUIT DESIGN

Figure 5 illustrates our approach to addressing the optimization problem outlined in (19). It consists of two key components: the circuit block and the optimization block. The circuit block, shown in brown in Figure 5, was designed using Cadence Virtuoso[®] software. Starting from a schematic drawing, Cadence Virtuoso[®] generates a netlist file, which is then imported into the Spectre[®] simulator to simulate the circuit's behavior. The optimization block is based on the standard PSO algorithm, with a novel inertia weight adjustment technique that will be explained in Section IV-C. In our proposed methodology, an Ocean language script

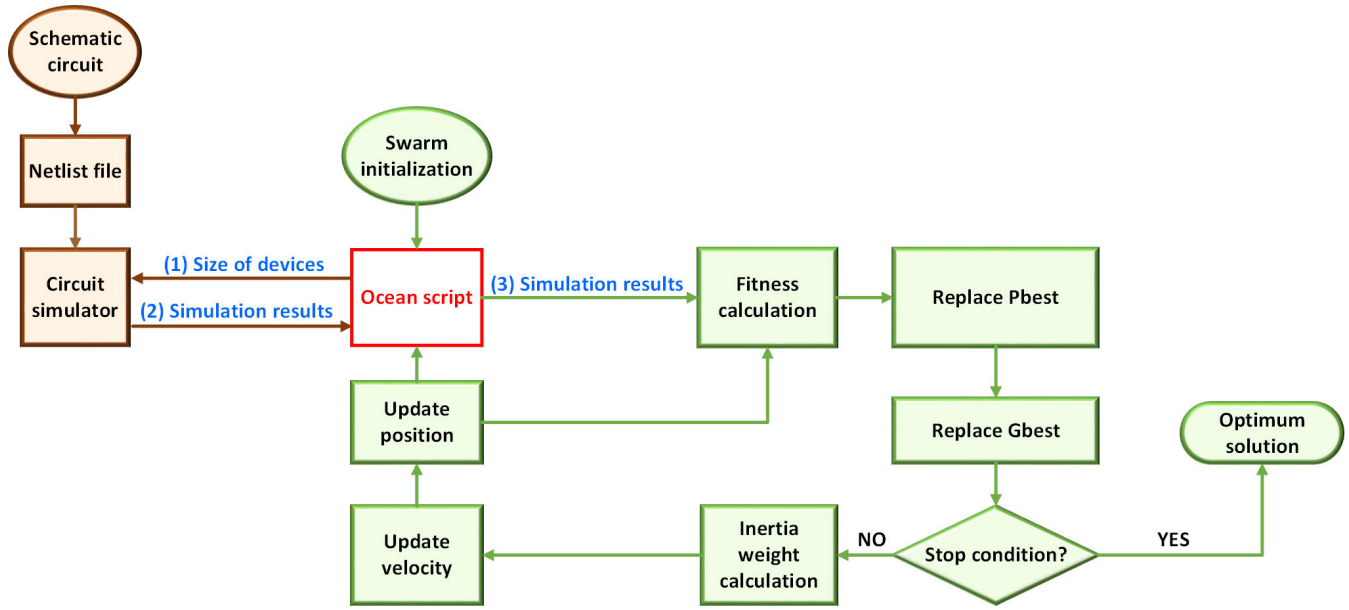


FIGURE 5. Proposed PSO-based optimization process for analog circuit design.

program serves as a bridge between the circuit block and the optimization block.

At the beginning of each iteration, the optimization block executes the Ocean script program. This program receives the position vector values of each particle as input, imports them to the simulator as design variable values, and triggers the simulation. The Ocean program then retrieves the simulation results from the simulator and transfers them back to the optimization block for computing the fitness function value.

The fitness function within the optimization block is defined by Equation (20):

$$\text{Fitness} = -\text{PSRR} + 1000 \times \text{penalty}. \quad (20)$$

This fitness function consists of two terms: the negative of the objective function and the penalty function. When the PSO algorithm minimizes the fitness function, the -PSRR is also minimized, which means that the PSRR parameter is maximized. The penalty function is included in the fitness function to serve as a mechanism to guarantee constraint adherence throughout the optimization process. At the start of each iteration, the penalty function is initialized with a value of 0. During the fitness evaluation phase, the penalty function value is calculated for each particle. Sequentially, it assesses each constraint function to determine compliance. If a constraint is not satisfied, the penalty function value increments by one, indicating a violation. This approach enables the algorithm to monitor any deviations from the defined constraints, promoting the generation of solutions that adhere to the specified constraints. The mechanism to calculate the value of the penalty function is summarized in Algorithm 2.

It is evident that if all the constraints are satisfied (the penalty function is minimized to 0) and the PSRR parameter

Algorithm 2 Penalty Function Calculation

Input : Value of constraint functions

Output: Penalty function value

/* N: No. of particles in swarm */
/* M: No. of performance metrics */

```

1 penalty = 0
2 for k in range (N) do
3   for j in range (M - 1) do
4     if constraint[k, j] ≥ 0 then
5       | penalty[k] = penalty[k] + 1
6     else
7       | penalty[k] = penalty[k]
8 return penalty

```

has the maximum value, the fitness function in Equation (20) is minimized. Therefore, it is suitable to propose (20) as the fitness function in our PSO optimization algorithm.

C. PROPOSED INERTIA WEIGHT ADJUSTMENT TECHNIQUES

This article presents three distinct approaches to decrease the inertia weight parameter from its maximum value ω_{\max} to its minimum value ω_{\min} . One of these methods is already established, while the other two are newly proposed by us.

Reference [22] presents a method for gradually reducing the inertia weight parameter from ω_{\max} to ω_{\min} , as illustrated in Equation (21). In this paper, we refer to this method as the PSO-linear decreasing (PSO-LD) method.

$$\omega = \omega_{\max} - \omega_{\min} \times \frac{t}{T}. \quad (21)$$

In [33], the concept of exponential adaptive crossover rate (CR) is introduced to improve the convergence of the differential evolution algorithm. The adaptive crossover rate is mathematically defined in (22):

$$CR = CR_0 \times \exp\left(-a \left(\frac{g}{G}\right)^b\right), \quad (22)$$

where CR_0 is the initial crossover rate, g is the current generation number, and G is the maximum generation number.

Through the application of Equation (22), the CR parameter assumes a heightened value during the initial runs, serving the purpose of preserving the possibility of convergence towards sub-optimal solutions. Subsequently, as the algorithm progresses into later runs, this parameter takes on a diminished value, thereby fostering a more focused approach to local search procedures.

The aforementioned concept applied to the CR parameter of the differential evolution algorithm can be harnessed to formulate a dynamic inertia weight parameter for the PSO algorithm. Equation (23) introduces an equation in which the value of ω undergoes an exponential reduction. During the initial iterations, ω experiences a substantial decrease from ω_{\max} to ω_{\min} , indicating a propensity for local search by the algorithm. Hence, we refer to this formula as the PSO - local exploitation orienter (PSO-LEO).

$$\omega = \omega_{\min} + (\omega_{\max} - \omega_{\min}) \times \exp\left(-\alpha \frac{t}{T}\right). \quad (23)$$

In Equation (24), during the initial iterations, ω is approximately equal to ω_{\max} , then undergoes a substantial reduction to ω_{\min} in subsequent iterations. This transition prompts the algorithm to emphasize global search during its initial iterations, thus enhancing its capacity to discover the global optimum. Hence, we name Equation (24) as the PSO - global exploration orienter (PSO- GEO).

$$\omega = \omega_{\max} \times \exp\left(-\left(\frac{t - T \left(1 - \beta \ln \frac{\omega_{\max}}{\omega_{\min}}\right)}{T}\right)^\beta\right). \quad (24)$$

V. RESULT AND DISCUSSION

A. SCENARIO

The PSO-based optimization block of our proposed algorithm, as described in Subsection IV-B, is implemented using Python 3.7.0. Within this Python program, the swarm size is set to 6, the acceleration coefficients are defined as $c_1 = 0.3$, $c_2 = 0.9$. The maximum and minimum inertia weights are set to $\omega_{\max} = 0.9$ and $\omega_{\min} = 0.4$, respectively. Four distinct methods of inertia weight utilization are employed in this work: keeping $\omega = \text{const}$ (conventional method), PSO-LD, PSO-LEO and PSO-GEO. These four methods are demonstrated in Figure 6. The α parameter in the PSO-LEO approach and the β parameter in the PSO-GEO approach are both set to a value of 8, serving as an illustrative example.

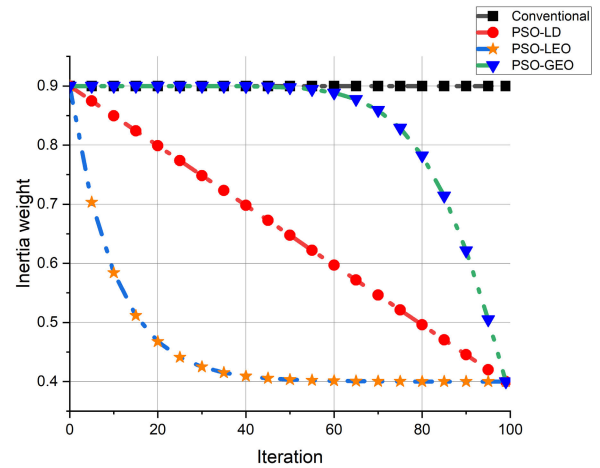


FIGURE 6. Four methods of employing inertia weight.

TABLE 6. Optimization result for 10 executions.

Execution	Conventional	PSO-LD	PSO-LEO	PSO-GEO
1	-99.8006	-98.3181	903.139	-99.009
2	903.6636	905.8816	900.5143	-99.9896
3	904.2904	-98.8251	906.8875	899.6047
4	905.5045	906.551	906.2682	904.9483
5	902.9503	-98.4502	901.1489	-99.9868
6	900.6525	-99.7719	902.2747	-99.9098
7	904.2006	901.0167	900.7134	900.7729
8	-98.7331	900.0905	906.1516	-97.5106
9	906.2794	904.5398	904.9945	-99.8476
10	-99.6770	906.3641	904.0085	-99.1143
Success rate	3/10	4/10	0/10	7/10
Minimum fitness value	-99.8006	-99.7719	900.5143	-99.9896
Mean value (success cases only)	-99.4036	-98.8413	N.A	-99.3382
Std.dev (success cases only)	0.5839	0.6565	N.A	0.9064

To ensure a fair comparison we used the same initial swarm positions for all four methods. To establish statistical significance, we ran each method 10 times, with 100 iterations each.

B. RESULT

Table 6 displays the final fitness value obtained from conducting 10 executions for each inertia weight reduction technique. Within this table, four techniques of employing inertia weight are compared in four criteria: success rate, optimal fitness value, mean fitness values (only for successful cases), and the standard deviation of successful fitness values.

In the case of the PSO-LEO approach, ω experiences a rapid decline, reaching ω_{\min} during the initial iterations. Consequently, the algorithm prioritizes the local search right from the beginning of each execution. As a result, it succeeds in identifying the local optimum of the fitness function but

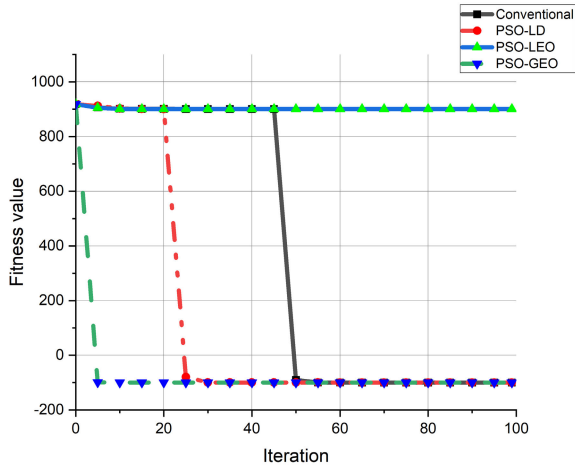


FIGURE 7. Evolution of the best run of four PSO approaches.

cannot discover the global optimum point in all ten executions. When comparing three methods capable of attaining the global optimum, namely the conventional method, PSO-LD method, and PSO-GEO method, it is evident that the latter method exhibits superior performance relative to the other two. It boasts the highest success rate, achieves the optimal fitness value, as well as exhibits the fastest convergence rate. As illustrated in Figure 7, the PSO-GEO method successfully locates the global optimum point and converges after just 5 iterations, while the PSO-LD method and the conventional method require 23 and 45 iterations, respectively, to reach convergence.

Table 7 displays the results for PSRR and constraint functions obtained through the best-performing executions of different approaches. Specifically, in the case of the PSO-LEO approach, the PSRR parameter achieves its highest value at 99.4857. However, it's worth noting that the TC parameter exceeds its defined constraint. According to Equation (20), when a constraint is violated, the fitness function value increases by 1000 units relative to the negative PSRR value. Consequently, the combination of the maximum PSRR value and the TC constraint violation results in a fitness value of 900.514, representing the local optimum found by the PSO-LEO approach, as shown in Table 6. To gain a deeper understanding of the trade-off between PSRR and TC, we illustrate the values of these parameters in relation to two important design variables in Figure 8.

Following Equation (20), the PSRR value of our BGR circuit relies on two key variables: R_{ts} , which depends on the resistance of M1A_PBIAS, and g_{m1} , indicative of the transconductance of M1C_PCASC (or M1D_PCASC, M1E_PCASC). Figure 8 visually demonstrates the dependencies of PSRR and TC on the geometric widths of M1A_PBIAS and M1C_PCASC transistors, denoted as w_{pbias} and w_{m1_pcasc} , respectively. Within the demonstrated space, two distinct regions stand out as having the highest PSRR values (depicted in red):

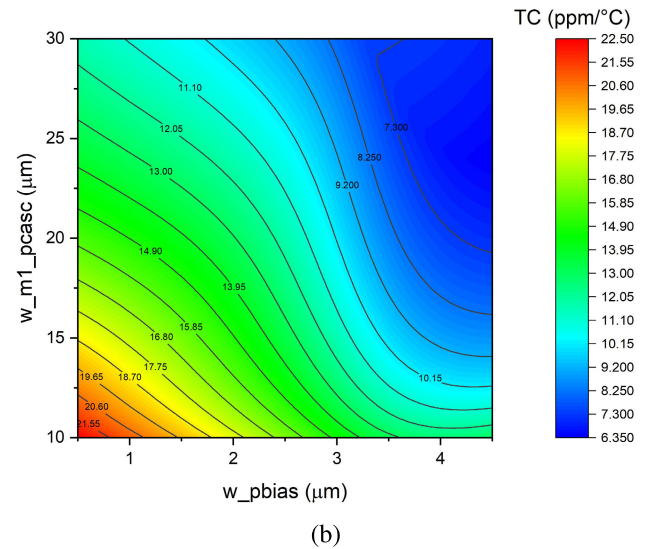
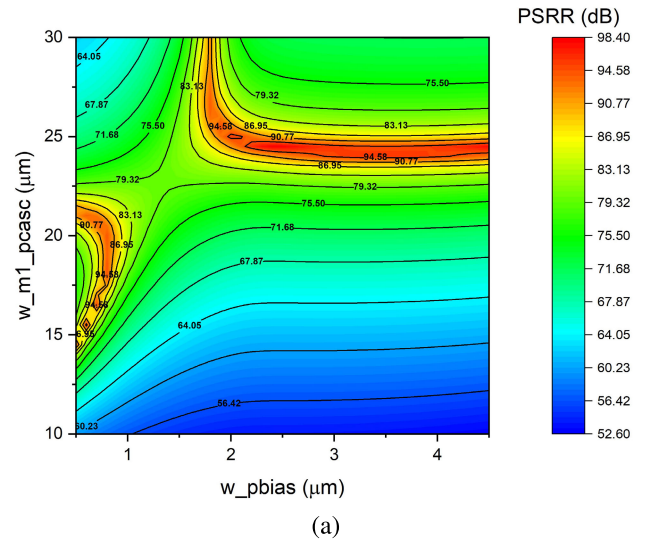


FIGURE 8. Contour plot versus key design variables for (a) PSRR parameter, (b) TC parameter.

- Region 1: bounded by the boundaries of $0.5 < w_{pbias} < 1.0$ and $14.5 < w_{m1_pcasc} < 22.7$. Within this constrained space, PSRR values are notably high, accompanied by elevated TC values ranging from approximately 14 to 18 ppm/°C.

- Region 2, where $2 < w_{pbias} < 4.5$ and $24 < w_{m1_pcasc} < 24.5$. In this confined area, PSRR values are notably high, with TC values falling below 8 when w_{pbias} exceeds 3.5 (the area of low TC is depicted in blue color).

In our experimental scenario, a design was implemented to ensure that, for all four inertia weight utilization methods, the G_{best} after the first iteration is set to $[w_{pbias}, w_{m1_pcasc}] = [1.0239, 19.517]$, which is in proximity to Region 1. In the context of the PSO-LEO approach, the inertia weight parameter is intentionally dropped to a low value during the initial iterations. This deliberate choice constrains the particle movements within the confines of Region 1,

TABLE 7. Best optimization result from four approaches.

Parameter	Constraint	Conventional	PSO-LD	PSO-LEO	PSO-GEO	Unit
PSRR		99.8006	99.7719	99.4857	99.9896	dB
V_{REF}	$798 \leq V_{REF} \leq 802$	800.8970	800.8720	800.9080	800.8760	mV
TC	≤ 8	7.0870	7.0057	11.4905	6.3938	ppm/°C
Loop gain @ DC	≥ 40	52.8190	52.5127	50.9776	52.7093	dB
Phase margin	≥ 60	78.0707	78.4994	79.5781	78.0045	degree
Gain margin	≥ 20	21.3404	21.5699	22.5117	21.2709	dB
Power	≤ 1000	301.5651	300.9598	300.8587	301.7596	μ W

TABLE 8. Value of design variables at the best design point.

Variable	Value provided by optimization algorithm (μ m)	Feature size value (μ m)
w_pbias	4.5	4.5
w_nbias	15	15
w_m1_pcasc	24.3543	24.355
w_m2_pcasc	15	15
w_ndiff	20	20
w_pdiff	4.5307	4.530
l_ndiff	3	3

preventing them from exploring more distant extremal points. Consequently, the particles become confined within an extremal point located in Region 1. In this location, the PSRR value is maximized, although at the cost of violating the TC's specification. Conversely, for the other approaches considered, the ω parameter exhibits a higher value during the initial phases, allowing the particles to venture beyond Region 1 and explore the attributes of Region 2.

Compared with PSO-LD, the higher success rate of PSO-GEO can be attributed to the utilization of a larger inertia weight value throughout the optimization process. Consequently, the particle velocities in the PSO-GEO method are greater than those in the PSO-LD method. This higher velocity allows the particles in PSO-GEO to reach Region 2 before the iteration ends, which contributes to their greater success rate compared to the particles in PSO-LD.

When PSO-GEO is compared with the conventional method, the higher success rate of PSO-GEO can be explained by the fact that in later iterations the inertia weight value in the conventional method is larger than that in PSO-GEO. A larger inertia weight value results in larger inertial velocities, potentially causing particles in the conventional method to bypass the optimal region within the Region 2.

These observations underscore the significance of the inertia weight parameter in influencing particle behavior and, subsequently, explain the high success rate of the PSO-GEO method compared to that of PSO-LEO, as well as the pre-existing conventional method and PSO-LD method.

Table 8 presents the values of the design variables obtained by the PSO-GEO approach, with which the best performance, as indicated in Table 7, is achieved. In addition,

TABLE 9. BGR circuit's simulation results after employing feature size values.

Parameter	Value	Unit
PSRR @ DC	159.9688	dB
PSRR @ 1 kHz	99.9896	dB
V_{REF}	800.8760	mV
TC	6.4056	ppm/°C
Loop gain @ DC	52.7094	dB
Phase margin	78.0044	degree
Gain margin	21.2708	dB
Power	301.7596	μ W

TABLE 10. Comparison with other works, in terms of circuit performance.

	This work ^S 2023	[34] ^L 2021	[35] ^M 2018	[36] ^S 2014	[9] ^M 2011
CMOS process (nm)	65	65	65	65	180
Output voltage (V)	0.8	0.6	1.2	0.44	0.698
Temperature range (°C)	-40 to 125	-40 to 100	-20 to 150	-45 to 120	-40 to 140
TC (ppm/°C)	6.4056	5	9.8	10.65	20
Power (μ W)	301.7596	5.2	N.A	104	134
PSRR (dB)	159.9688@DC 99.9896@1kHz	91 @ DC	70 @ DC	20.21 @ DC	95 @ DC

^S: schematic simulation, ^L: post-layout simulation, ^M: measurement

the corresponding feature size values, rounded to 5 nm, are presented.

Table 9 shows the performance of the BGR circuit after employing the feature size values presented in Table 8.

Table 10 compares the performance of the BGR circuit designed in this research with other works. By utilizing a proposed cascode load within the op-amp and implementing an optimization algorithm, our work has achieved a superior PSRR value compared to earlier works. However, it is essential to note that in our circuit, the current flowing across transistors is large (about 30 μ A), leading to a high value of power dissipation. Furthermore, in terms of TC, our work does not perform as well as the studies [34] and [35], because in these works, a high-order piecewise curvature technique

has been applied to improve TC, while in our design, the first order temperature compensated structure is used.

VI. CONCLUSION

This study centers on three aspects. Firstly, we optimized the topology selection for the BGR circuit by introducing a cascode current source block to enhance bias accuracy, and a cascode load was incorporated for the op-amp to improve both its differential gain and the overall BGR circuit's PSRR parameter. Secondly, the PSO algorithm was employed to address the optimization problem, with the objective of maximizing PSRR while ensuring the satisfaction of other specifications. Thirdly, we introduced four strategies for adapting the inertia weight parameter in the PSO algorithm: the conventional approach, which maintains ω unchanged, the existing PSO-LD methods, and our two novel methods: PSO-LEO, which features a rapid decrease the value of ω to ω_{\min} in early iterations, and PSO-GEO, characterized by a high ω value during early iterations followed by a significant drop.

The results indicated that the PSO-GEO approach yields the most favorable outcomes, primarily owing to its capacity to effectively guide particles toward the intricate global optimum region. Furthermore, a comprehensive comparison in terms of circuit performance was also conducted, revealing that our circuit, optimized by the PSO algorithm, achieved a PSRR value of 99.9896 at 1 kHz, surpassing the values reported in other published work. These comparative outcomes underscore the potential utility of both the PSO algorithm and the PSO-GEO technique in forthcoming engineering applications, extending beyond BGR circuit design. However, further research on the effectiveness of both PSO and PSO-GEO is warranted. As the No Free Lunch (NFL) Theorem states, no single metaheuristic algorithm can universally address all optimization problems [37]. Therefore, continued exploration of PSO and PSO-GEO's capabilities in various optimization scenarios is crucial.

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communications, wireless security, signal processing, optimization for IC design and wireless networks, AI, and quantum computing.

TRANG HOANG received the Ph.D. degree in microelectronics from CEA-LETI and University Joseph Fourier, France, in 2009. He is currently an Associate Professor of electronics engineering with the Ho Chi Minh City University of Technology (HCMUT), Vietnam National University, Ho Chi Minh City (VNU HCM), Vietnam, and the Dean of the Graduate School, HCMUT-VNU HCM. His research interests include ASIC/FPGA implementation, IC architecture, MEMs, wireless



communications, wireless security, signal processing, optimization for IC design and wireless networks, AI, and quantum computing.

THANG NGUYEN QUOC was born in Ba Ria-Vung Tau, Vietnam. He received the Bachelor of Engineering degree in electronics engineering from the Ho Chi Minh City University of Technology (HCMUT), Vietnam National University Ho Chi Minh City (VNU-HCM), in November 2023. He will be pursuing the degree with the Department of Electrical and Computer Engineering, Faculty of Engineering and Applied Science, Memorial University of Newfoundland, St. John's,



received the Ph.D. degree in electrical engineering from the Otto-von-Guericke University of Magdeburg, Magdeburg, Germany, in 2003. He was a Postdoctoral Research Associate with Concordia University, Montreal, QC, Canada; Dalhousie University, Halifax, NS, Canada; and the University of Washington, Seattle, WA, USA. He is currently a Full Professor with the Department of Electrical and Computer Engineering, Faculty of Engineering and Applied Science, Memorial University of Newfoundland, St. John's, NL, Canada. His current research interests include very large-scale integration computer-aided design, mixed-signal integrated system/circuit design, microelectromechanical systems design and design automation, wireless sensor networks, microfluidics and biosensors, and microprocessor-based instrumentation for ocean and biomedical applications.



Engineering, Faculty of Engineering and Applied Science, Memorial University of Newfoundland, St. John's, NL, Canada. His current research interests include very large-scale integration computer-aided design, mixed-signal integrated system/circuit design, microelectromechanical systems design and design automation, wireless sensor networks, microfluidics and biosensors, and microprocessor-based instrumentation for ocean and biomedical applications.

TRUNG Q. DUONG (Fellow, IEEE) is a Canada Excellence Research Chair (CERC) and a Full Professor at the Memorial University of Newfoundland, Canada. He is also the Adjunct Chair Professor in telecommunications at Queen's University Belfast, U.K. He was a Distinguished Advisory Professor at Inje University, South Korea (2017-2019). He is an Adjunct Professor and the Director of Institute for AI and Big Data at Duy Tan University, Vietnam (2012-present), a Distinguished Professor at Thuyloi University, Vietnam (2023-2028) and a Visiting Professor (under Eminent Scholar program) at Kyung Hee University, South Korea (2023-2024). His current research interests include quantum communications, wireless communications, signal processing, machine learning, and real-time optimization.

He is a fellow of the Asia-Pacific Artificial Intelligence Association (AAIA). He received the Best Paper Award from the IEEE VTC-Spring 2013, IEEE ICC 2014, IEEE GLOBECOM 2016, 2019, and 2022, IEEE DSP 2017, IWCMC 2019 and 2023, and IEEE CAMAD 2023. He was a recipient of the prestigious Newton Prize 2017. He has received two prestigious awards, including the Research Chair of the Royal Academy of Engineering (2021–2025) and the Royal Academy of Engineering Research Fellowship (2015–2020). He has served as an Editor/Guest Editor for IEEE Transactions on Wireless Communications, IEEE Transactions on Communications, IEEE Transactions on Vehicular Technology, IEEE Communications Letters, IEEE Wireless Communications Letters, IEEE Wireless Communications, *IEEE Communications Magazine*, and IEEE Journal on Selected Areas in Communications.

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