Advances in Reversed Nested Miller Compensation

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***Abstract*—The use of two frequency compensation schemes for three-stage operational transconductance amplifiers, namely the reversed nested Miller compensation with nulling resistor (RNMCNR) and reversed active feedback frequency compensation (RAFFC), is presented in this paper. The techniques are based on the basic RNMC and show an inherent advantage over traditional compensation strategies, especially for heavy capacitive loads. Moreover, they are implemented without entailing extra transistors, thus saving circuit complexity and power consumption. A well-defined design procedure, introducing phase margin as main design parameter, is also developed for each solution. To verify the effectiveness of the techniques, two amplifiers have been fabricated in a standard 0.5-μm CMOS process. Experimental measurements are found in good agreement with theoretical analysis and show an improvement in small-signal and large-signal amplifier performances. Finally, an analytical comparison with the nonreversed counterparts topologies, which shows the superiority of the proposed solutions, is also included.**

***Index Terms*—Analog integrated circuits, CMOS, feedback amplifier, frequency compensation, multistage amplifier.**

I. Introduction

THE operational transconductance amplifier (OTA) is a basic building block in most analog and mixed-signal electronic systems. An increasing number of applications require high-gain high-bandwidth amplifiers able to drive capacitive loads under low-voltage supply conditions. As the supply voltage continues to scale down, traditional cascode topologies are no longer suitable for achieving high dc gains, since they cause a reduction of the voltage swings. To avoid cascoding, dc gains in excess of 100 dB are achieved by cascading three transconductance gain stages. However, this approach causes bandwidth reduction, since each stage inevitably introduces low-frequency poles which require additional compensation capacitors to provide adequate closed-loop stability.

For this purpose, compensation of three-stage amplifiers, where the second stage is noninverting and the last is inverting, is obtained through the nested Miller compensation (NMC) technique [1]–[5]. This approach employs two compensation capacitors and exploits the Miller effect to split the low frequency poles and achieve the desired phase margin and transient response. However, this solution results in bandwidth and slew rate reduction (the gain-bandwidth product is one-quarter as that achievable by a single-stage amplifier, [6]) and in a high power consumption. Recently, different compensation topologies have been proposed in order to overcome the inherent limits of NMC [6]–[13], especially for heavy capacitive loads [14]–[16], [23]. Indeed, many applications require high-gain OTAs driving loads in the order of hundreds of picofarads in battery-powered equipments, such as high-accuracy $\Sigma\Delta$ modulators, flash and pipeline analog-to-digital converters, linear regulators, and active matrix display drivers.

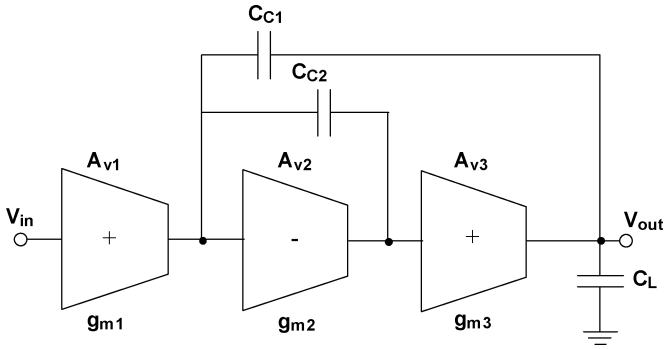

Fig. 1. Block diagram of the basic RNMC.

When the inner OTA stage is the only inverting one, another kind of compensation scheme, termed the reversed NMC (RNMC) is the most suitable option [4], [5], [17]–[20]. This technique exploits the same operating principle of the NMC but provides an inherent bandwidth improvement since, as shown in Fig. 1, the inner compensation capacitor does not load the output node [4], [19].

In this paper, we shall discuss two simple and high-performance compensation strategies, namely the RNMC feedforward with nulling resistor (RNMCFNR) and reversed active feedback frequency compensation (RAFFC). It is shown that the techniques significantly improve small-signal and large-signal performance, while maintaining low the circuit complexity, since they can be implemented using only passive components.

The paper is organized as follows. The analysis and design equations of the two techniques are presented in Section II. Circuits implementation along with some simulation results are discussed in Section III. Experimental measurements, and some considerations regarding the peculiar features of the proposed approaches, including an analytical comparison between the proposed compensation topologies and the nonreversed counterparts, are reported in Section IV. The authors' conclusion and additional remarks are given in Section V. Appendix A, providing useful and general results related to three-stage amplifiers, is also included.

II. Compensation Techniques

The block diagrams of a three-stage amplifier exploiting the two proposed techniques are illustrated in Figs. 2 and 3. In particular, Fig. 2 shows the topology named *RNMCFNR*, where the compensation is achieved by means of the Miller capacitors C_{C1}

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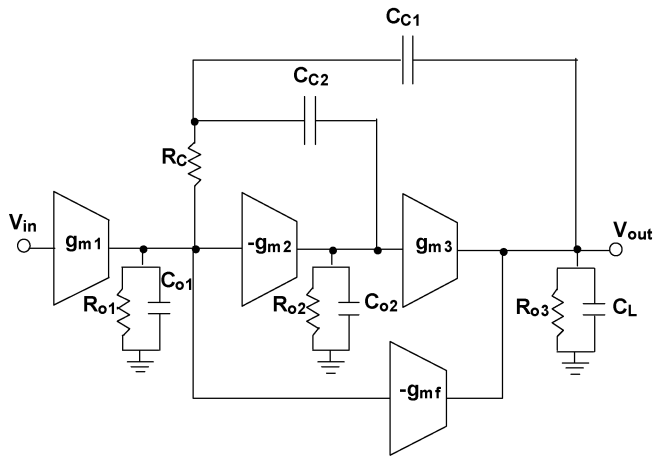

Fig. 2. Block diagram of the RNMCFNR technique.

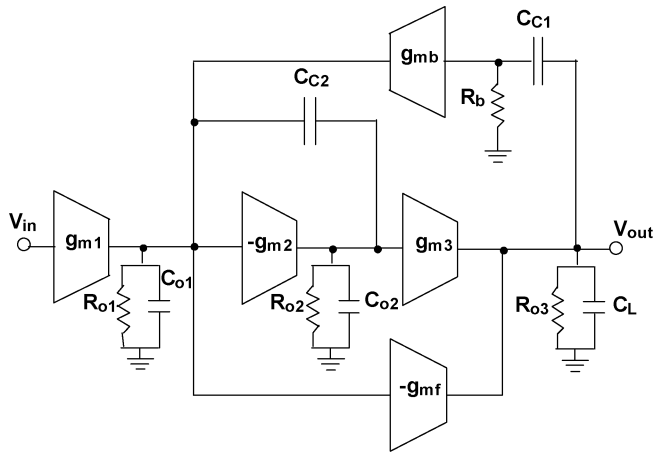

Fig. 3. Block diagram of the RAFFC technique.

and C_{C2}, the resistor R_C and the inverting feedforward stage g_{mf}. Likewise, fig. 3 shows the topology named *RAFFC*, which makes use of a current buffer in the outer compensation loop.

For both topologies, the design of the compensation network starts from the analysis of the open-loop transfer function, which can be obtained by analyzing the equivalent small-signal circuits shown in the same Figs. 2 and 3, in which parameters g_{mi}, r_{oi} and C_{oi} represent the ith stage transconductance, resistance and equivalent output capacitance, respectively, whereas C_L is the load capacitance. In order to simplify the expressions, while maintaining accuracy, in the following the transfer function will be carried out assuming that the dc gain of each stage $A_{Vi} = g_{mi}r_{oi}$ is much greater than unity and that C_L, C_{C1}, $C_{C2} \gg C_{oi}$. Consequently, we will neglect the high-frequency poles due to parasitics.

A. RNMCFNR

The RNMCFNR structure (Fig. 2) of the sole compensation branch is in principle the same as proposed in [10], but the open-loop transfer function is almost dissimilar due to the different amplifier topology.

Using the assumption stated above, small-signal symbolic analysis yields (1), shown at the bottom of this page, where ω_{P1} is the dominant pole

$$\omega_{P1} \cong \frac{1}{C_{C1}r_{o1}g_{m2}r_{o2}g_{m3}r_{o3}} \tag{2}$$

and A_0 is the dc voltage gain

$$A_0 = -g_{m1}r_{o1}g_{m2}r_{o2}g_{m3}r_{o3}. \tag{3}$$

Therefore, the gain-bandwidth product is, as usual

$$\omega_{\mathrm{GBW}} = |A_0|\omega_{P1} = \frac{g_{m1}}{C_{C1}}. \tag{4}$$

The transfer function exhibits two nondominant poles (usually complex and conjugates) and two zeros that can be both allocated in the left-half plane through a suitable choice of R_C and g_{mf}. Specifically, our approach exploits R_C to cancel out the coefficient of s^2 in the numerator of (1), so that only one negative zero is left.

This condition holds by setting

$$R_C = \frac{1}{g_{m2} + g_{mf}}. \tag{5}$$

Note that (5) requires matching between a resistance and two transconductances, thus process variations may lead to incomplete elimination of the zero. However, this is not crucial for stability since the zero is still positioned at high frequencies if the s^2 coefficient is maintained relatively small. Nevertheless, appropriate biasing schemes can be used to ensure reliable matching.

Among the possible alternatives, we choose to set

$$g_{mf} = g_{m3} \tag{6}$$

in order to obtain a symmetrical push-pull output stage improving slew rate and settling performance (as we will clarify considering the transistor level scheme of Fig. 4). Substituting (5) and (6) into (1) yields

$$A_{\mathrm{vRNMCFNR}}(s) = A_0 \frac{1 + s\frac{C_{C1}+C_{C2}}{g_{m2}+g_{m3}}}{\left(1+\frac{s}{\omega_{P1}}\right)\left[1 + s\frac{C_{C1}+C_L}{g_{m3}C_{C1}}C_{C2} + s^2\frac{C_{C2}C_L}{g_{m2}g_{m3}}\right]}. \tag{7}$$

$$A_{\mathrm{vRNMCFNR}}(s) = A_0 \frac{1 + s\left[(C_{C1}+C_{C2})R_C + \left(\frac{g_{mf}}{g_{m2}g_{m3}} - \frac{1}{g_{m2}}\right)C_{C2}\right] + s^2\frac{(g_{mf}+g_{m2})R_C - 1}{g_{m2}g_{m3}}C_{C1}C_{C2}}{\left(1+\frac{s}{\omega_{P1}}\right)\left[1 + s\frac{(g_{m2}+g_{mf}-g_{m3})C_{C1}+g_{m2}C_L}{g_{m2}g_{m3}C_{C1}}C_{C2} + s^2\frac{C_{C2}C_L}{g_{m2}g_{m3}}\right]} \tag{1}$$

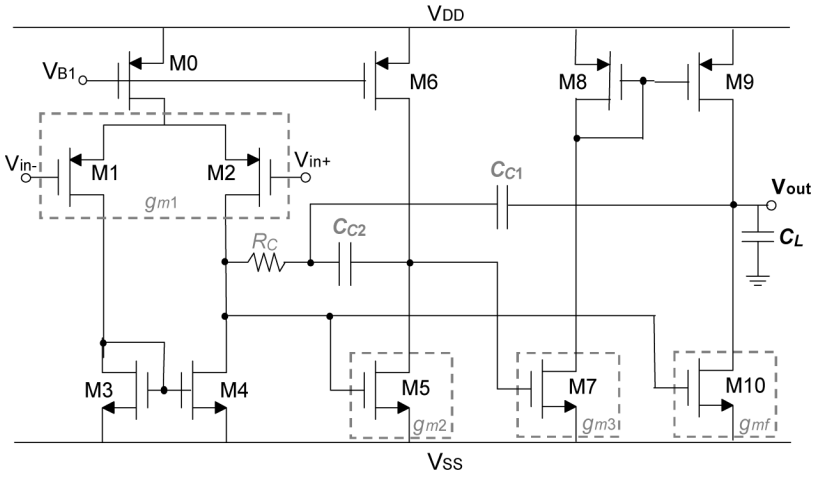

Fig. 4. Schematic of the three-stage amplifier compensated using the RNMCFNR technique.

The design usually starts from the determination of the transconductance of the first stage g_{m1}, which is determined to satisfy noise requirement or the standard deviation of the random offset due to mismatches. Then, the value of C_{C1} is obtained using (4) after setting the desired gain-bandwidth product. The value of C_{C2} is set so as to avoid peaking in the frequency response. At this purpose, comparing (A1) in the Appendix with (7) and applying (A5), after simple algebra we get

$$C_{C2} = \frac{2g_{m3}C_{C1}^2C_L}{g_{m2}(C_{C1}+C_L)^2} \approx \frac{2g_{m3}C_{C1}^2}{g_{m2}C_L} = \frac{2g_{m3}g_{m1}^2}{g_{m2}C_L\omega_{\mathrm{GBW}}^2} \tag{8}$$

where the rightmost approximation holds if $C_L \gg C_{C1}$. It is worth noting that unlike the similar compensation technique NMCFNR [6], [10], where C_{C2} is proportional to C_L, now C_{C2} assumes small values in presence of heavy capacitive loads, thus allowing a considerable saving of silicon area.

Besides, unlike the conventional NMC topologies (where the higher g_{m3} the better is the amplifier performance), the value of the transconductance of the last stage is set only to obtain feasible values of C_{C2} according to (8). For the sake of simplicity, among the possible options, we set

$$g_{m3} = g_{m2}. \tag{9}$$

By applying (A4) in the Appendix, using (4) and (8) and assuming $C_L \gg C_{C1}$, phase margin evaluation yields

$$\Phi = \tan^{-1}\left\{\frac{2\frac{g_{m2}}{g_{m1}}\left[\left(\frac{g_{m2}}{g_{m1}}\right)^2-1\right]}{3\left(\frac{g_{m2}}{g_{m1}}\right)^2+2}\right\}. \tag{10}$$

Since the phase margin is a design specification, we have to solve (10) to evaluate the required value of the ratio g_{m2}/g_{m1}. Although the exact solution can be found, it is too complex for hand calculation, nonetheless it can be approximated with an error lower than 8% for Φ ranging from 45° to 85° by

$$\frac{g_{m2}}{g_{m1}} \cong 1.5\tan\Phi + 0.5. \tag{11}$$

The last design constraint regards asymptotic stability and is obtained by applying (A7) in the Appendix

$$\omega_{\mathrm{GBW}} < \frac{C_{C1}+C_L}{C_L}\frac{g_{m2}}{C_{C1}} \approx \frac{g_{m2}}{C_{C1}}. \tag{12}$$

Remembering (4), this condition simply states that the transconductance of the second stage must be higher than that of the first stage to ensure asymptotic stability. Finally, it should be noted that, unlike in the NMC, g_{m3} could in principle assume any value and, even if it is not convenient, it could be set smaller than g_{m1}.

B. RAFFC

The RAFFC structure (Fig. 3) was first introduced by the authors in [20] and exploits the same principle of operation proposed in [12], [13]. In this Section the technique will be revised and design equations rearranged, showing an inherent improvement as compared to the solutions proposed in [12], [13]. The small-signal open-loop transfer function is expressed by (13) at the bottom of the page, where ω_{P1}, A_0 and the gain-bandwidth product are again expressed by (2), (3), and (4). It is apparent that choosing g_{mf} equal to g_{m3}, the s^2 term in the numerator of (13) is set equal to zero and, as explained in Section II-A, the large-signal performance is enhanced as well.

Therefore, using (6) and assuming $g_{mb} \cong 1/R_b$, (14) is rewritten as

$$A_{\mathrm{v}}(s) = A_0\frac{1+s\frac{C_{C1}}{g_{mb}}}{\left(1+\frac{s}{\omega_{P1}}\right)\left[1+s\frac{C_{C1}+C_L}{g_{m3}C_{C1}}C_{C2}+s^2\frac{C_{C2}C_L}{g_{mb}g_{m3}}\right]}. \tag{14}$$

$$A_{\mathrm{v}}(s) = A_0\frac{1+s\left[C_{C1}R_b+\left(\frac{g_{mf}}{g_{m2}g_{m3}}-\frac{1}{g_{m2}}\right)C_{C2}\right]+s^2\frac{g_{mf}-g_{m3}}{g_{m2}g_{m3}}R_bC_{C1}C_{C2}}{\left(1+\frac{s}{\omega_{P1}}\right)\left[1+s\frac{(g_{m2}+g_{mf}-g_{m3})C_{C1}+g_{m2}C_L}{g_{m2}g_{m3}C_{C1}}C_{C2}+s^2\frac{C_{C2}C_L}{g_{mb}g_{m3}}\right]} \tag{13}$$

It is worth noting that the zero cancellation is now inherently more reliable, since it does not require matching between resistance and transconductances.

Indeed, matching of g_{mf} and g_{m3} necessitates a lower design effort and can be accomplished in the RNMC topology in a simple and efficient way, as will be clarified in the next Section.

Note that the transfer functions of the two solutions are very similar. In particular, the second-order polynomial at the denominator of (1) is the same as in (13), provided that $g_{m2} = g_{mb}$. Moreover, both the transfer functions have one LHP zero. Therefore, the design equations are derived by following the same design procedure of Section II-A and are reported subsequently

$$C_{C2} = \frac{2g_{m3}C_{C1}^2C_L}{g_{mb}(C_{C1}+C_L)^2} \approx \frac{2g_{m3}C_{C1}^2}{g_{mb}C_L} = \frac{2g_{m3}g_{m1}^2}{g_{mb}C_L\omega_{\mathrm{GBW}}^2}. \tag{15}$$

It is worth noting that parameter $\mathrm{g_{m2}}$ can now be almost freely set, since it does not appear in any design constraint. However, in a first design step we can again apply (9). Applying (A4) and using (15) we can express the phase margin as (assuming $C_L \gg C_{C1}$)

$$\Phi = \tan^{-1}\left[\frac{\left(\frac{g_{mb}}{g_{m1}}\right)^3}{\left(\frac{g_{mb}}{g_{m1}}\right)^2+2}\right]. \tag{16}$$

Again, the exact solution of (16) for g_{mb}/g_{m1} is too complex and is therefore approximated with an error lower than 6% for Φ ranging from 45° to 85° by

$$\frac{g_{mb}}{g_{m1}} = \tan\Phi + 0.7. \tag{17}$$

The design constraint on asymptotic stability is carried out by applying (A7) in the Appendix

$$\omega_{\mathrm{GBW}} < \frac{C_{C1}+C_L}{C_L}\frac{g_{mb}}{C_{C1}} \approx \frac{g_{mb}}{C_{C1}}. \tag{18}$$

In this case both g_{m2} and g_{m3} could be set even smaller than g_{m1}, thus allowing power and area saving, but in general to preserve amplifier performance this choice is not convenient. Besides, it is apparent that the derived design equations of the RAFFC topology depends only on the ratio of transconductances and capacitors layouted by the designer (C_{C1}, C_{C2}) and on C_L. In contrast, the solutions proposed in [12] and [13], show a dependence on the parasitic capacitance at the output of the first stage, which strongly depends on the specific topology and transistor dimensions of the first (and second) stage. Therefore, simulations are mandatory to get the value of compensation capacitors, even in a first pencil-and paper design step (note that many other recent compensation strategies also depend upon parasitics, e.g., [14], [15], [23]).

It is also apparent that the RAFFC technique achieves, in principle, similar performances of RNMCFNR. Nevertheless, the advantage of this solution arises in a low power context, i.e., when small values of the stage transconductances are set. Indeed, in this case RNMCFNR would require high values of R_C to accomplish the zero cancellation (which, in turn, involves increased area occupation). Moreover, as will be clarified later, the RAFFC solution does not entail extra transistors for its implementation. Therefore, it is the simplest compensation topology among those presented in literature, since it requires only two capacitors, just like the basic NMC and RNMC topologies.

III. Circuit Implementations

To prove the effectiveness of the proposed compensation techniques and show the advantage over other previously reported solutions, we fabricated two OTAs in a 0.5-μm CMOS (AMI-MOSIS) standard process. Both amplifiers were designed to reach a gain-bandwidth product of about 2 MHz and a phase margin of 60° with a (off chip) capacitive load of 500 pF and a 3-V supply. Moreover, a low-power version of the RAFFC topology is easily obtained by directly reducing the stage quiescent currents. It dissipates 1/3 of the current of the previous solution, while achieving 1/2 of the target gain-bandwidth product (and the same phase margin).

A. RNMCFNR

The simplified schematic of the implemented three-stage amplifier compensated using the RNMCFNR technique is shown in Fig. 4. The first stage is made up of a pMOS differential pair (M1–M2) with a current mirror load (M3–M4). The second inverting stage is realized by common source M6–M5, while the last noninverting stage is made up by M7–M10. The feedforward stage g_{mf} is generated exploiting the active load transistor M10 of the last stage, whose gate is connected to the output of the first stage.

Moreover, with this connection M9–M10 act as a pseudoclass AB output stage able to drive the load capacitor, C_L, with a current much higher than the output branch quiescent current. As a result, slew rate is in principle ultimately determined by the maximum available current from the first stage charging C_{C1} and C_{C2}.

To achieve the target gain-bandwidth product of 2 MHz, we set $g_{m1} = 140$ μA/V and $C_{C1} = 11$ pF, according to (4). Then, to obtain the phase margin of 60°, using (12) we set $g_{m2} = 450$ μA/V. Besides, using (6) and (10) we set $g_{m2} = g_{m3} = g_{mf} = 450$ μA/V. Consequently, the required value of R_C was 1.1 kΩ [see (5)]. Finally, the compensation capacitor C_{C2} was set using (8). It was equal to 0.48 pF. With the aid of computer simulations, the compensation capacitors C_{C1} and C_{C2} were fine tuned to 11.5 and 0.35 pF, respectively. The drain current of M1–M2 was set equal to 10 μA, while the drain current of the second and last stage was 20 μA, thus achieving a total current consumption of 80 μA (plus other 5 μA required by the biasing network, not shown in Fig. 4). Transistors dimensions are reported in Table I. Fig. 5 shows the simulated post-layout open-loop frequency response of the amplifier. The dc gain was equal to 109 dB, the gain-bandwidth product was 2.3 MHz with a phase margin of 58°.

B. RAFFC

The simplified schematic of the implemented three-stage amplifier compensated using the RAFFC technique is shown in

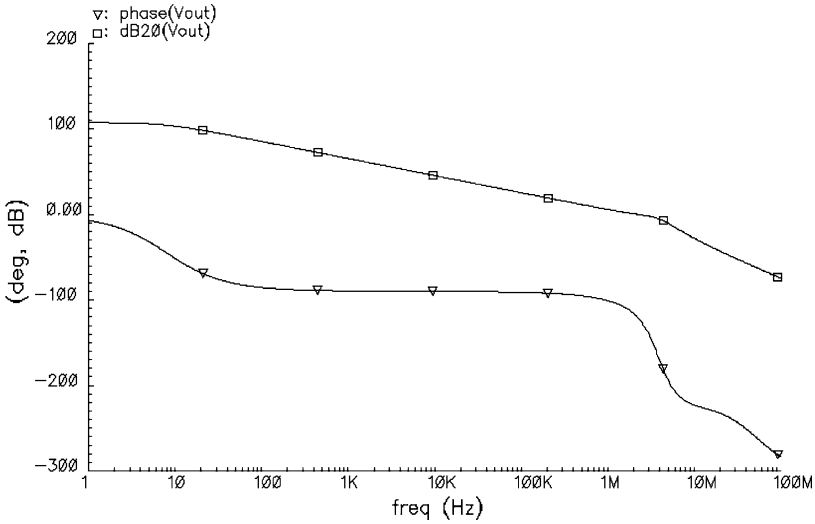

Fig. 5. Simulated open-loop frequency response of the RNMCFNR amplifier.

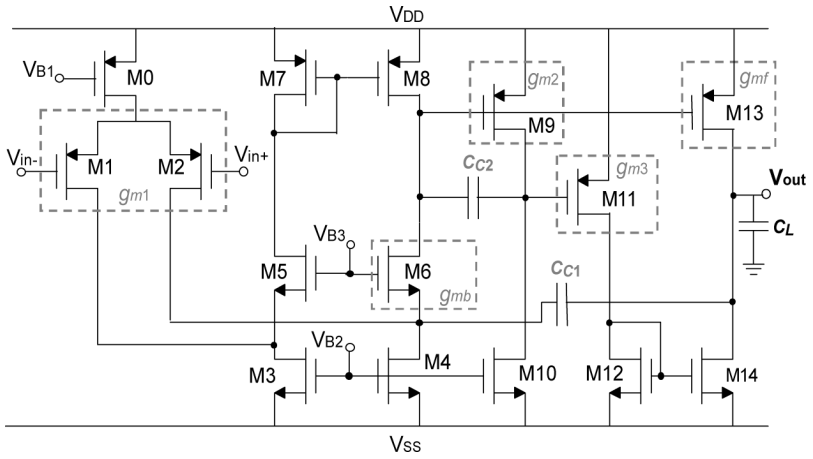

Fig. 6. Schematic of the three-stage amplifier compensated using the RAFFC technique.

TABLE I
TRANSISTORS DIMENSIONS FOR RNMCFNR

Transistor	Aspect ratio
M0, M6, M8, M9	4x(30/1.8)
M1, M2	18/0.6
M3, M4	30/0.6
M5, M7, M10	2x(30/0.6)

Fig. 6. The first stage is a traditional folded cascode stage with a pMOS input differential (M0–M8). The second stage is the common source M10, M9 while the last noninverting stage is realized through transistors M11–M14.

Again, the feedforward stage g_{mf} is generated by exploiting the active load transistor M13 of the last stage, whose gate is connected to the output of the first stage.

Thus, with this connection M13–M14 act as a pseudoclass AB output stage and the slew rate is therefore determined by the maximum available current from the first stage charging C_{C1} and C_{C2}.

Compared to the previous solution, this one ensures that the common mode input range can reach the lower rail voltage V_{SS} (0 V). Moreover, it allows implementing the additional transconductance stage g_{mb} of the compensation network exploiting the common gate M6. This is achieved by simply connecting C_{C1} at the source of M6, rather than to its drain, which is the output of the first stage [15]. As a result, only two capacitors are required for the compensation network, just like the basic RNMC of Fig. 1. Therefore, this compensation approach is the simplest among all those previously reported, the most efficient of which usually require extra circuitry (and bias currents) to implement the additional transconductance stages of the compensation network [11]–[15], [18].

To achieve the target gain-bandwidth product of 2 MHz, we set again $g_{m1} = 140$ μA/V and $C_{C1} = 11$ pF, according to (4). Then, to obtain the phase margin of 60°, using (20) we found $g_{mb} = 340$ μA/V. However, after transistor-level fine tuning at the simulator, we reduced g_{mb} to 280 μA/V. Then, we set $g_{m2} = g_{m3} = g_{mf} = 390$ μA/V. Note that the condition stated by (6) is satisfied with good accuracy since M11 and M13 are both p-channel devices (and therefore can be well matched by proper layout) and their current is tracked by current mirror M12–M14. Finally, the compensation capacitor C_{C2} was

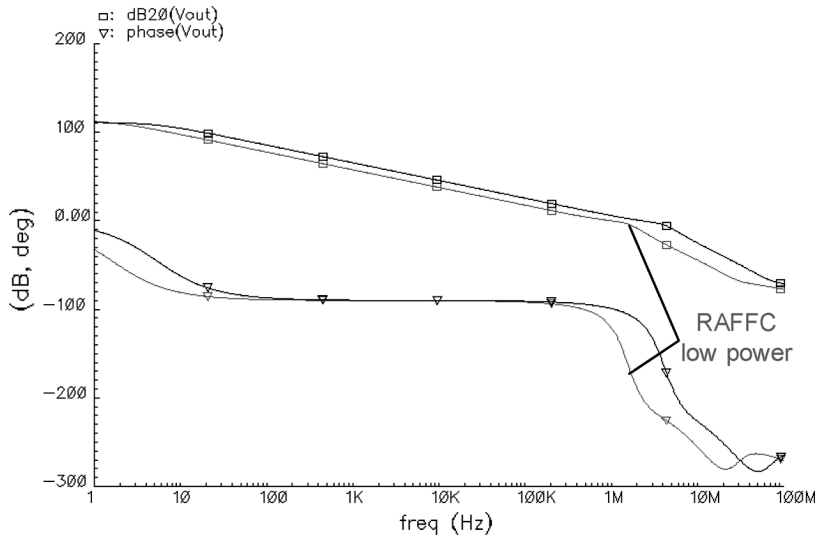

Fig. 7. Simulated open-loop frequency response of the RAFFC amplifier (black line) and the low power version (gray line).

TABLE II
TRANSISTORS DIMENSIONS FOR RAFFC

Transistor	Aspect ratio
M0	4x(30/0.9)
M1, M2	30/0.9
M3, M4, M9,M10, M11, M13	4x(30/0.9)
M5, M6, M7, M8	2x(30/0.9)
M12, M14	3x(30/0.9)

dimensioned using (16) which gives 0.56 pF. During the simulation step this value was again reduced to 0.35 pF, without significantly changing the target phase margin (note that this variation involves a reduction of the damping factor of the second-order polynomial with a consequent settling time reduction [23]). The drain current of M1–M2 was set equal to 10 μA, while the drain current of the second and last stage was 20 μA, thus achieving a total current consumption of 100 μA (plus other 5 μA due to the biasing network, not shown in Fig. 6). Transistors dimensions are reported in Table II. Fig. 7 shows the simulated open-loop frequency response. The resulting dc gain, gain-bandwidth product and phase margin are equal to 112 dB, 2.4 MHz, and 60°, respectively.

It is worthwhile noting that although the stage transconductances have almost the same value in both circuits, the solution shown in Fig. 6 requires higher current to bias the input stage owing to the folded cascode topology. However, since the design equations of RAFFC depend upon the ratio of the transconductance stages, once C_{C1} and C_{C2} are set, the phase margin remains constant if all the transconductances are scaled down by the same factor (of course, if g_{m1} is reduced maintaining C_{C1} at a fixed value, the gain-bandwidth product is also reduced). This reduction can be simply accomplished by scaling down the reference current. Indeed, by reducing all the branch currents by 33%, the transconductances are $g_{m1} = 54$ μA/V, $g_{m2} = g_{m3} = g_{mf} = 160$ μA/V, $g_{mb} = 95$ μA/V, giving a gain-bandwidth product of 1 MHz and a phase margin of 58°.

The simulated post-layout frequency response is superimposed in Fig. 7 (gray line). Note, as a final observation, that this strategy cannot be adopted in the RNMCFNR once layout is finished, since lower transconductances would require higher values of R_C to ensure the same phase margin.

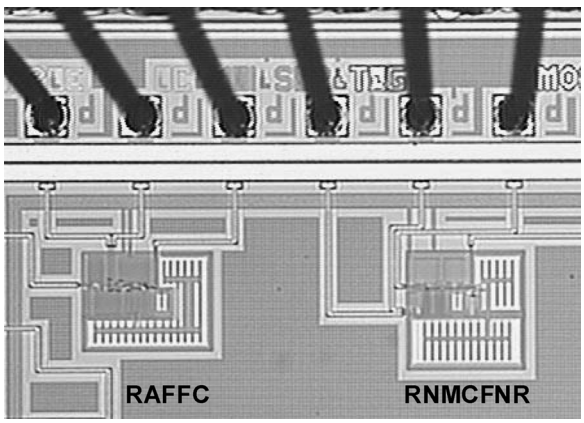

Fig. 8. Microphotograph of the two proposed amplifiers.

IV. EXPERIMENTAL RESULTS AND PERFORMANCE COMPARISON

A. Experimental Results

Fig. 8 shows a microphotograph of the fabricated chip. The implemented amplifiers were experimentally tested for both dc and ac specifications.

Figs. 9 and 10 show the response of the amplifiers in unity-gain configuration to a 500-mV_{pp} input step.

A detail of the frequency response (magnitude and phase) near the unity gain frequency is also plotted in Figs. 11–13 for the RNMCFNR, RAFFC, and RAFFC low power, respectively. Approximately the same results were obtained using the indirect method proposed in [24], which allows us to determine the open-loop parameters of an amplifier by measuring its closed-loop 3-dB cut-off frequency and the corresponding phase.

Main performance parameters are summarized in Table III. Observe that negative settling time of RAFFC low power is the

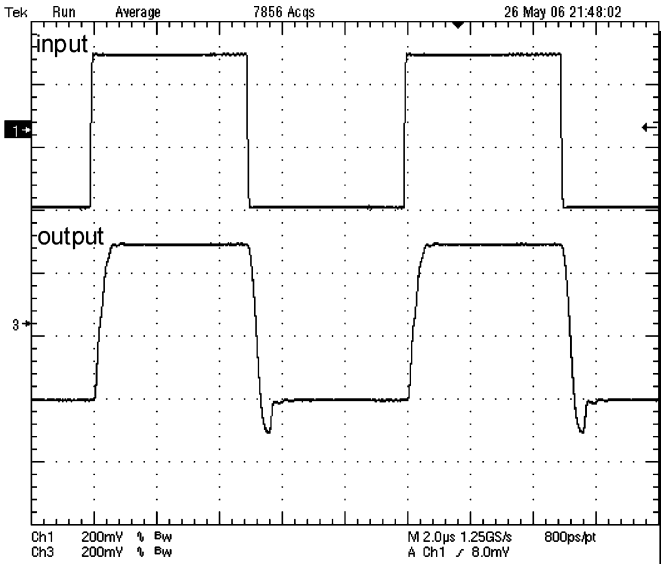

Fig. 9. Measured unity-gain transient response of RNMCFNR amplifier.

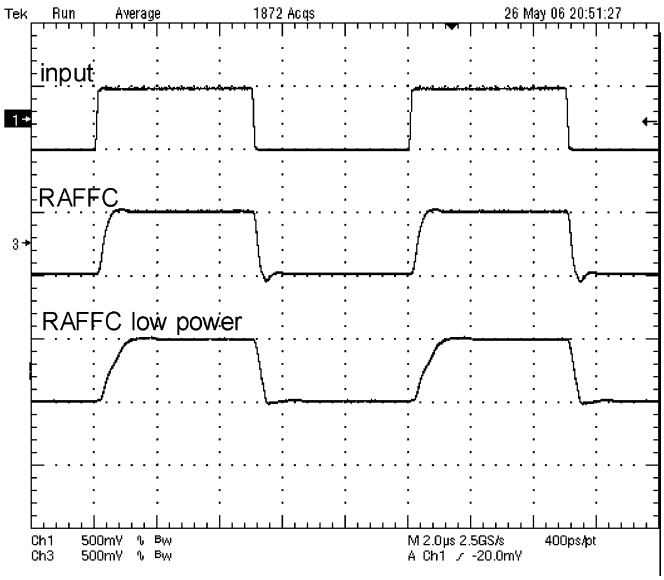

Fig. 10. Measured unity-gain transient responses of the RAFFC amplifier and its low power version.

lowest one, owing to the absence of (negative) peaking in its step response.

Additional measurements were also executed adding a 25-kΩ resistor in parallel to the 500-pF load. In this case a reduction of the DC gain of about 9 dB was observed for all topologies, whereas an increase in the phase margin of about 6°, 7° and 8° was measured for RNMCFNR, RAFFC, and RAFFC low power, respectively. Moreover, due to the pseudoclass AB output stage topology, no significant change in the time response of the amplifiers was detected.

B. Performance Comparison

The performance comparison of different amplifiers is usually carried out by using two figures of merit, referring to the small-signal and large-signal behavior. The originally adopted figures of merit were [11]–[16]

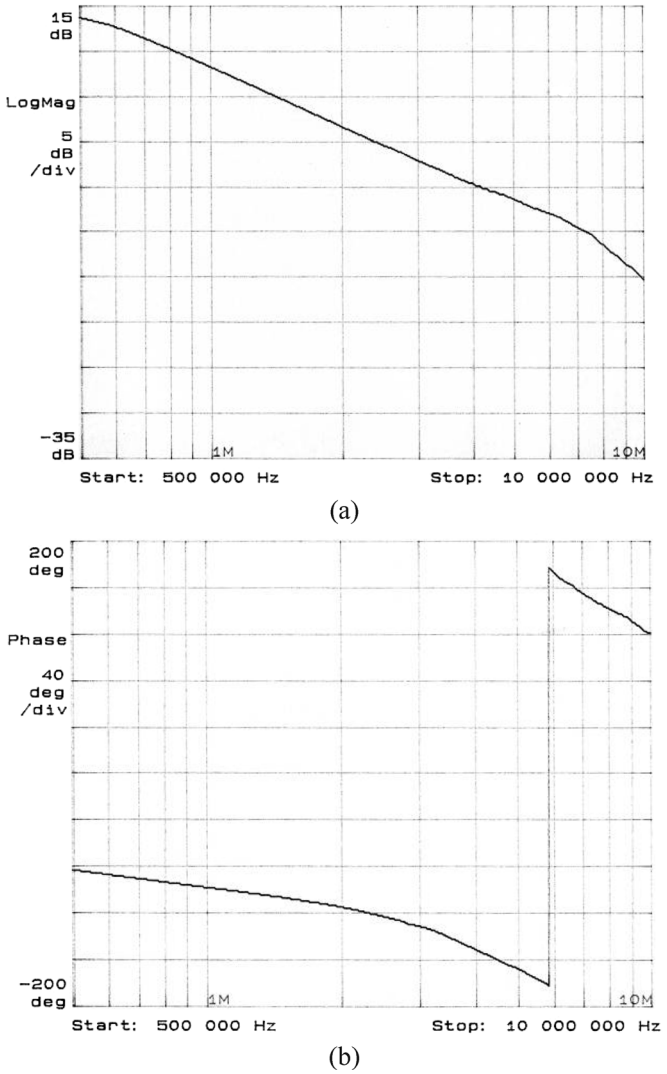

Fig. 11. Frequency response near the gain-bandwidth product of RNMCFNR amplifier. (a) Magnitude. (b) Phase.

$$\mathrm{FOM}_S = \frac{\omega_{\mathrm{GBW}} \cdot C_L}{\mathrm{Power}} \tag{19}$$

$$\mathrm{FOM}_L = \frac{\mathrm{SR} \cdot C_L}{\mathrm{Power}} \tag{20}$$

where SR is the slew rate and Power is the dc power consumption. The higher is the value of both FOM_S and FOM_L the better is the amplifier. However, these figures of merit may lead to imprecise results because they depend upon the supply voltage. Since ω_{GBW} and SR depend on the quiescent current flowing in the relevant transistors, to allow a fair comparison two more precise figures of merit were proposed in [14], [15]

$$\mathrm{IFOM}_S = \frac{\omega_{\mathrm{GBW}} \cdot C_L}{I_{dd}} \tag{21}$$

$$\mathrm{IFOM}_L = \frac{\mathrm{SR} \cdot C_L}{I_{dd}} \tag{22}$$

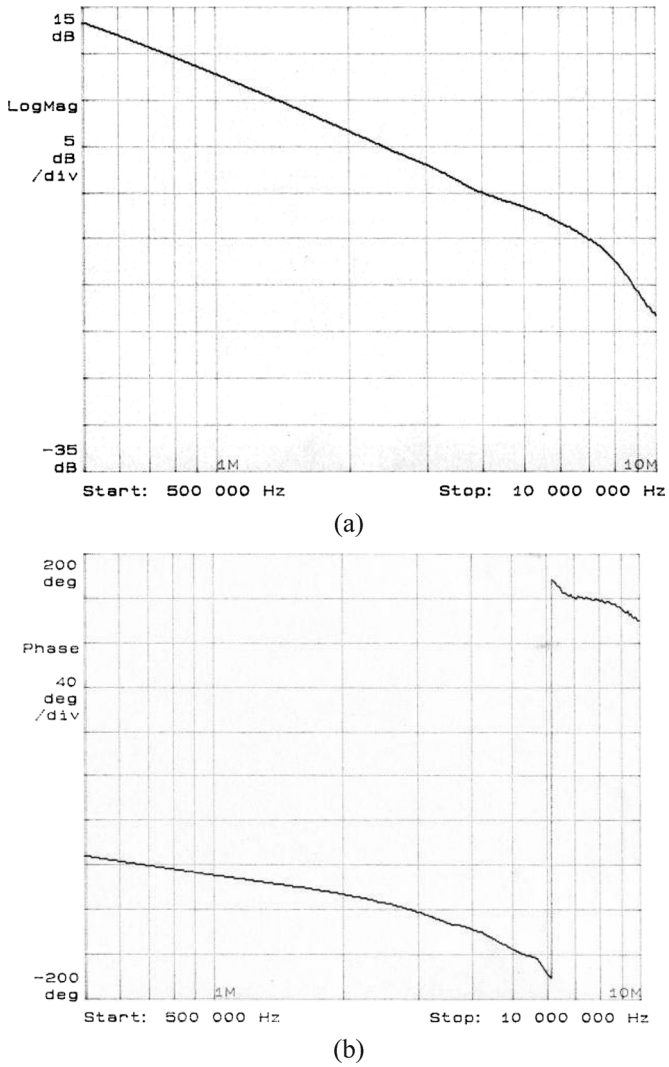

Fig. 12. Frequency response near the gain-bandwidth product of RAFFC amplifier. (a) Magnitude. (b) Phase.

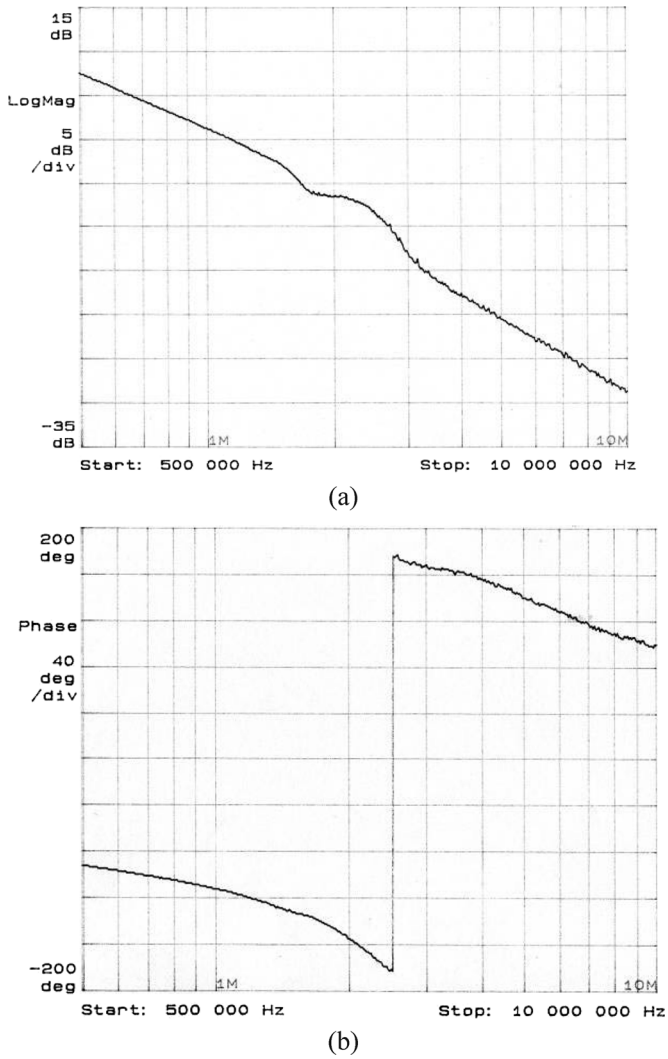

Fig. 13. Frequency response near the gain-bandwidth product of RAFFC low power amplifier. (a) Magnitude. (b) Phase.

By using these formulas, a comparison with other multistage amplifiers is reported in Table IV. The low power version of the RAFFC topology, obtained as explained in Section III-B, achieves the best overall performance. Note that the value of C_{C1} could be reduced in a further optimization to increase both the ω_{GBW} and SR. Among the other solutions reported in literature, only [15] shows comparable performance with RAFFC. However, this compensation technique requires additional circuitry for the implementation of the compensation network. Moreover, a careful optimization step using a circuit simulator must be performed, since design equations depend upon parasitics, and is therefore particularly exposed to process variations. On the contrary, the design of the two considered solutions is straightforward and can be almost completely performed in a pencil-and-paper design step. Indeed, the main advantage of the RAFFC technique is its inherent low complexity, since only two capacitors are needed for its implementation, provided that a folded cascode input stage is used. Finally, it was shown that its power consumption can be simply reduced diminishing the external reference current, without compromising the amplifier phase margin.

TABLE III
MAIN PERFORMANCE PARAMETERS

	RNMCFNR	RAFFC	RAFFC low power
Technology	0.5 μm CMOS		
Power Supply (V)	3		
Loading Capacitance	500 pF		
Area (mm^2)	0.025	0.024	
Total Bias Current (μA)	85	105	35
Input Offset Voltage (mV)	4.3	5.1	4.5
DC Gain (dB)†	109	112	113
Gain-bandwidth Product (MHz)	2.4	2.4	1.1
Phase Margin (deg)	58	58	56
CMRR @ DC (dB) †	79	80	83
PSRR @ DC (dB) †	75	81	84
Positive/Negative Slew Rate (V/μs) ††	1.8 / -1.8	2.1 / -1.8	0.78 / -1.8
Positive/Negative Settling Time at 1% (ns) ††	740 / 810	496 / 560	1000 / 400
HD2/HD3 @ 100 kHz, 100 mVpp (dB) ††	-58.3 / -53.1	-60.3 / -55.2	-57.3 / -51.1
HD2/HD3 @ 100 kHz, 500 mVpp (dB) ††	-54.2 / -50.4	-57 / -55.2	-51.2 / -48.4

† post layout simulation
†† in unity gain configuration

TABLE IV
COMPARISON OF DIFFERENT MULTI-STAGE AMPLIFIERS

	C_L (pF)	V_{DD} (V)	I_{TOT} (mA)	*Power* (mW)	*GBW* (MHz)	*Average SR* (V/µs)	*Comp. Capacitors* (pF)	FOM_S (MHz·pF)/mW	FOM_L (V/µs·pF/mW)	$IFOM_S$ (MHz·pF/mA)	$IFOM_L$ (V/µs·pF/mA)
MNMC [8]	100	8	9.5	76	100	35	C_{C1}= - C_{C2}= -	132	46	1053	368
NGCC [9]	20	2	0.34	0.68	0.61	2.5	C_{C1}= - C_{C2}= -	18	74	36	148
NMCFNR [10]	100	2	0.2	0.406	1.8	0.79	C_{C1}=30 C_{C2}=5.3	443	195	886	390
DFCFC [11]	1000	2	0.2	0.426	1	0.36	C_{C1}=55 C_{C2}=3	2347	845	4694	1690
AFFC [13]	100	1.5	0.17	0.25	5.5	0.36	C_{C1}=5.4 C_{C2}=4	2200	564	3235	212
ACBCF [14]	500	2	0.162	0.324	1.9	1	C_{C1}=10 C_{C2}=3	2932	1543	5864	3086
TCFC [15]	150	1.5	0.03	0.045	2.85	1.035	C_{C1}=1.1 C_{C2}=0.92	9500	3450	14250	5175
DPZCF [16]	500	1.5	0.15	0.225	1.4	2	C_{C1}=30 C_{C2}=20	3111	4444	4667	6666
RNMC with VB NR [18]	15	3	0.48	1.44	19.46	13.8	C_{C1}=3 C_{C2}=0.7	209	149	608	431
SMFFC [21]	120	2	0.21	0.42	9	3.4	C_{C1}=4 (one)	2571	971	5143	1943
RNMCFNR (This work)	**500**	**3**	**0.085**	**0.255**	**2.4**	**1.8**	**C_{C1}=11.5 C_{C2}=0.35**	**4706**	**3529**	**14118**	**10588**
RAFFC (This work)	**500**	**3**	**0.105**	**0.315**	**2.4**	**1.95**	**C_{C1}=11 C_{C2}=0.35**	**3810**	**3095**	**11430**	**9285**
RAFFC low power (This work)	**500**	**3**	**0.035**	**0.105**	**1.1**	**1.29**	**C_{C1}=11 C_{C2}=0.35**	**5238**	**6143**	**15714**	**18429**

C. Compensation Networks Comparison

In order to better highlight the topological advantages of the proposed solutions with respect to the nonreversed counterparts independently of the particular amplifier topology, design choices and technology, we carry out an analytical comparison based on the figure of merit, introduced by the authors in [22],[1] which relates load capacitance, gain-bandwidth product and the total transconductance of the three-stage amplifier

$$\begin{aligned}\mathrm{FOM} &= \frac{\omega_{\mathrm{GBW}} \cdot C_L}{g_{m1} + g_{m2} + g_{m3} + g_{\mathrm{mCOMP}}} \\ &= \frac{G_{Nm1}}{G_{Nm1} + G_{Nm2} + 1 + \frac{g_{\mathrm{mCOMP}}}{g_{m3}}} \frac{C_L}{C_{C1}}\end{aligned} \tag{23}$$

where $G_{Nm1} = g_{m1}/g_{m3}$, $G_{Nm2} = g_{m2}/g_{m3}$ and g_{mCOMP} represents the sum of the compensation network transconductances, if any, which require additional bias current (i.e., more power consumption) for their implementation.

Several considerations lead to define the figure of merit in (23). Not only the transconductance is a key design parameter in the small-signal domain, but it is also strictly related to other significant design aspects such as power consumption and silicon area. Indeed, the transconductance shows the trade-off between transistor area and bias current. On the other hand, remembering that for a CMOS transistor operating in saturation $g_m = 2I_{\mathrm{TOT}}/V_{\mathrm{DSsat}}$ and assuming an almost equal V_{DSsat} for the transistors of the amplifiers being analyzed, the transconductance represents an assessment of current dissipation only. Moreover, and perhaps more significantly, the FOM in (23) can be analytically evaluated starting from the design equations derived in the previous section, regardless technology and other design choices. Thus, the comparison among different compensation topologies can be carried out through the behavior of their FOMs.

The FOM in (23) for the proposed topologies and the nonreversed counterparts, NMCFNR and AFFC, versus the phase margin, Φ, and parameters G_{Nm1}, G_{Nm2} is summarized in Table V. In particular, the RNMCFNR and RAFFC FOMs were derived by using the design equations reported above (the value of C_{C1} obtained from (8) and (15) were used, thus considering C_{C2} as a free parameter [20]). On the other hand, NMCFNR and AFFC FOMs are evaluated in [22], where also their design strategies are presented.

Referring to Table V, parameter c_{No1} represents the ratio between the parasitic capacitance at the output of the first stage of AFFC and the load capacitance C_L and $c_{NC2} = C_{C2}/C_L$.

It should be noted that for all topologies the transconductance g_{mf} is not included in the FOM evaluation since it is always implemented using the load transistor of the last stage [10], [12], [13], [20] and therefore no additional bias current is required for its implementation. The same assumption was made for the transconductance g_{mb} of RAFFC which was again implemented exploiting the transistors of the basic amplifier topology [20].

Without loss in generality, we make the comparison assuming a phase margin equal to 70°, because this value allows us to optimize the 1% settling time [5], [25]. Nevertheless, almost the same results can be found for different phase margin values.

Fig. 14 compares the FOM of NMCFNR with the proposed nonreversed counterpart for different values of G_{Nm2}, and

[1]In this manuscript we do not further report and discuss the comparison among the several NMC topologies, since they are deeply analyzed in [22]. In [22], the reader can also find a more in depth discussion regarding the proposed FOM.

TABLE V
ANALYTICAL FOM EXPRESSIONS

NMCFNR [10]	$\frac{2}{\left(G_{Nm1}+G_{Nm2}+1\right)\left(\tan\left(\Phi-\tan^{-1}\left(\frac{G_{Nm1}}{2}+\frac{1}{\tan\Phi+\sqrt{\tan^2\Phi+2}}\right)\right)+\sqrt{\tan^2\left(\Phi-\tan^{-1}\left(\frac{G_{Nm1}}{2}+\frac{1}{\tan\Phi+\sqrt{\tan^2\Phi+2}}\right)\right)+2}\right)}$
RNMCFNR (This work)	$\frac{4}{3G_{Nm1}\left(\tan\Phi+1\right)+2}\sqrt{\frac{G_{Nm1}}{c_{NC2}\left(3\tan\Phi+1\right)}}$
AFFC [12], [13]	$\frac{\sqrt{2\left(1-G_{Nm2}\right)G_{Nm1}}}{\sqrt{c_{No1}\left(\tan\left(\Phi-\Phi_B\right)+\sqrt{\tan^2\left(\Phi-\Phi_B\right)+2}\right)}\left(G_{Nm1}\left(1+\tan\left(\Phi-\Phi_B\right)+\sqrt{\tan^2\left(\Phi-\Phi_B\right)+2}\right)+G_{Nm2}+1\right)}$ $\Phi_B=\tan^{-1}\left(\frac{1}{\tan\Phi+\sqrt{\tan^2\Phi+2}}\right)$
RAFFC (This work)	$\frac{1}{G_{Nm1}+G_{Nm2}+1}\sqrt{\frac{G_{Nm1}}{c_{NC2}\left(\tan\Phi+0.7\right)}}$

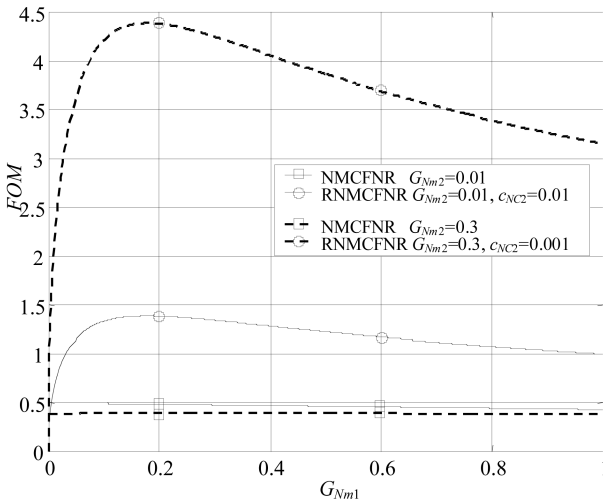

Fig. 14. Analytical comparison of the proposed RNMCFNR versus NMCFNR in [10].

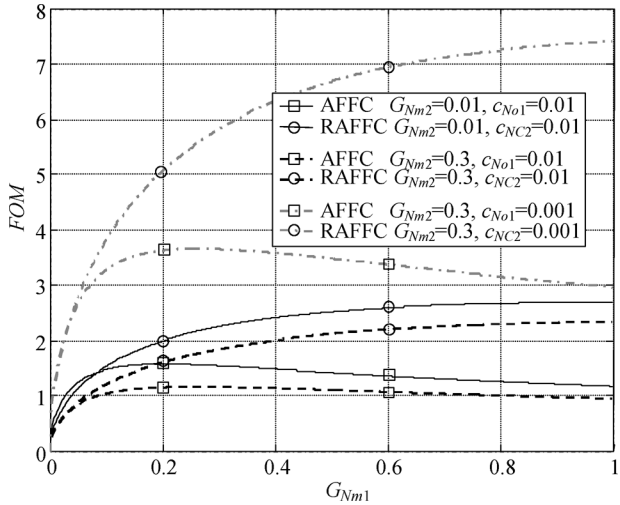

Fig. 15. Analytical comparison of the proposed RAFFC versus AFFC in [12].

c_{NC2}. It can be seen, as expected, that the performance of RNMCFNR is better than NMCFNR in all conditions, but especially in the presence of higher capacitive loads (i.e., smaller values of c_{NC2}).

Analogously, Fig. 15 compares the FOM of AFFC and RAFFC for different values of G_{Nm2}, c_{NC2} and c_{No1}. It can be seen that the proposed solution shows always a higher FOM value when $G_{Nm1} > 0.1$, whereas performances are comparable if $G_{Nm1} < 0.1$ (i.e., when g_{m3} is much higher than g_{m1}).

Finally, comparing Fig. 14 and 15 it appears that RAFFC FOM is higher than the RNMCFNR one for $g_{m1}/g_{m3} > 0.2$.

V. CONCLUSION

Two compensation techniques improving the basic RNMC topology were presented. The techniques were theoretically analyzed and design equations to achieve the desired phase margin developed. Two amplifiers exploiting the two techniques were fabricated and showed a significant improvement in both small-signal and large-signal performances with respect to already presented implementations. As a further advantage, the compensation approaches require a straightforward design and implementation, since only passive components are required. In particular, the RAFFC technique requires only two capacitors, while achieving the best performance. Finally, an analytical comparison between the proposed solutions and the nonreversed counterparts showed the inherent improvements of the topologies developed.

APPENDIX A

In this section, we briefly present some general results for a generic three-stage amplifier.

A. Phase Margin Evaluation

Let $A_v(s)$ represents the open-loop transfer function of a generic three-stage amplifier

$$A_{\rm v}(s)=A_0\frac{1+sb_1+s^2b_2}{\left(1+\frac{s}{\omega_{P1}}\right)\left(1+sa_1+s^2a_2\right)}. \qquad \text{(A1)}$$

The phase margin Φ is expressed by

$$\Phi = 180^\circ - \tan^{-1}\left(\frac{\omega_{\rm GBW}}{\omega_{p1}}\right) - \tan^{-1}\left(\frac{a_1\omega_{\rm GBW}}{1-a_2\omega_{\rm GBW}^2}\right) + \tan^{-1}\left(\frac{b_1\omega_{\rm GBW}}{1-b_2\omega_{\rm GBW}^2}\right). \quad \text{(A2)}$$

Since $\omega_{P1} \ll \omega_{\rm GBW}$, (A2) can be approximated as

$$\Phi = \tan^{-1}\left(\frac{1-a_2\omega_{\rm GBW}^2}{a_1\omega_{\rm GBW}}\right) + \tan^{-1}\left(\frac{b_1\omega_{\rm GBW}}{1-b_2\omega_{\rm GBW}^2}\right). \quad \text{(A3)}$$

Finally, by applying the well-known properties of trigonometric functions, after a few algebra we get

$$\Phi = \tan^{-1}\frac{\left(1-a_2\omega_{\rm GBW}^2\right)\left(1-b_2\omega_{\rm GBW}^2\right)+a_1b_1\omega_{\rm GBW}^2}{\omega_{\rm GBW}\left[a_1\left(1-b_2\omega_{\rm GBW}^2\right)-b_1\left(1-a_2\omega_{\rm GBW}^2\right)\right]}. \quad \text{(A4)}$$

To avoid frequency peaking in the open-loop frequency response, which may cause instability due to the reduced gain margin value, a proper value of the damping factor of the second-order polynomial at the denominator of (A1) must be chosen [5], [6]. After setting $\xi = 1/\sqrt{2}$ (which guarantees a flat frequency response, while representing a good compromise between bandwidth and stability) we get

$$a_2 = \frac{a_1^2}{2}. \quad \text{(A5)}$$

B. Asymptotic Stability

Now let us develop a general criterion for the stability of a generic three-stage amplifier whose open-loop transfer function can be expressed as (A1). Since the polynomial order at the denominator of (A1) is higher than the numerator, stability is determined only by the denominator of the closed-loop transfer function in unity gain configuration given by [5], [9].

$$A_{\rm v,CL}(s) = A_0\frac{1}{1+s\frac{1}{\omega_{\rm GBW}}+s^2\frac{a_1}{\omega_{\rm GBW}}+s^3\frac{a_2}{\omega_{\rm GBW}}}. \quad \text{(A6)}$$

By applying the Routh–Hurwitz criterion [12]–[15] to (A6), the following relation is found:

$$a_1 > a_2\omega_{\rm GBW}. \quad \text{(A7)}$$

It is worth noting that (A7), which states a condition for the unconditional stability, also states a constraint on the maximum intrinsically achievable gain-bandwidth product of the amplifier.

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