Low-Voltage Operational Amplifier with Rail-to-Rail Input and Output Ranges

JOHAN H. HUIJSING, SENIOR MEMBER, IEEE, AND DANIEL LINEBARGER, MEMBER, IEEE

Abstract—**An operational amplifier is described which can perform precision signal operations in nearly the full supply voltage range, even when this range is as slow as 1.5 V totally. The untrimmed input offset voltage is typically 0.3 mV in an input common-mode (CM) voltage range which extends beyond both supply voltages for about 200 mV. The output voltage can reach each supply rail within 150 mV. A nested-loop frequency-compensation scheme yields a stable unity-gain bandwidth of 0.6 MHz while the low-frequency open-loop voltage gain is 110 dB. The op amp is integrated in a standard low-cost bipolar process and the chip measures 1.5×1.7 mm^2.**

I. Introduction

OPERATIONAL amplifiers for low supply voltages should be able to utilize the largest possible part of the supply-voltage range for input and output signal operations in order to get the best signal-to-noise ratio. Usually, base–emitter or gate–source voltages prevent the input and/or output from reaching the positive and/or negative supply voltages within about 0.7 V [1]. This becomes a problem when the supply voltage is low as in battery-powered systems or in low-power applications.

The operational-amplifier design presented here includes three new solutions to low supply-voltage operation: firstly, an input stage with a rail-to-rail common-mode input-voltage range which achieves a constant transconductance over the full common-mode range; secondly, a rail-to-rail class-*AB* output stage; and thirdly, a simple overall frequency compensation structure that allows a large gain with three or more common-emitter stages in cascade. With these measures an operational amplifier capable of performing precision operations on signals in the nearly full supply-voltage range has been obtained.

II. Input Stage

Rail-to-rail common-mode voltage swing at the input can only be obtained by using two input stages in parallel such that the common-mode (CM) voltage of one can reach the positive supply rail and that of the other the negative supply rail.

An example of such an existing input stage is given in Fig. 1. [2], [3]. Two complementary emitter-coupled transistor pairs are connected in parallel to the input. The input of the n-p-n pair Q_1, Q_2 can reach the positive supply provided the voltage drops across the collector resistances R_{10} and R_{11} do not cause significant saturation of these transistors. Similarly, the input of the p-n-p pair Q_3, Q_4 can reach the negative supply. The collector currents of the input transistors are summed by four folded cascode transistors Q_8–Q_{11} into one output current. Transistor Q_8 is connected as a diode to ensure that the outputs of Q_2, Q_4 are properly subtracted from those of Q_1, Q_3.

Three common-mode input voltage ranges can be distinguished.

1) In the range from the negative supply voltage V_{EE} to $V_{EE}+0.7$ V only the p-n-p pair Q_1, Q_2 is operating.
2) In the range from the positive supply voltage V_{CC} to $V_{CC}-0.7$ V only the n-p-n pair Q_3, Q_4 is operating.
3) In the intermediate range both pairs are operating.

When the CM voltage moves from one range into another the transconductance of the input stage changes by a factor of two. This prevents frequency compensation from being optimal since the bandwidth is proportional to that transconductance. Moreover, transient distortion occurs when fast changes in the common-mode voltage abruptly saturate and restore the tail-current sources.

These drawbacks can be overcome by the activation of only that input transistor pair which is able to function properly. In Fig. 2 [4] the n-p-n pair is normally activated by the current source I_{B1} via Q_5 and the current mirror Q_6, Q_7, while the p-n-p pair is nonconducting. That is the case when the common-mode input voltage is at least 60 mV higher than the reference voltage $V_{B1}=0.8$ V at the base of Q_5. When the input CM voltage decreases through the reference voltage V_{B1}, the emitter current is gradually steered from the emitter of Q_5 to the p-n-p pair, removing current from the n-p-n pair. A turnover between 10 and 90 percent of the current takes place in a voltage turnover range of about 120 mV, centered around the reference voltage V_{B1}. Since the transconductance of bipolar transistors is proportional to their emitter current, and since we keep the sum of the emitter currents constant, the transconductance of the combination of the p-n-p and n-p-n pairs is also constant. When the total supply voltage sinks below a value of about 1.5 V at 25 °C the transconductance strongly decreases in the middle of the CM range in which the current source I_{B1} becomes saturated.

The CM range extends above the positive as well as below the negative supply-rail voltage for about 0.2 V at 25

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J. H Huijsing was with the Signetics Corporation, Sunnyvale, CA 94086 He is now with the Delft University of Technology, Department of Electrical Engineering, Mekelweg 4,2628 DC Delft, Holland.

D Linebarger is with the Signetics Corporation, Sunnyvale, CA 94086.

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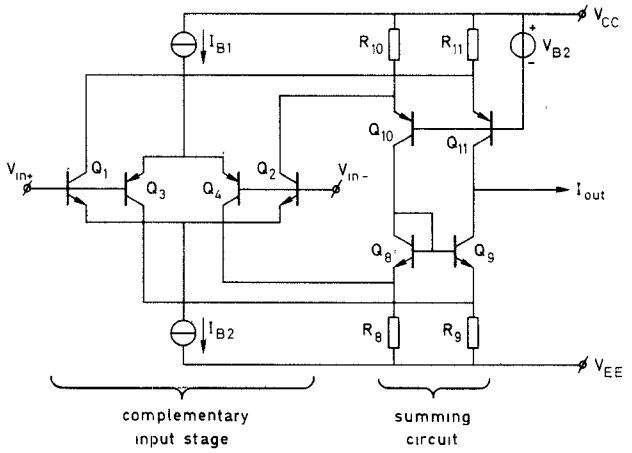

Fig. 1. Input stage with rail-to-rail common-mode voltage range.

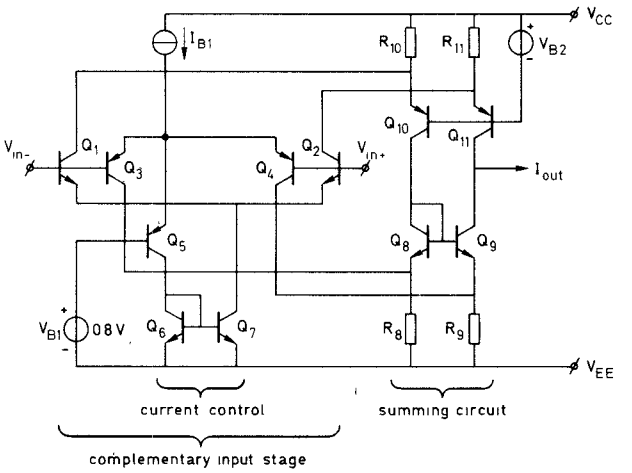

Fig. 2. Input stage with rail-to-rail common-mode voltage range and a constant transconductance over the full common-mode range.

°C, assuming the voltage across the resistors R_8–R_{11} is about 0.2 V.

An undesirable property of these kinds of input stages is that the input offset voltage will change between that of the n-p-n and p-n-p transistor pair when the CM input voltage crosses the turnover range. Proper circuit layout with a cross-coupled quad for each input pair can typically keep the untrimmed offset voltage change below 0.1 mV. The impact on signal operations is that the CM rejection ratio (CMRR) for signals within the turnover range will roughly be restricted to a value of minimally 120 mV/0.1 mV = 1200, or 62 dB. Moreover, the input supply current changes direction when the CM input voltage crosses the turnover range. To cope with this problem the bias current of the input transistors has been kept as low as 2 μA, leaving about a 30-nA bias current. The input offset current can be kept as small as a few nanoamperes.

III. Output Stage

Rail-to-rail output voltage swing cannot be obtained by the popular class-AB voltage-follower configuration. Instead, the push-and-pull output transistors must be connected in a common-emitter configuration.

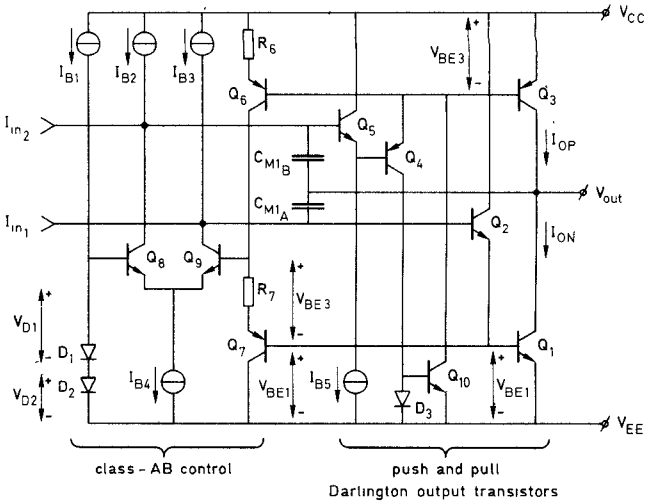

Fig. 3. Output stage with rail-to-rail output-voltage swing and accurate class-AB control.

Combining biasing and driving in this configuration would lead to a complex feedforward signal path, for example, like that in the low-voltage op amp LM10 [1].

The present design separates the functions of driving and biasing, as can be seen in Fig. 3 [5]. The n-p-n output transistor Q_1 is connected with the emitter follower Q_2 in a two-transistor combination. The p-n-p output transistor Q_3 is connected with the emitter followers Q_4 and Q_5 in a three-transistor combination. These output transistor combinations can directly be accessed by two driving signals, in equal phase, on their input bases. The biasing of the output transistor combinations is controlled, in opposite phase, by the two collector signals of the differential amplifier consisting of the transistors Q_8, Q_9. To this end the differential amplifier compares the summed voltages across two diodes D_1 and D_2 at the base of Q_8 with the summed voltages across the two base–emitter junctions of the output transistors Q_1 and Q_3 at the base of Q_9. To realize the summing of the base–emitter voltage of Q_3 this voltage is converted into a current by the base–emitter junction of Q_6 and resistor R_6 and reconverted into a voltage across the base–emitter junction of Q_7 and resistor R_7. The summed voltage across the emitter–base junctions of the output transistors Q_1 and Q_3 ($V_{BE1}+V_{BE3}$) is proportional to the logarithm of the product of the push and pull currents I_{OP} and I_{ON}, respectively. The combined voltages across diodes D_1 and D_2 ($V_{D1}+V_{D2}$) are proportional to the logarithm of the square of the reference current I_{B1}. When the diode characteristics and temperatures of the pairs Q_1, D_1 and Q_3, D_2 are equal, the feedback control will cause ($V_{BE1}+V_{BE3}$) to equal ($V_{D1}+V_{D2}$). As a result

$$I_{OP} \times I_{ON} = I_{B1}^2. \tag{1}$$

This relation shows an efficient class-AB biasing, in which none of the output transistors is ever completely cut off.

The dc and ac performance of the output stage, when implemented in a standard bipolar process, is dominated by the relatively poor performance of the lateral p-n-p output transistor Q_3. A 16× emitter provides a reasonable current gain at a 10-mA positive output current. To in-

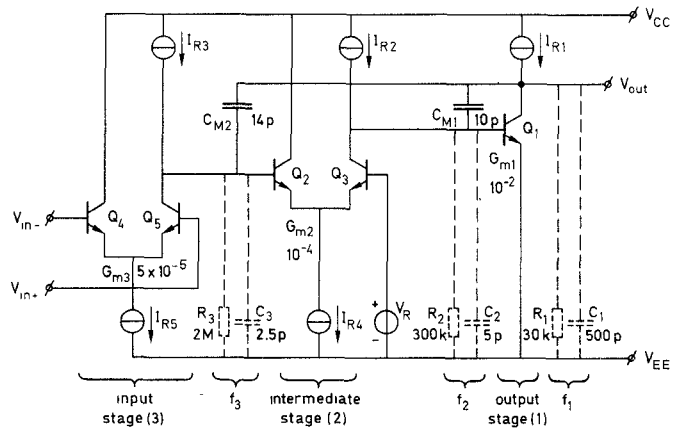

Fig. 4. High-frequency design with three common-mode emitter stages (simplified) and a nested Miller-compensation structure.

crease the current capability of the driver transistor Q_4, its current gain is boosted by a factor of 4 with a current mirror D_3, Q_{10}. When the total supply voltage decreases below a value of about 1.5 V the p-n-p output transistor combination Q_3, Q_4 is the first output transistor combination which cannot support 10 mA of output current. Moreover, the bandwidth of the output stage at positive output currents is limited by that of the lateral p-n-p output transistor Q_3 to a value of the order of 1 MHz.

There is no doubt that the amplifier characteristics such as output current capability, bandwidth, and slew rate would be much improved if Q_3 could be implemented with a vertical p-n-p transistor.

Separation of the functions of biasing and driving prevents the driving signals from being delayed by the biasing circuitry. The output transistor combinations are directly accessible by driving signals on their input bases, as shown in Fig. 3. This is very important for a simple high-frequency compensation. For example, the output transistor combinations can be HF compensated by Miller capacitors C_{M1A} and C_{M1B} between their collectors and their bases.

IV. High-Frequency Design

Having fulfilled the requirements at the input and output by the input stage and the output stage, respectively, we can now consider the overall design. The simplest approach would be to connect the output of the input stage with the input of the output stage [2], [6]. However, that combination does not have enough voltage gain for a general-purpose op amp when the output is loaded with a 1K resistance. Such a situation could be compared with a μA741 without an emitter-follower output stage [7].

The only way to increase the gain is to insert a common-emitter intermediate stage between the output stages. This is shown in a simplified form in Fig. 4. The circuit has three dominating poles, one at the output of each common-emitter gain stage. Simple pole splitting does not remove the third pole.

This situation is similar to that of the power op amp μA791 [8] or the BiMos op amp CA3130 [9]. In the first case the third pole is shifted to higher frequencies by reducing the gain of the output stage with local resistive feedback and in the second case the third pole is broadbanded with a relatively low output resistance. A method which more efficiently utilizes the gain for both the high-frequency linearization of the output stage and the low-frequency external loop is the nested differentiating feedback loop described by Cherry [10]. However, this method uses a rather complicated structure with poles and zeros which would require too many on-chip capacitors.

The present high-frequency design (Fig. 4.) uses two nested Miller integrators with only two low-value capacitors C_{M1} and C_{M2} [11]. C_{M1} is connected between the final output and the output of the intermediate stage. C_{M2} is connected between the final output and the output of the first stage.

The frequency characteristic of the intermediate and output stages is shown in Fig. 5(a). This combination has two pole frequencies f_1 and f_2. Insertion of the first Miller capacitor C_{M1} splits these frequencies such that f_2 is shifted to a higher frequency f_2' and f_1 to a lower frequency f_1'. The result is a well-compensated combination of the intermediate and output stages which allows feedback by a second Miller-integrator capacitor.

The frequency characteristic of the whole amplifier is shown in Fig. 5(b). It has the additional third-pole frequency f_3 of the input stage. After the first Miller capacitor C_{M1} is inserted, the frequency characteristic contains the pole frequencies f_1' and f_3. The second Miller capacitor C_{M2} splits these frequencies such that f_3 is shifted to a higher frequency f_3' and f_1' to a lowest frequency f_1''.

The result is a straight 6-dB/octave roll-off from one dominating pole frequency f_1'' down to 0 dB. No pole-zero cancellation has been applied, so that the frequency response has no pole-zero doublets in the passband. The nesting can basically be repeated by placing another noninverting amplifier in front of the left-hand stage and using another Miller capacitor.

V. Pole Frequencies

The pole frequencies of the uncompensated intermediate and output stages (Fig. 5(a)) are at $f_1 = 1/2\pi R_1 C_1 \simeq 10$ kHz and $f_2 = 1/2\pi R_2 C_2 \simeq 100$ kHz with $R_1 = 3$ kΩ, $C_1 =$ 500 pF, $R_2 = 300$ kΩ, $C_2 = 5$ pF, while the transconductances are $G_{m1} = 10^{-2}$ mho and $G_{m2} = 10^{-4}$mho, respectively. The p-n-p output transistor combination brings about a bandwidth-limiting pole frequency at $f_L \simeq 4$ MHz.

Insertion of $C_{M1} = 10$ pF shifts f_2 to a second bandwidth-limiting pole frequency f_2'

$$f_2' \simeq G_{m1}/2\pi C_1(1 + C_2/C_{M1}) \simeq 2 \text{ MHz} < 1/2f_L. \quad (2)$$

The factor in parentheses represents the attenuation in the feedback path through C_{M1} by C_2. Frequency f_2' should not exceed $1/2f_L$, otherwise complex poles would arise causing a "bump" in the frequency response near $1/2f_L$

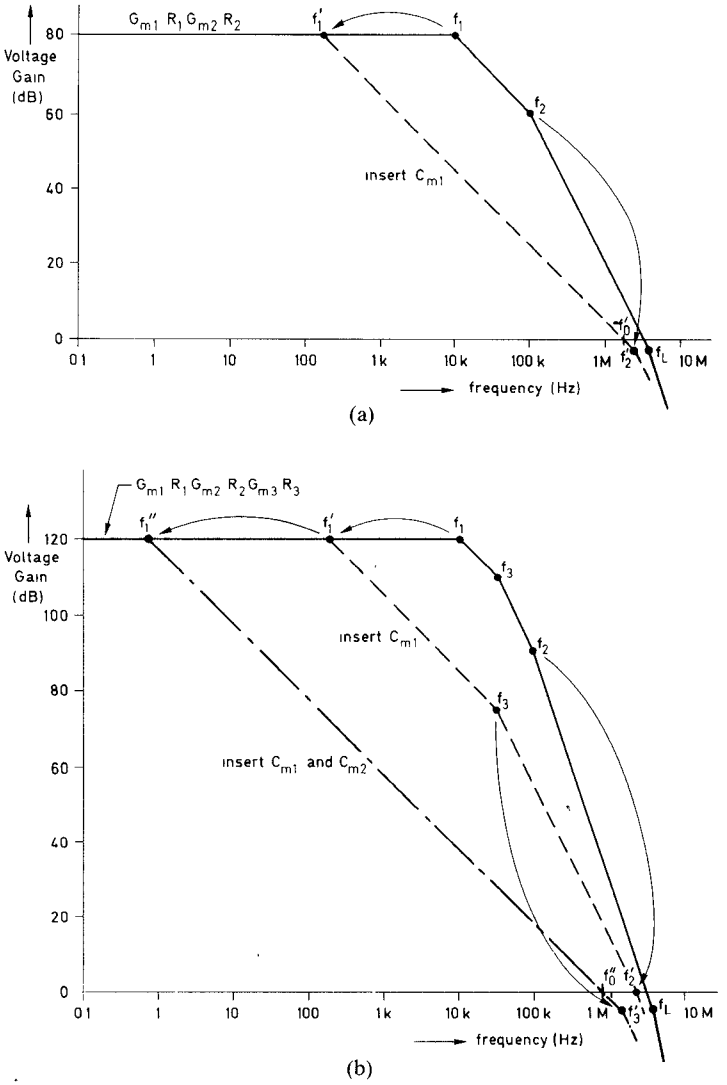

Fig. 5. (a) Frequency response of the output and intermediate stages of the amplifier of Fig. 4 with single Miller compensation. (b) Frequency response of the complete amplifier of Fig. 4 with nested Miller compensation.

[7]. Special care must be taken with the design of the p-n-p output transistor combination to avoid the "bump" at positive output currents higher than 0.25 mA, at which G_{m1} would increase too much.

The values of C_{M1} and G_{m2} are generally chosen such that the frequency f_0' at which the 6-dB/octave slope in the frequency response of the intermediate and output stage crosses the 0-dB line is lower than f_2'; hence

$$f_0' = G_{m2}/2\pi C_{M1} \simeq 1.6 \text{ MHz} < f_2'. \quad (3)$$

The low-frequency gain A_{12} in the intermediate and output stages equals

$$A_{12} = G_{m1} R_1 G_{m2} R_2 = 10^4. \quad (4)$$

The resulting lower pole frequency f_1' equals

$$f_1' = f_0'/A_{12} \simeq 160 \text{ Hz}. \quad (5)$$

When the input stage (Fig. 4) is included with the third pole frequency $f_3 = 1/2\pi R_3 C_3 \simeq 30$ kHz with $R_3 = 2$ MΩ and $C_3 = 2.5$ pF, while the transconductance is $G_{m3} = 5 \times 10^{-5}$ mho, the overall frequency response with C_{M1} again shows (Fig. 5(a)) two dominant pole frequencies f_1' and f_3 and a frequency-limiting pole f_2'. Insertion of $C_{M2} = 14$ pF shifts f_3 to a third bandwidth-limiting pole frequency f_3':

$$f_3' \simeq G_{m2}/2\pi C_{M1}(1 + C_3/C_{M2}) \simeq 1.3 \text{ MHz} < 1/2 f_2'. \quad (6)$$

The factor in parentheses represents the attenuation in the feedback through C_{M2} by C_3. If C_{M1} and G_{m2} had been chosen such that f_3' would exceed $1/2\ f_2'$, complex poles would have resulted. In fact, the present example has slightly complex poles. In addition to the poles, two zeros appear above 10 MHz, one of which is a right half plane zero. These zeros can be disregarded.

The values of C_{M2} and G_{m3} are generally chosen such that the frequency f_3'' at which the 6-dB/octave slope crosses the 0-dB line is lower than $1/2\ f_3'$ in order that the unity-gain feedback amplifier shows no overshoot in the

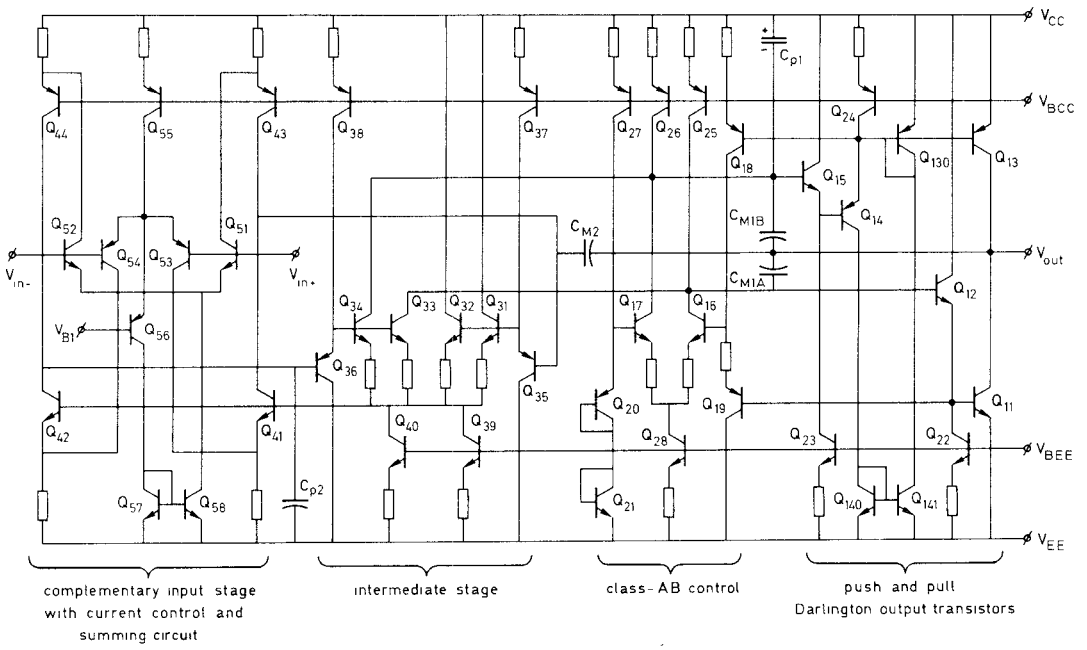

Fig. 6. Overall circuit of the low-voltage operational amplifier without circuitry for protection, clipping, and biasing.

pulse response. Hence

$$f_0'' = G_{m3}/2\pi C_{M2} \simeq 0.6 \text{ MHz} < 1/2f_3'. \tag{7}$$

With an overall low-frequency gain of

$$A_{123} = G_{m1}R_1G_{m2}R_2G_{m3}R_3 = 10^6 \tag{8}$$

the resulting dominant pole frequency f_1'' equals

$$f_1'' = f_0''/A_{123} \simeq 0.6 \text{ Hz}. \tag{9}$$

The resulting frequency response offers a low-frequency gain of 120 dB, equal to that of the uncompenstated amplifier, and a 6-dB/octave roll-off down to below unity gain with a 0-dB bandwidth of 0.6 MHz. Most of the high-frequency loop gain which has been spent for the compensation is used internally to linearize the class-*AB* output stage and to lower its output impedance.

VI. Overall Design

The circuit of the complete low-voltage operational amplifier is drawn in Fig. 6 without the circuitry for protection, clipping, and biasing.

The intermediate stage has not come up for discussion yet. Extending the symmetry of the input stage into the intermediate stage improves the common-mode rejection ratio. This ratio would otherwise suffer from the signal-dependent changes of the common-mode currents in the summing circuit. Instead of a single output, the input stage delivers a symmetrical pair of output currents to the intermediate stage at the bases of Q_{35} and Q_{36}. The common-mode component of these currents is controlled by feedback from the common-emitter point of the intermediate stage to the bases of Q_{41} and Q_{42} which are a part of the summing circuit. The symmetry of the intermediate stage necessitates the use of an extra capacitor C_{P2} which balances out the second Miller capacitor C_{M2} and provides this stage with the right high-frequency ground reference. The left-hand output side of the intermediate stage delivers two in-phase driving currents for the n-p-n and p-n-p output transistor combinations.

The "bump" in the frequency characteristic due to the p-n-p output transistor combination is reduced by the parallel diode capacitor $C_{P1} = 9$ pF, the parallel diode Q_{130}, and the driver booster Q_{140}, Q_{141}.

The bias circuit is given in Fig. 7. It includes a proportional-to-absolute-temperature (PTAT) generator with the four transistors Q_{61}–Q_{64}. The transistors Q_{65}, Q_{66} and Q_{68}, Q_{69} provide a low output impedance at the bias lines V_{BCC} and V_{BCC}. The cascodes Q_{67} and Q_{70} reduce the supply-voltage sensitivity. The emitter resistor of Q_{61} can be partly short circuited by an external pin for bias adjustment. When short circuited its bias current is about 10 μA and the total supply current is 0.5 mA. In this situation the amplifier produces its normal characteristics. When open the bias current is about 2 μA and the total supply current is 0.1 mA. In that situation the characteristics such as output-current capability, bandwidth and slew rate are reduced by a factor of 3.

VII. Performance

The photomicrograph of the chip (Fig. 8) shows (left middle) a quad layout for both the n-p-n and p-n-p input pairs. The typical offset is only 0.3 mV. The offset change when crossing a voltage range of 100 mV between 0.75 and 0.85 V above the negative supply voltage is typically 0.1 mV. The total MOS capacitance on the chip is only 26 pF. On the right-hand side the 16× output p-n-p and the 8×

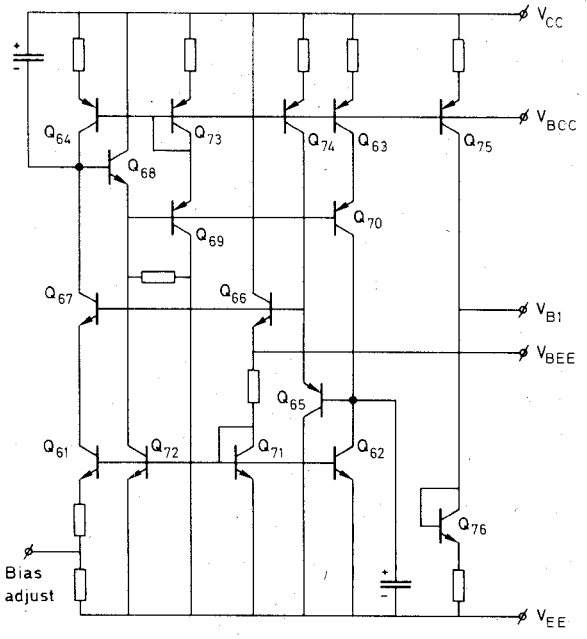

Fig. 7. Bias circuit.

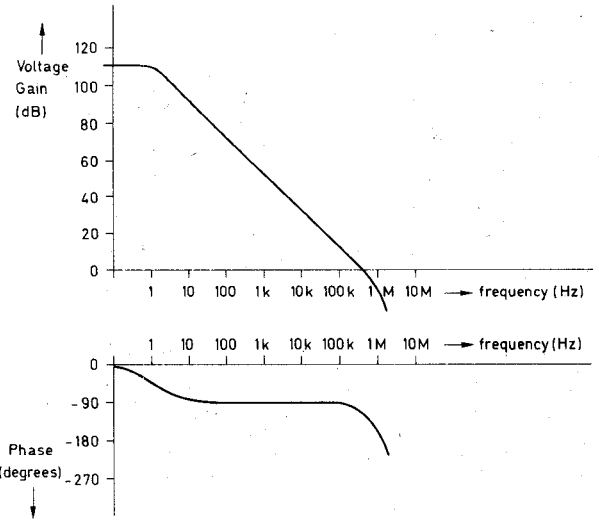

Fig. 8. Photomicrograph of the low-voltage operational amplifier chip (1.5×1.7 mm^2).

output n-p-n can be distinguished. The chip measures 1.5×1.7 mm^2.

The open-loop frequency and phase characteristics are shown in Fig. 9. The dc gain is 110 dB with a resistive load of 10 kΩ. The bandwidth is 0.6 MHz and the unity-gain phase margin is 79°.

The open-loop output impedance decreases from about 20 kΩ at 1 Hz to 1 Ω at 20 kHz. The unity-gain feedback output impedance is as low as 30 mΩ below 20 kHz. The op amp is stable with capacitive loads up to 1 nF.

Typical characteristics are listed in Table I. The slew rate is 0.25 V/μ s. The input referred noise spectral density at 5 kHz is 25 nV/Hz$^{1/2}$. The low-frequency CMRR measured with a rail-to-rail input voltage swing is 97 dB at a total supply voltage of 15 V and 85 dB at 1.8 V. The CMRR is 66 dB when the CM voltage is in the range between 0.6 and 0.8 V above the negative supply voltage.

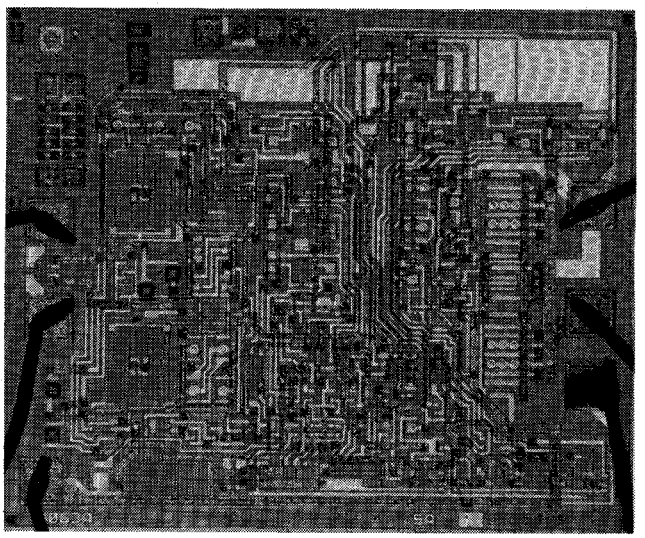

Fig. 9. Open-loop frequency and phase characteristics of the low-voltage operational amplifier with $V_{CC} - V_{EE} = 1.8$ V and $R_L = 10$ kΩ.

TABLE I
TYPICAL CHARACTERISTICS OF THE LOW-VOLTAGE OPERATIONAL AMPLIFIER AT A TOTAL SUPPLY VOLTAGE ($V_{CC} - V_{EE}$) BETWEEN 1.8 AND 15 V AND AT AN AMBIENT TEMPERATURE OF 25° C

parameter	symbol	value	units
Input offset voltage	V_{OS}	0.3	mV
Temperature coefficient of V_{OS}		4	μV/°C
Input offset current	I_{OS}	20	nA
Input bias currrent	I_B	40	nA
Common mode rejection ratio	CMRR		
rail-to-rail at (V_{CC} - V_{EE}) = 15V		97	dB
rail-to-rail at (Vcc - V_{EE}) = 1.8V		85	dB
between 0.6V and 0.8V above V_{EE}		66	dB
Common-mode range	V_{CM}	(V_{CC} + 0.2) to (V_{EE} - 0.2)	V
Large signal open-loop gain with R_L=10kΩ	A_{VOL}	300	V/mV
Output voltage swing Vout with R_L=10kΩ		(V_{CC} - 0.2) to (V_{EE} + 0.2)	V
Quiescent supply current			
bias pin to V_{EE}		0.5	mA
bias pin open		0.1	mA
Short-circuit output current	I_{SC}		
bias pin to V_{EE}		+20/-40	mA
bias pin open		+ 8/-15	mA
Open-loop output resistance	R_O		
freq. = 1 Hz		20k	Ω
freq. = 20kHz		1	Ω
Slew rate	SR		
bias pin to V_{EE}		0.25	V/μs
bias pin open		0.1	V/μs
Small-signal gain-bandwidth product			
bias pin to V_{EE}		0.6	MHz
bias pin open		0.2	MHz
Unity-gain phase margin with R_L = 10kΩ		70	Degrees
Input refered noise spectral density			
freq. = 5 kHz		25	nV/√Hz

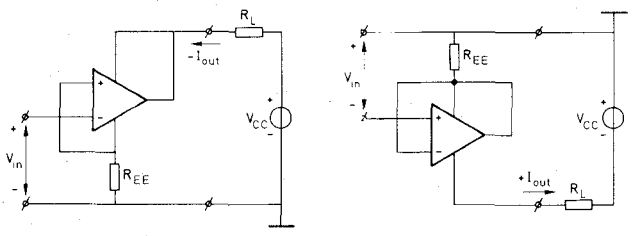

Fig. 10. (a) Voltage-to-current converter for negative currents. $I_{out} = V_{in}/R_{EE}$ with $-I_{out} > I_{BIAS\ SUPPLY}$. (b) Voltage-to-current converter for positive currents. $I_{out} = V_{in}/R_{EE}$ with $I_{out} > I_{BIAS\ SUPPLY}$.

A typical application of the rail-to-rail input common-mode range is that the low-voltage op amp can be connected as a self-contained voltage-to-current converter for either negative output currents (Fig. 10(a)) or positive currents (Fig. 10(b)). In Fig. 10(a) the differential input of the op amp equates the input voltage and the voltage across the current-measuring resistor R_{EE}. The negative supply terminal controls the current through R_{EE}. The output and positive supply terminals collect the current through R_{EE} and deliver it to the output load. The negative output current equals

$$-I_{out} = V_{in}/R_{EE}. \tag{10}$$

The converter in Fig. 10(b) performs the same function for positive currents. The lower threshold of the output current is set by the amplifier bias current. The converter can be used in combination with sensors to obtain a two-wire supply-voltage-independent current signal.

VIII. Conclusion

The design goal of integrating a low-voltage operational amplifier which can perform precision signal operations on nearly the full supply voltage range has been achieved. The usable signal range is about 0.2 V lower than the supply-rail voltages and is only limited by the saturation voltage of the output transistors. The lowest total supply voltage is 1.5 V at 20 °C. At that voltage the input stage still has a constant transconductance over the full supply voltage range and the output transistors can deliver the full output current. The highest supply voltage in the present process is 18 V. Qualities such as output current capability, bandwidth, and slew rate largely depend on the lateral p-n-p output transistor. When using an integration process which allows better p-n-p's these qualities can strongly be improved.

Acknowledgment

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Johan H. Huijsing (SM'81) was born in Bandung, Indonesia on May 21, 1938. He received the ingenieurs (M.S.) degree in electrical engineering from Delft University of Technology, Delft, The Netherlands, in 1969, and the Ph.D. degree from the same university in 1981 for work on operational amplifiers.

Since 1969 he has been a member of the research and teaching staff of the Electronic Instrumentation Laboratory, Department of Electrical Engineering, Delft University of Technology. His interest is in research on analog integrated circuits and integrated sensors for instrumentation systems.

Daniel Linebarger (S'82–M'77) was born in Mount Shasta, CA on October 1, 1958. He received the B.S.E.L. degree from California Polytechnic State University, San Luis Obispo, CA, in 1982.

He joined Signetics Linear Division, Sunnyvale, CA, in 1982, where he is currently involved in the design and development of analog integrated circuits.