

## 14.0 TIMER3 MODULE

The Timer3 module timer/counter incorporates these features:

- Software selectable operation as a 16-bit timer or counter
- Readable and writable 8-bit registers (TMR3H and TMR3L)
- Selectable clock source (internal or external) with device clock or Timer1 oscillator internal options
- Interrupt on overflow
- Module Reset on CCP Special Event Trigger

A simplified block diagram of the Timer3 module is shown in Figure 14-1. A block diagram of the module's operation in Read/Write mode is shown in Figure 14-2.

The Timer3 module is controlled through the T3CON register (Register 14-1). It also selects the clock source options for the CCP modules (see **Section 15.1.1 “CCP Modules and Timer Resources”** for more information).

**REGISTER 14-1: T3CON: TIMER3 CONTROL REGISTER**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
RD16	T3CCP2	T3CKPS1	T3CKPS0	T3CCP1	$\overline{\text{T3SYNC}}$	TMR3CS	TMR3ON
bit 7							bit 0

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7	<b>RD16:</b> 16-Bit Read/Write Mode Enable bit 1 = Enables register read/write of Timer3 in one 16-bit operation 0 = Enables register read/write of Timer3 in two 8-bit operations
bit 6, 3	<b>T3CCP2:T3CCP1:</b> Timer3 and Timer1 to CCPx Enable bits 1x = Timer3 is the capture/compare clock source for both CCP modules 01 = Timer3 is the capture/compare clock source for CCP2; Timer1 is the capture/compare clock source for CCP1 00 = Timer1 is the capture/compare clock source for both CCP modules
bit 5-4	<b>T3CKPS1:T3CKPS0:</b> Timer3 Input Clock Prescale Select bits 11 = 1:8 Prescale value 10 = 1:4 Prescale value 01 = 1:2 Prescale value 00 = 1:1 Prescale value
bit 2	<b><math>\overline{\text{T3SYNC}}</math>:</b> Timer3 External Clock Input Synchronization Control bit (Not usable if the device clock comes from Timer1/Timer3.) <u>When TMR3CS = 1:</u> 1 = Do not synchronize external clock input 0 = Synchronize external clock input <u>When TMR3CS = 0:</u> This bit is ignored. Timer3 uses the internal clock when TMR3CS = 0.
bit 1	<b>TMR3CS:</b> Timer3 Clock Source Select bit 1 = External clock input from Timer1 oscillator or T13CKI (on the rising edge after the first falling edge) 0 = Internal clock (Fosc/4)
bit 0	<b>TMR3ON:</b> Timer3 On bit 1 = Enables Timer3 0 = Stops Timer3