Faculty of Engineering.

Autonomous University of Querétaro

Career: Automation Engineer.

Subject: Systems with reconfigurable logic.

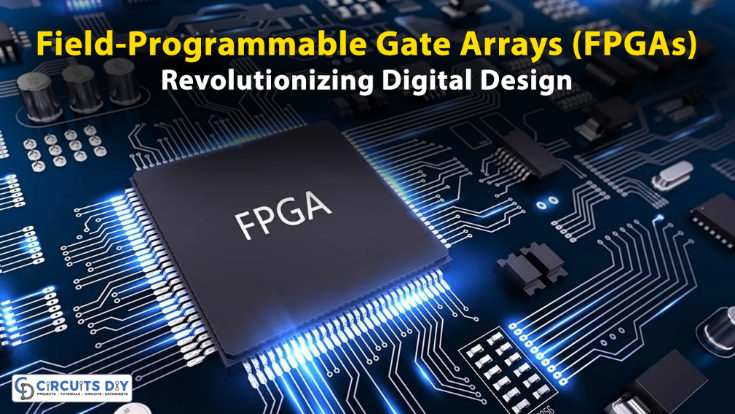
Student: Martínez Murillo Omar Yarif.

Student: Diego Joel Zúñiga Fragoso.

Student: Daniela del Carmen Manríquez Navarro.

Student: Joselyn Gallegos Abreo.

Practice 3: Switch case,IF,When



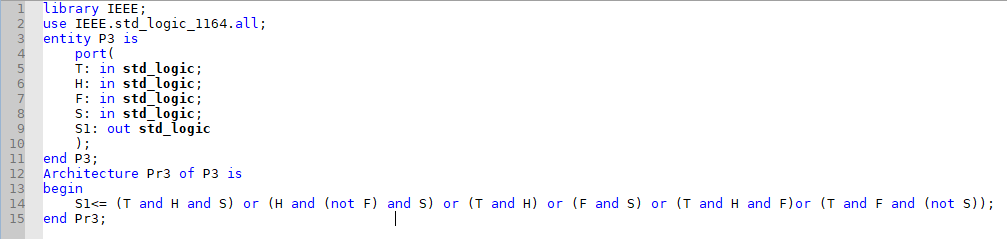


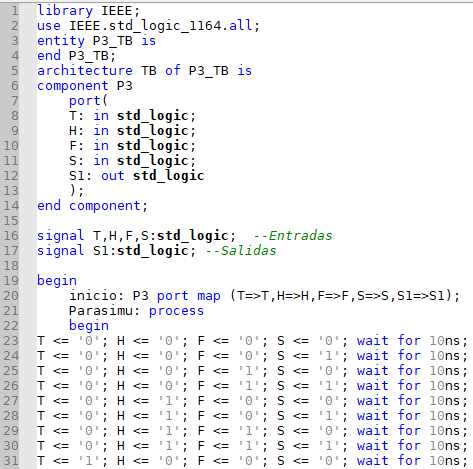
**Introduction**

The practice is divided into three parts. The first part involves the use of Karnaugh maps, where the task is to design a system for monitoring environmental conditions. A truth table is generated, and the Karnaugh map is used to obtain the most simplified equation for the Boolean operations. The second part focuses on the use of the switch-case statement in VHDL. Here, the goal is to display the alphabet on an FPGA by creating a truth table, performing a simulation, and then programming it. Lastly, the practice covers the use of the if statement in VHDL to display words, again creating a truth table, performing a simulation, and then programming it.

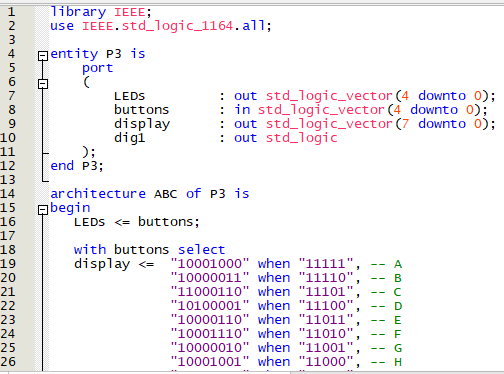
**Methodology**

* First, we create the Karnaugh map based on the truth table derived from the given conditions.
* Second, the equation is extracted, and the base code is programmed in Aldec-Active-VHDL.



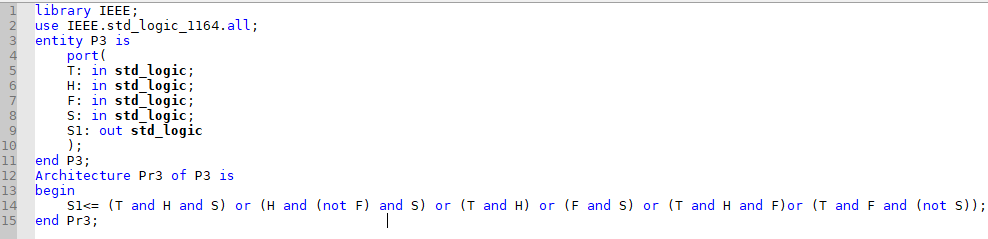
* Third, a testbench is created for simulation.
* Fourth, a truth table is created for the switch-case code, where specific combinations are defined to represent letters of the alphabet.

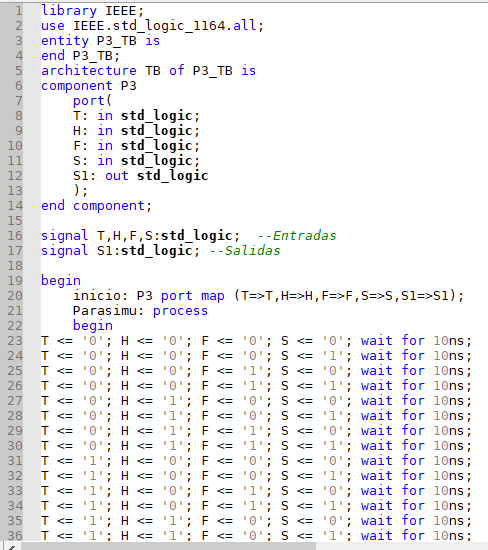


* Fifth, the configuration is set up in Aldec-Active-VHDL, followed by simulation.
* Sixth, the configuration is transferred to Quartus, and the pins are assigned.
* Seventh, the program is loaded onto the FPGA.
* Eighth, a truth table is created for the if statement, which should display 4-letter words.
* Ninth, the configuration is set up in Aldec-Active-VHDL, followed by simulation.
* Tenth, the configuration is transferred to Quartus, and the pins are assigned.
* Eleventh, the program is loaded onto the FPGA.

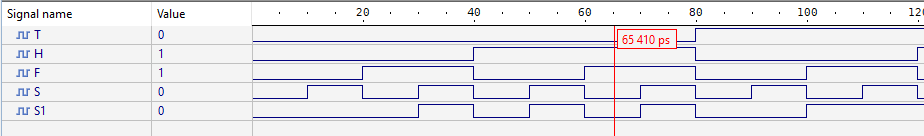
**Results**

Base algorithm Karnaugh

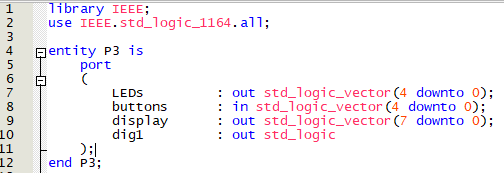


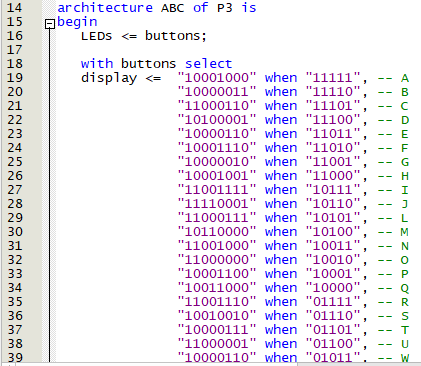
Test Bench

Simulation

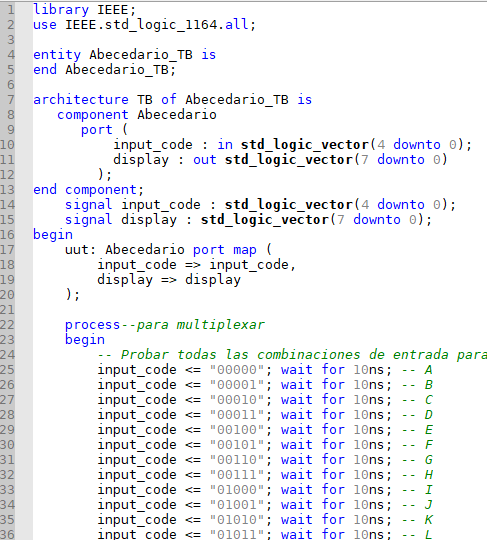


Base algorithm of Switch

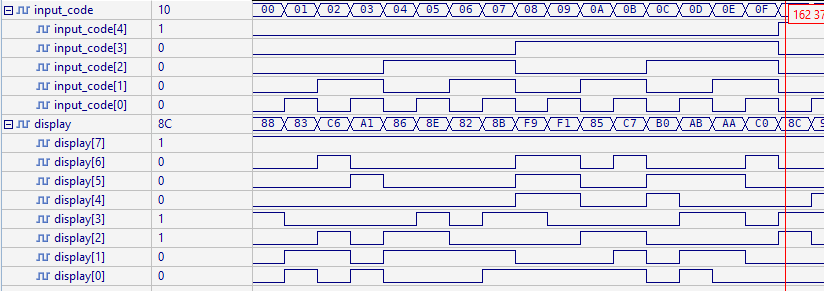




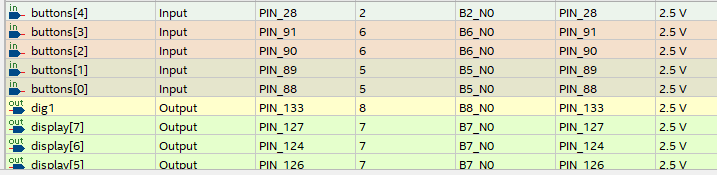
Test Bench



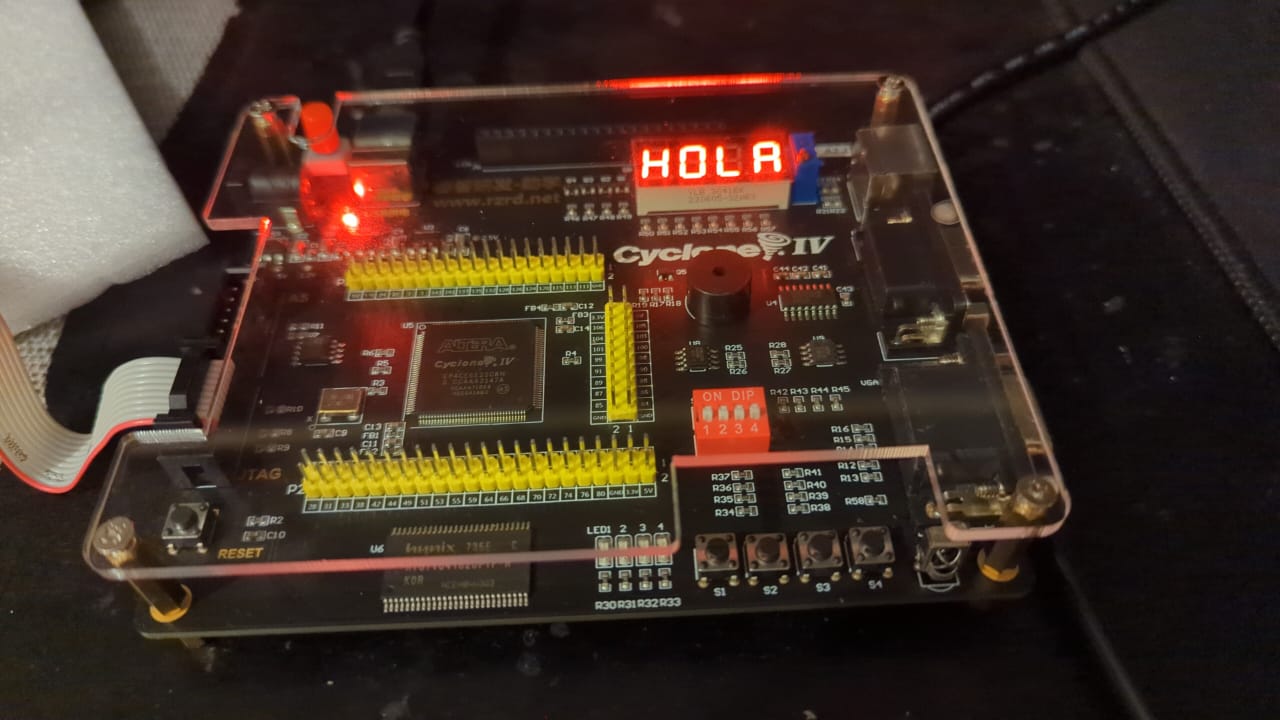
Simulation



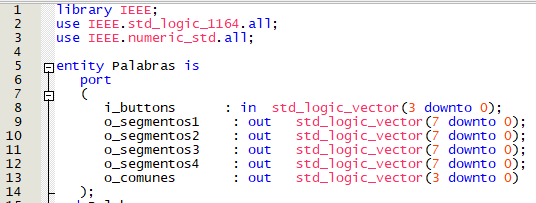
Asigned PIN’s of Switch

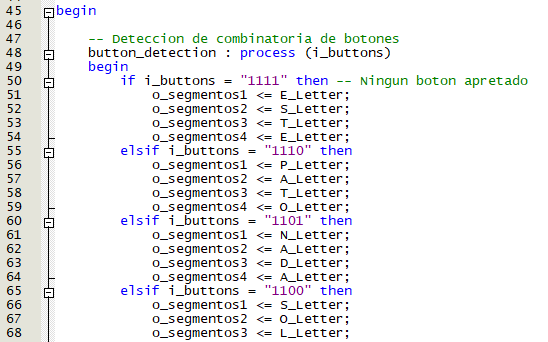


Hardware images

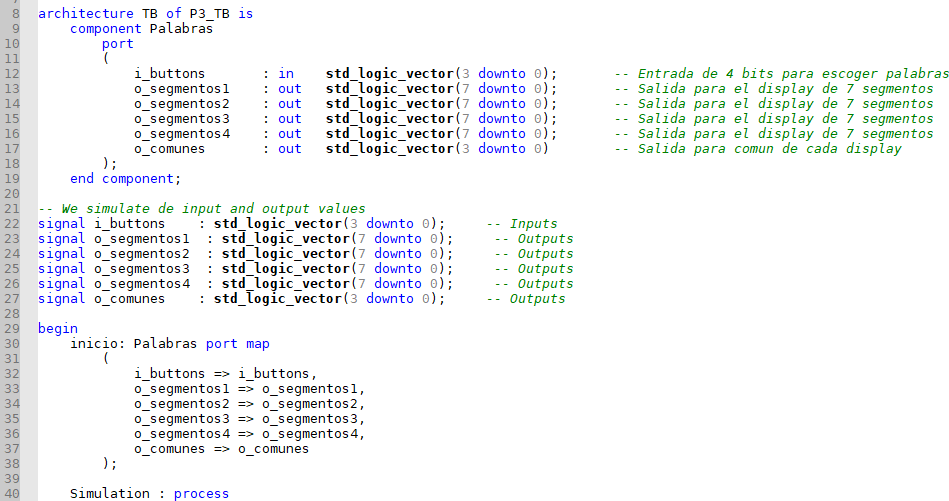


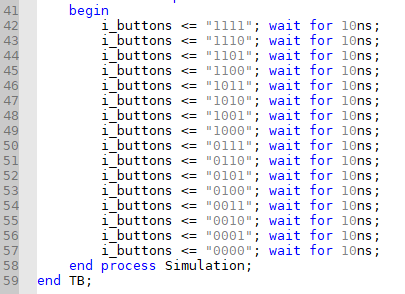
Base algorithm of IF





Test Bench





Truth table

Imagen que contiene Texto

Descripción generada automáticamente

Hardware images

Un circuito electrónico

Descripción generada automáticamente con confianza media

**Conclusión**

Throughout the practice, we successfully represented letters on a 7-segment display, configuring each letter through a combination of 5 inputs. Additionally, we gained experience using the Quartus software, which allowed us to become more familiar with VHDL and its selective structures, such as `IF` and `SWITCH`. We also learned to use the `process` block to generate sequential actions, such as multiplexing the displays. This practice gave us a deeper understanding of VHDL programming and the control of displays through combinational and sequential logic.