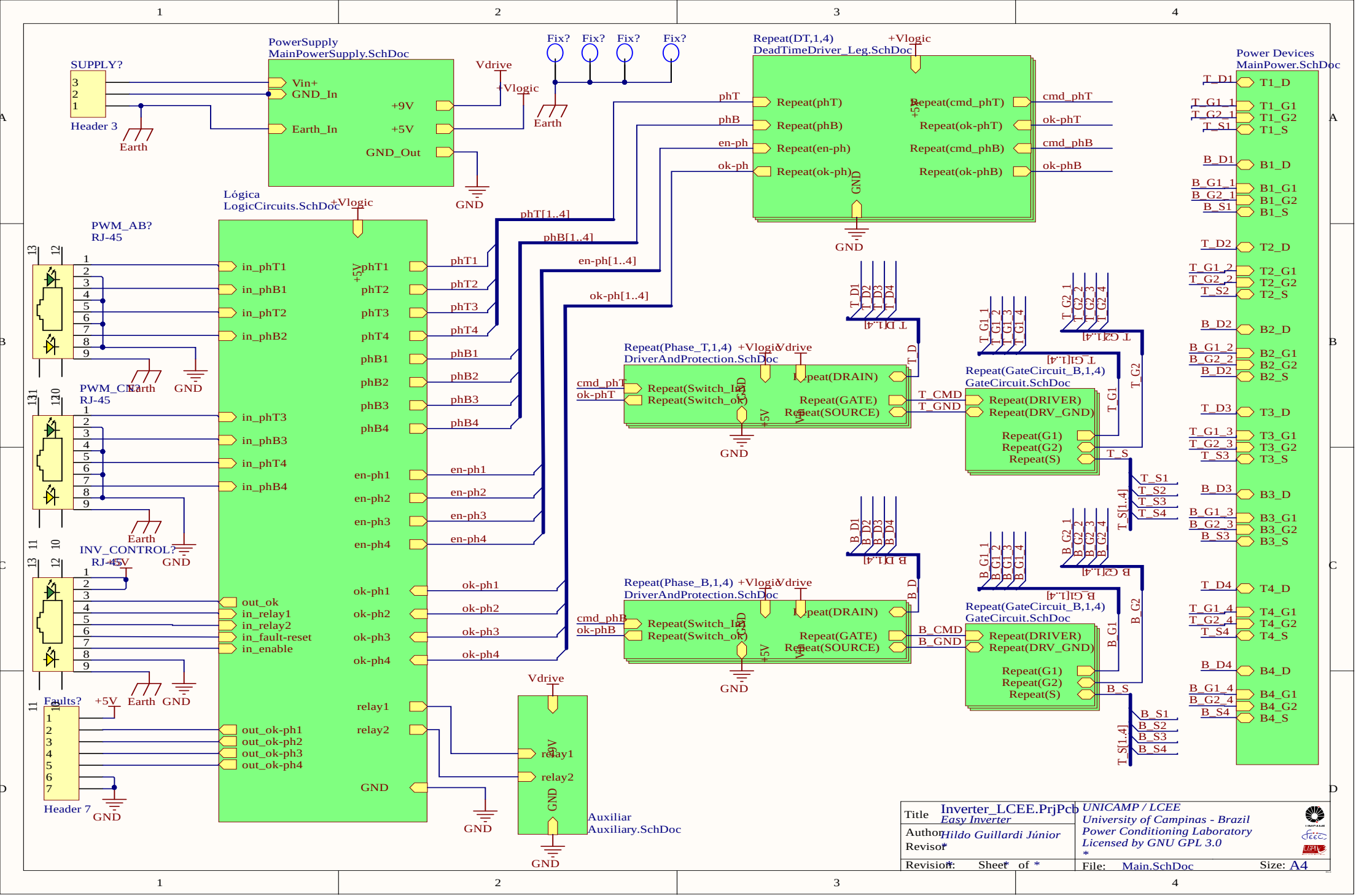
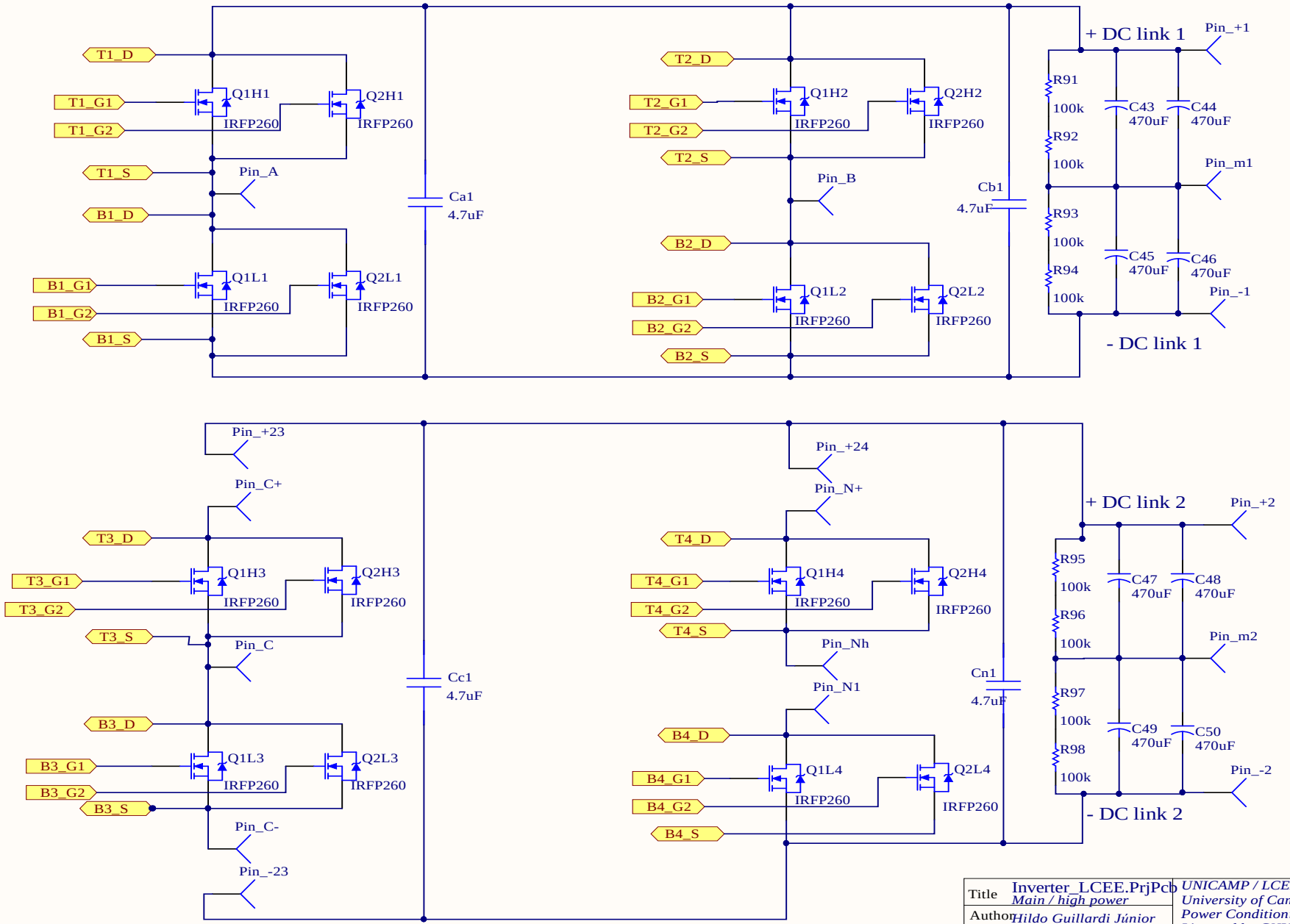
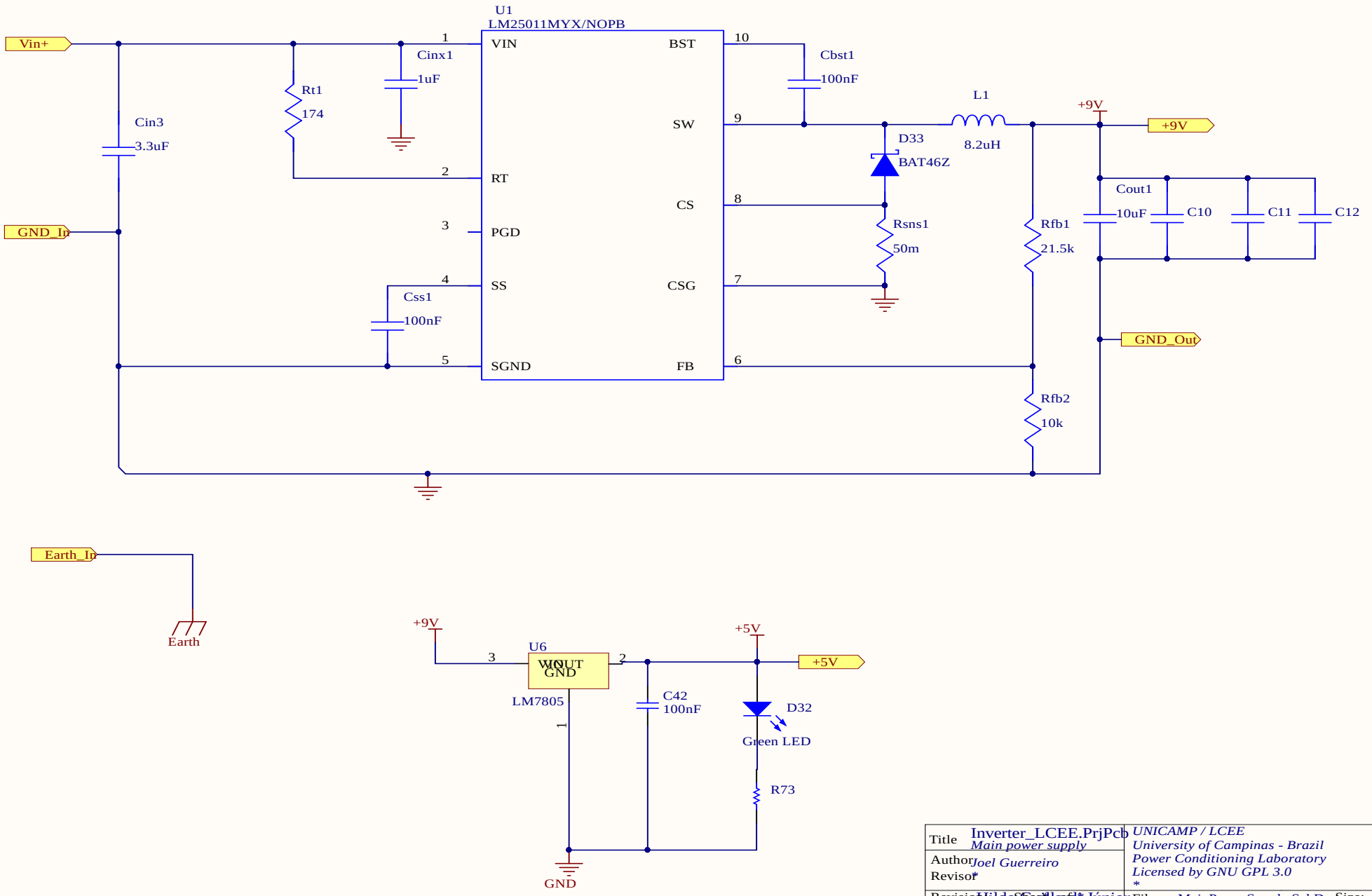

SUPPLY?
Header 3
Earth
PowerSupply
MainPowerSupply.SchDoc
Vin+
GND_In
Earth_In
+9V
+5V
GND_Out
Vdrive
+Vlogic
Fix?
Earth
GND
Repeat(DT,1,4)
DeadTimeDriver_Leg.SchDoc
+Vlogic
phT
phB
en-ph
ok-ph
Repeat(phT)
Repeat(phB)
Repeat(en-ph)
Repeat(ok-ph)
Repeat(cmd_phT)
Repeat(ok-phT)
Repeat(cmd_phB)
Repeat(ok-phB)
cmd_phT
ok-phT
cmd_phB
ok-phB
Power Devices
MainPower.SchDoc
T1_D
T1_G1
T1_G2
T1_S
B1_D
B1_G1
B1_G2
B1_S
T2_D
T2_G1
T2_G2
T2_S
B2_D
B2_G1
B2_G2
B2_S
T3_D
T3_G1
T3_G2
T3_S
B3_D
B3_G1
B3_G2
B3_S
T4_D
T4_G1
T4_G2
T4_S
B4_D
B4_G1
B4_G2
B4_S
Lógica
LogicCircuits.SchDoc
PWM_AB?
RJ-45
PWM_CD?
RJ-45
INV_CONTROL?
RJ-45
Faults?
Header 7
in_phT1
in_phB1
in_phT2
in_phB2
in_phT3
in_phB3
in_phT4
in_phB4
out_ok
in_relay1
in_relay2
in_fault-reset
in_enable
out_ok-ph1
out_ok-ph2
out_ok-ph3
out_ok-ph4
phT1
phT2
phT3
phT4
phB1
phB2
phB3
phB4
en-ph1
en-ph2
en-ph3
en-ph4
ok-ph1
ok-ph2
ok-ph3
ok-ph4
relay1
relay2
phT[1..4]
phB[1..4]
en-ph[1..4]
ok-ph[1..4]
Repeat(Phase_T,1,4)
DriverAndProtection.SchDoc
Repeat(Switch_In)
Repeat(Switch_ok)
Repeat(DRAIN)
Repeat(GATE)
Repeat(SOURCE)
Repeat(GateCircuit_B,1,4)
GateCircuit.SchDoc
Repeat(DRIVER)
Repeat(DRV_GND)
Repeat(G1)
Repeat(G2)
Repeat(S)
T_CMD
T_GND
T_G1
T_G2
T_S
T_S[1..4]
Repeat(Phase_B,1,4)
DriverAndProtection.SchDoc
B_CMD
B_GND
B_G1
B_G2
B_S
B_S[1..4]
Auxiliar
Auxiliary.SchDoc
Title
Inverter_LCEE.PrjPcb
Easy Inverter
Author
Hildo Guillardi Júnior
Revision
UNICAMP / LCEE
University of Campinas - Brazil
Power Conditioning Laboratory
Licensed by GNU GPL 3.0
File: Main.SchDoc
Size: A4
Sheet * of *



Title	Inverter_LCEE.PrjPcb *Main / high power*	*UNICAMP / LCEE* *University of Campinas - Brazil* *Power Conditioning Laboratory* *Licensed by GNU GPL 3.0* *	
Author	*Hildo Guillardi Júnior*		
Revisor	*		
Revision: *	Sheet * of *	File: MainPower.SchDoc	Size: A4

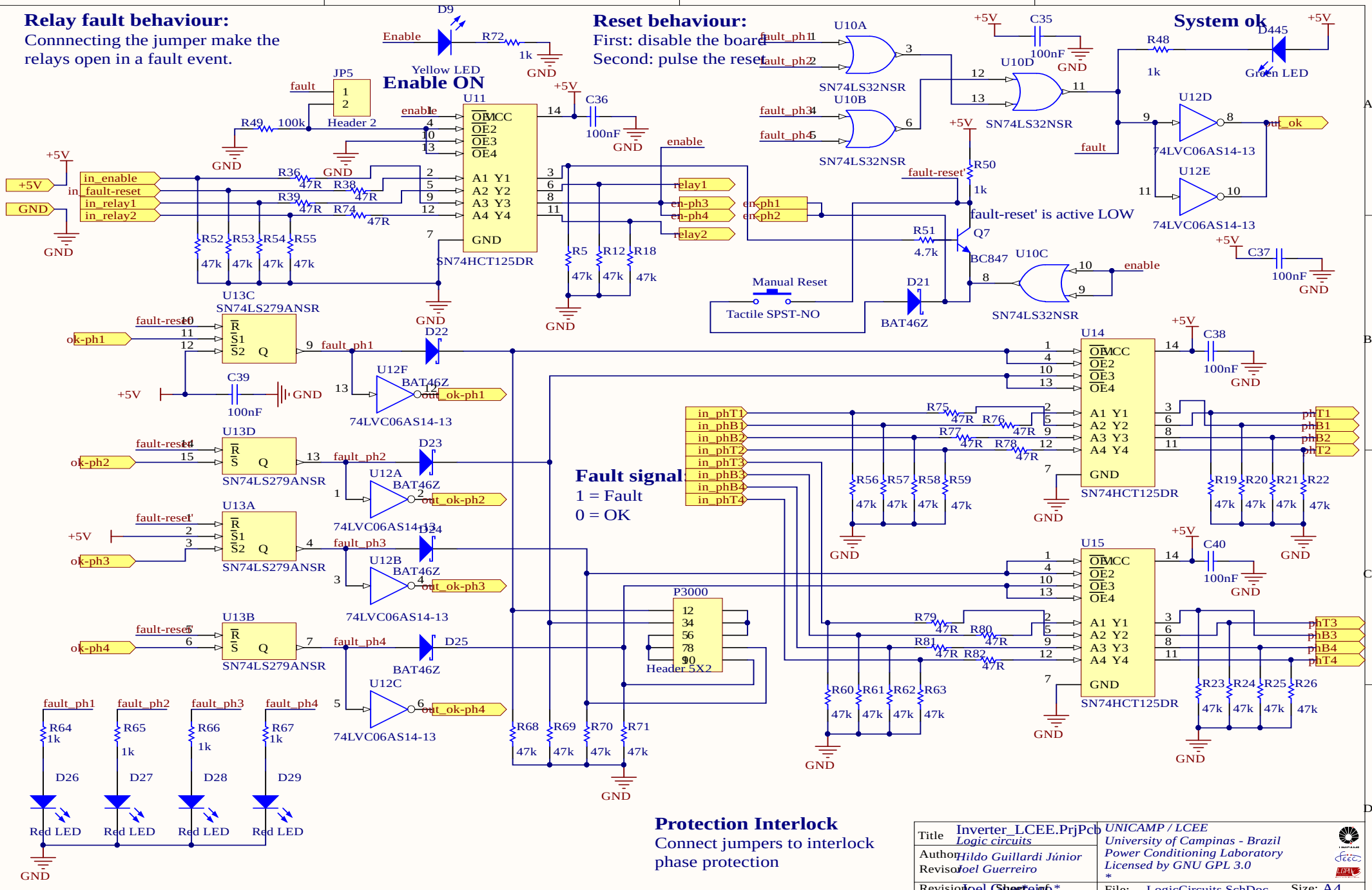


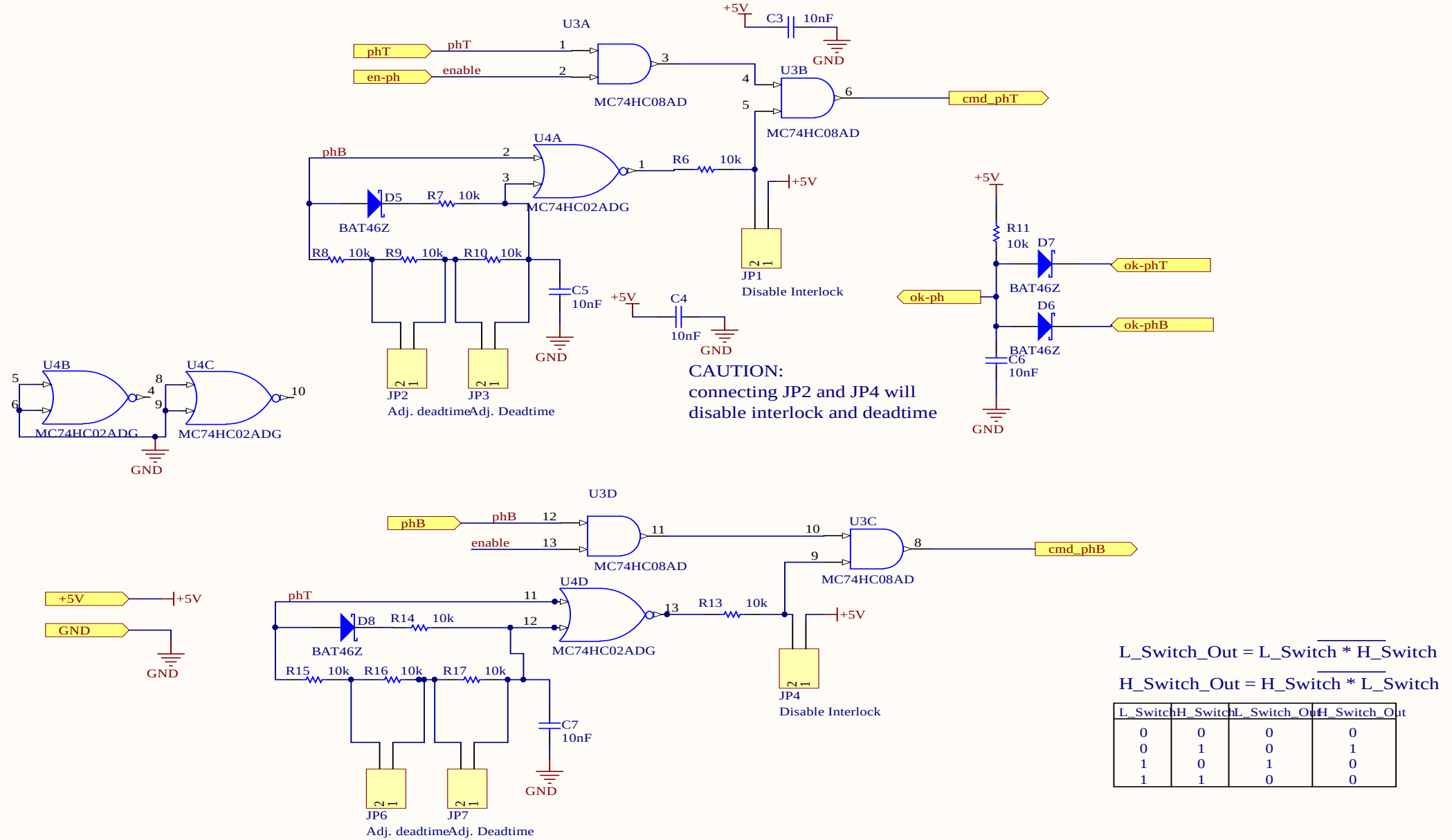
Title	Inverter_LCEE.PrjPcb *Main power supply*
Author	*Joel Guerreiro*
Revisor	*
Revision	Scale: *

UNICAMP / LCEE
University of Campinas - Brazil
Power Conditioning Laboratory
Licensed by GNU GPL 3.0
*

Hildo Guillardi Júnior

File: MainPowerSupply.SchDoc Size: A4


Relay fault behaviour:
Connnecting the jumper make the relays open in a fault event.
Reset behaviour:
First: disable the board
Second: pulse the reset
System ok
Enable ON
fault-reset' is active LOW
Fault signal:
1 = Fault
0 = OK
Protection Interlock
Connect jumpers to interlock phase protection
Yellow LED
Green LED
Red LED
Manual Reset
Tactile SPST-NO
SN74LS32NSR
SN74HCT125DR
SN74LS279ANSR
74LVC06AS14-13
BAT46Z
BC847
Header 2
Header 5X2
Inverter_LCEE.PrjPcb
Logic circuits
Hildo Guillardi Júnior
Joel Guerreiro
UNICAMP / LCEE
University of Campinas - Brazil
Power Conditioning Laboratory
Licensed by GNU GPL 3.0
LogicCircuits.SchDoc
Size: A4

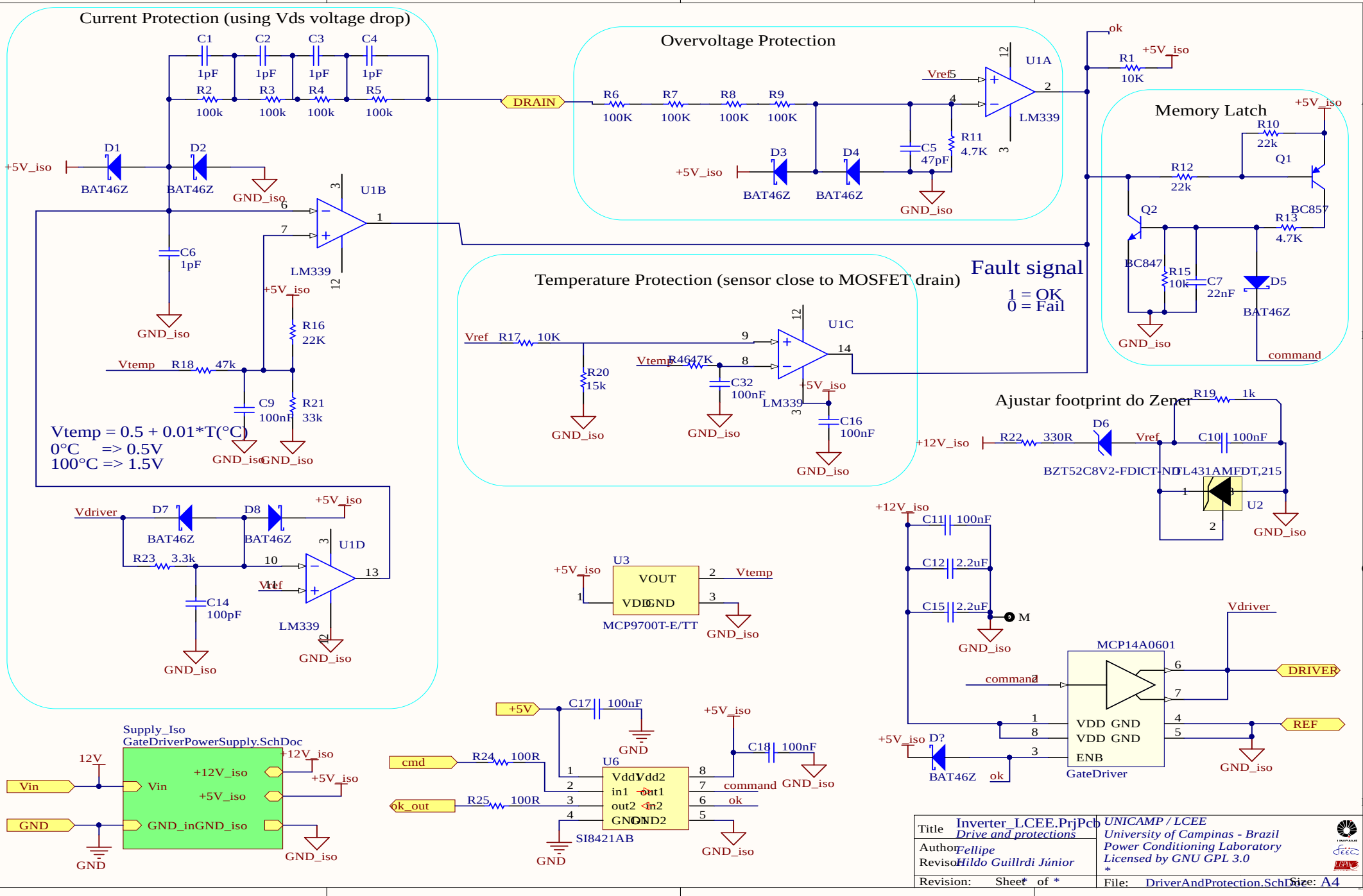


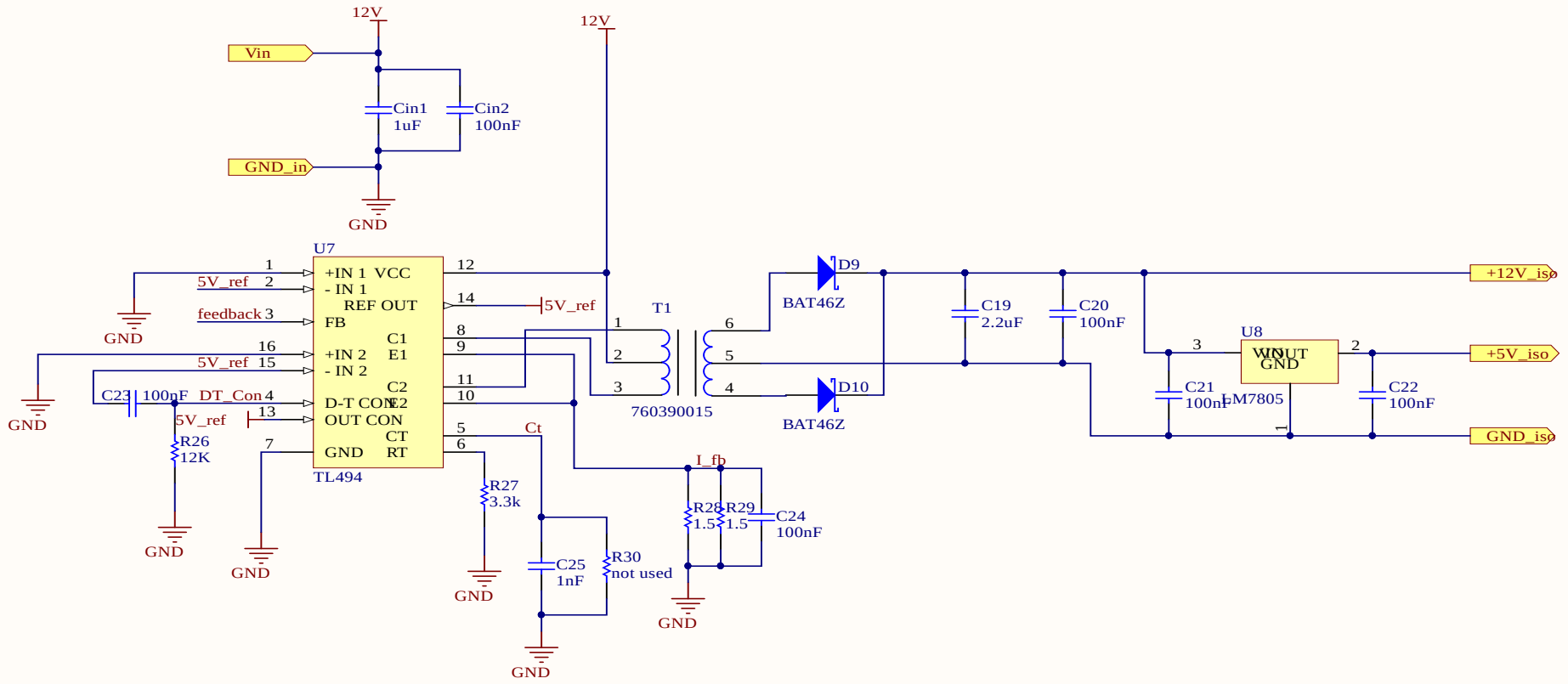
$$L\_Switch\_Out = L\_Switch * \overline{H\_Switch}$$

$$H\_Switch\_Out = H\_Switch * \overline{L\_Switch}$$

L_Switch	H_Switch	L_Switch_Out	H_Switch_Out
0	0	0	0
0	1	0	1
1	0	1	0
1	1	0	0

Title	Inverter_LCEE.PrjPcb *Dead time & interlock*	*UNICAMP / LCEE* *University of Campinas - Brazil* *Power Conditioning Laboratory* *Licensed by GNU GPL 3.0* *
Author	*Fellipe*	
Revison	*Hildo / Joel*	
Revision: *	Sheet * of *	File: DeadTimeDriver_Leg.SchDoc Size: A4


Current Protection (using Vds voltage drop)
C1 1pF
C2 1pF
C3 1pF
C4 1pF
R2 100k
R3 100k
R4 100k
R5 100k
DRAIN
D1 BAT46Z
D2 BAT46Z
+5V_iso
GND_iso
U1B
LM339
C6 1pF
R16 22K
Vtemp
R18 47k
C9 100nF
R21 33k
Vtemp = 0.5 + 0.01*T(°C)
0°C => 0.5V
100°C => 1.5V
Vdriver
D7 BAT46Z
D8 BAT46Z
U1D
R23 3.3k
C14 100pF
Vref
Overvoltage Protection
R6 100K
R7 100K
R8 100K
R9 100K
U1A
LM339
R11 4.7K
C5 47pF
D3 BAT46Z
D4 BAT46Z
ok
R1 10K
Temperature Protection (sensor close to MOSFET drain)
Vref R17 10K
R20 15k
Vtemp R4647K
C32 100nF
U1C
C16 100nF
Fault signal
1 = OK
0 = Fail
Memory Latch
R10 22k
Q1
R12 22k
Q2
BC857
R13 4.7K
BC847
R15 10k
C7 22nF
D5 BAT46Z
command
Ajustar footprint do Zener
R19 1k
D6
R22 330R
+12V_iso
BZT52C8V2-FDICT-ND
TL431AMFDT,215
U2
C10 100nF
U3
VOUT
VDD GND
MCP9700T-E/TT
Vtemp
C11 100nF
C12 2.2uF
C15 2.2uF
MCP14A0601
command
DRIVER
REF
VDD GND
VDD GND
ENB
GateDriver
D? BAT46Z
ok
Supply_Iso
GateDriverPowerSupply.SchDoc
12V
Vin
GND
+12V_iso
+5V_iso
GND_inGND_iso
+5V
C17 100nF
C18 100nF
cmd
R24 100R
ok_out
R25 100R
U6
Vdd1 Vdd2
in1 out1
out2 in2
GND1 GND2
SI8421AB
Title Inverter_LCEE.PrjPcb
Drive and protections
Author Fellipe
Revison Hildo Guillrdi Júnior
Revision: Sheet * of *
UNICAMP / LCEE
University of Campinas - Brazil
Power Conditioning Laboratory
Licensed by GNU GPL 3.0
*
File: DriverAndProtection.SchDoc
Size: A4

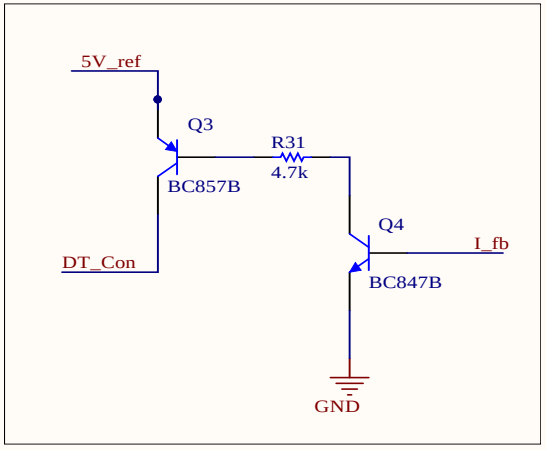


Switching frequency: 300kHz
Max. duty cycle: 45%
Input voltage: 8V
Output voltage: 12.5V

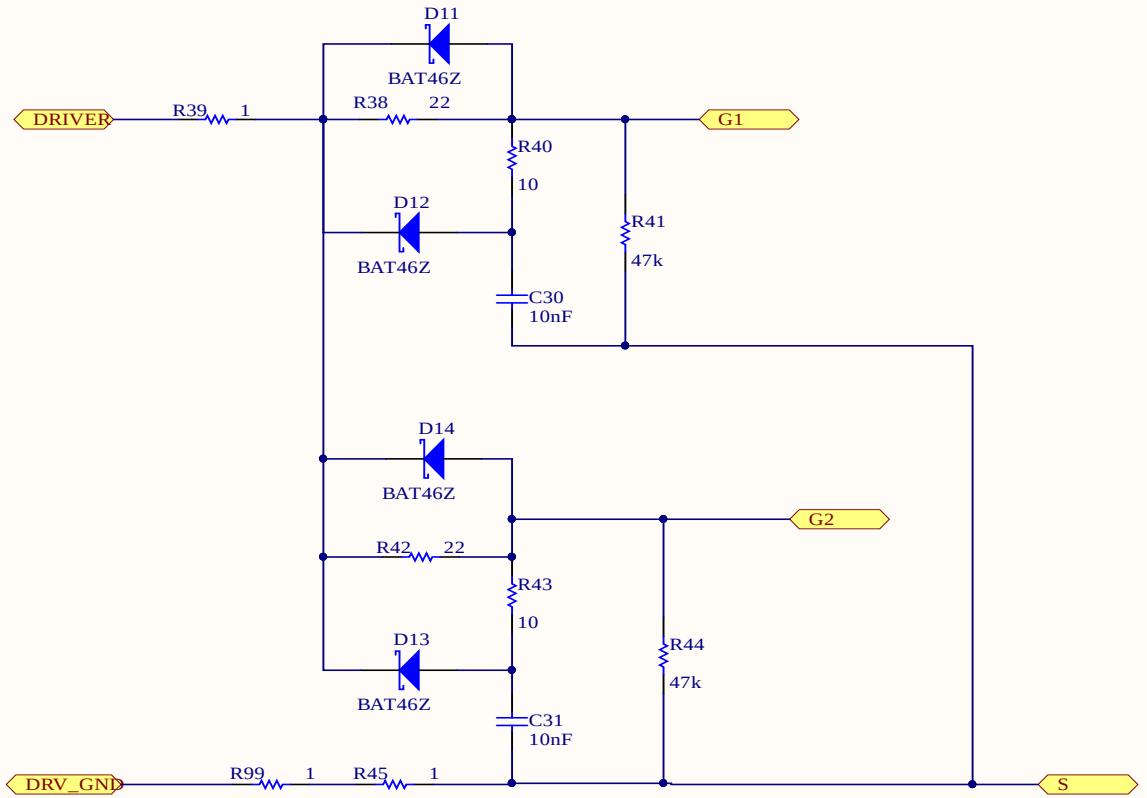
SMPS Controller:
TL494IDR
Alt. part: TL594CDR2G

Push-pull transformer:
Wurth Electronics
760390015

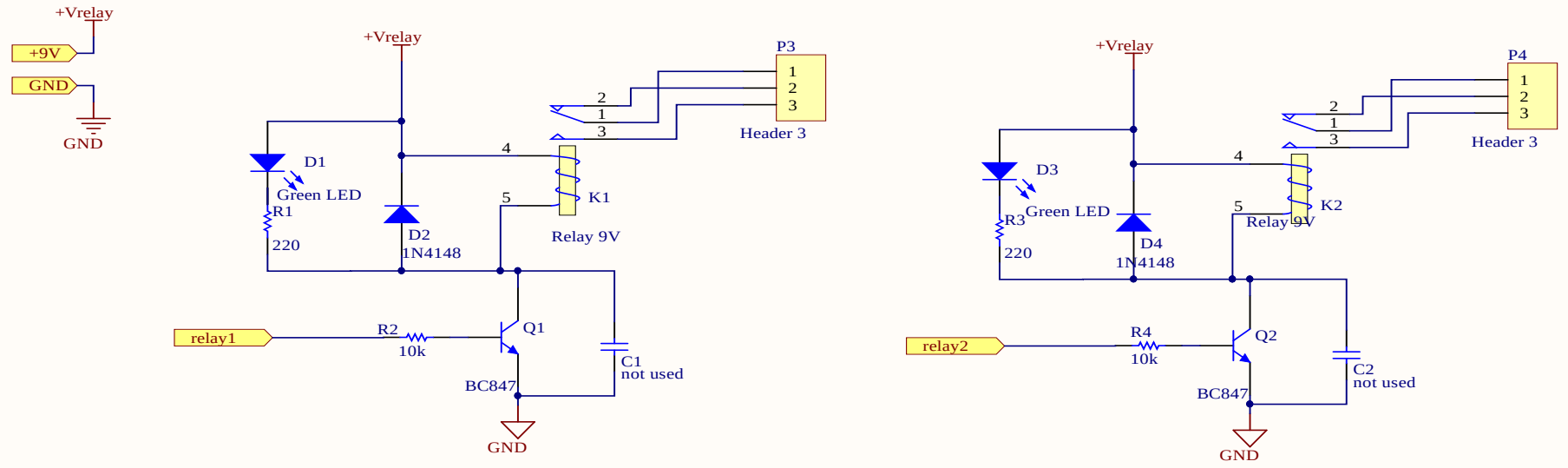
Current limit circuit



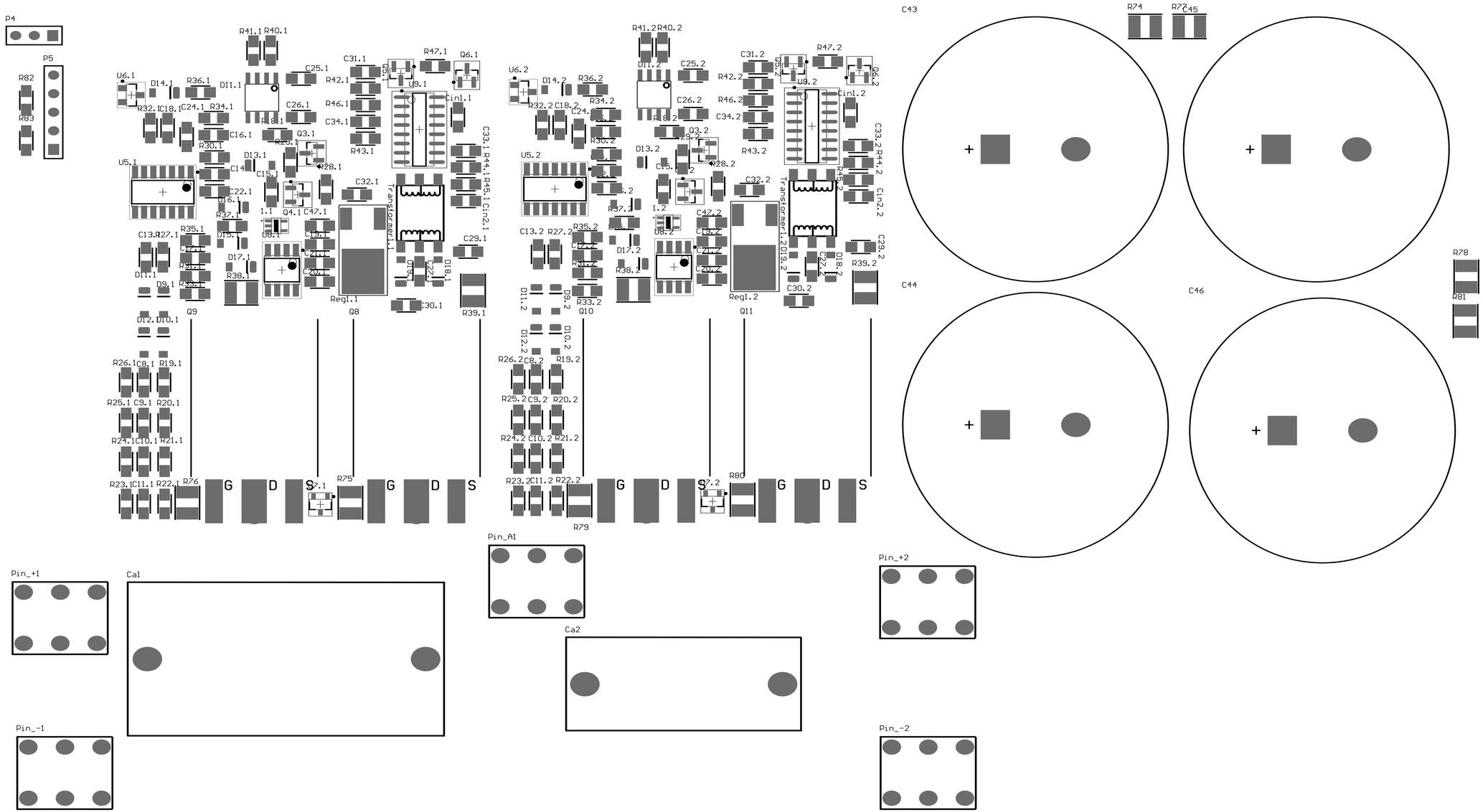
Title	Inverter_LCEE.PrjPcb *Isolated power supply*	*UNICAMP / LCEE* *University of Campinas - Brazil* *Power Conditioning Laboratory* *Licensed by GNU GPL 3.0* *	
Author	*Fellipe / Arthur*		
Revision	*Hildo / Joel*		
Revision: *	Sheet * of *	File: GateDriverPowerSupply.SchDoc	Size: A4



Title	Inverter_LCEE.PrjPcb *Gate drive circuit*	*UNICAMP / LCEE* *University of Campinas - Brazil* *Power Conditioning Laboratory* *Licensed by GNU GPL 3.0* *	
Author	*Hildo Guillardi Júnior*		
Revisor	*		
Revision: *	Sheet * of *	File: GateCircuit.SchDoc	Size: A4



Title	Inverter_LCEE.PrjPcb *Relays & auxiliary circuits*	*UNICAMP / LCEE* *University of Campinas - Brazil* *Power Conditioning Laboratory*
Author	*Hildo Guillardi Júnior*	*Licensed by GNU GPL 3.0*
Revison	*Fellipe*	*
Revision: *	Sheet * of *	File: Auxiliary.SchDoc Size: A4


P4
P5
R82
R83
U6.1
U5.1
U9.1
Cin1.1
Transformer1.1
Reg1.1
Q9
Q8
Q7.1
R76
R75
R41.1
R40.1
R47.1
Q6.1
C31.1
C25.1
R42.1
R46.1
C34.1
R43.1
C33.1
R44.1
R45.1
Cin2.1
C32.1
C29.1
C30.1
R39.1
U6.2
U5.2
U9.2
Cin1.2
Transformer1.2
Reg1.2
Q10
Q11
Q7.2
R80
R79
R41.2
R40.2
R47.2
Q6.2
C31.2
C25.2
R42.2
R46.2
C34.2
R43.2
C33.2
R44.2
R45.2
Cin2.2
C32.2
C29.2
C30.2
R39.2
R78
R81
C43
C44
C45
C46
R74
R77
Pin_A1
Pin_+1
Pin_-1
Pin_+2
Pin_-2
Ca1
Ca2