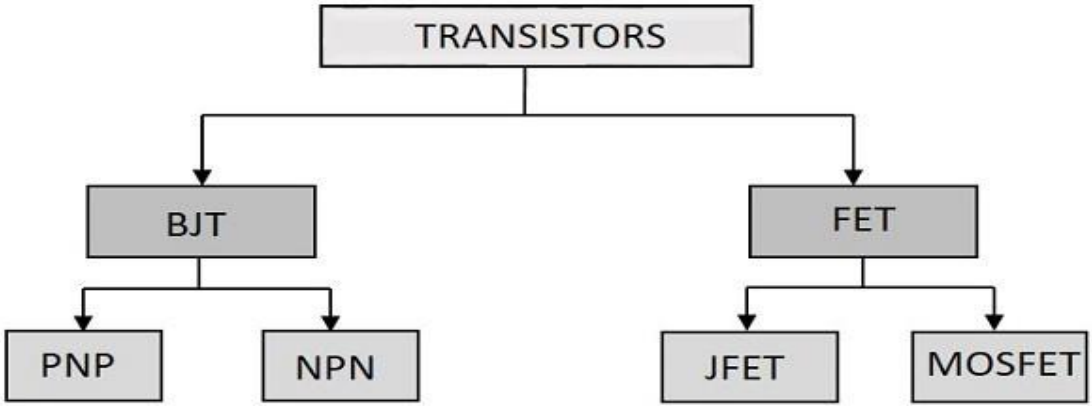
**TRANSISTORS (BJT AND FET)**

Transistor= trans+istor.

Transfers the resistance from low resistance region to high resistance region. There are two types of transistors in use.




The primary transistor is the BJT and FET is the modern version of transistor.

**BJTs (BIPOLAR JUNCTION TRANSISTORS):**

The transistor formed by back to back connection of two diodes.

**Bipolar Junction Transistors:** The operation of the transistor depends on both majority and minority carriers. BJT is a current controlled device. That means output current ($I_C$) is controlled by input current ( $I_B$). The voltage between two terminals controls the current through the third terminal. So it is called current controlled device.

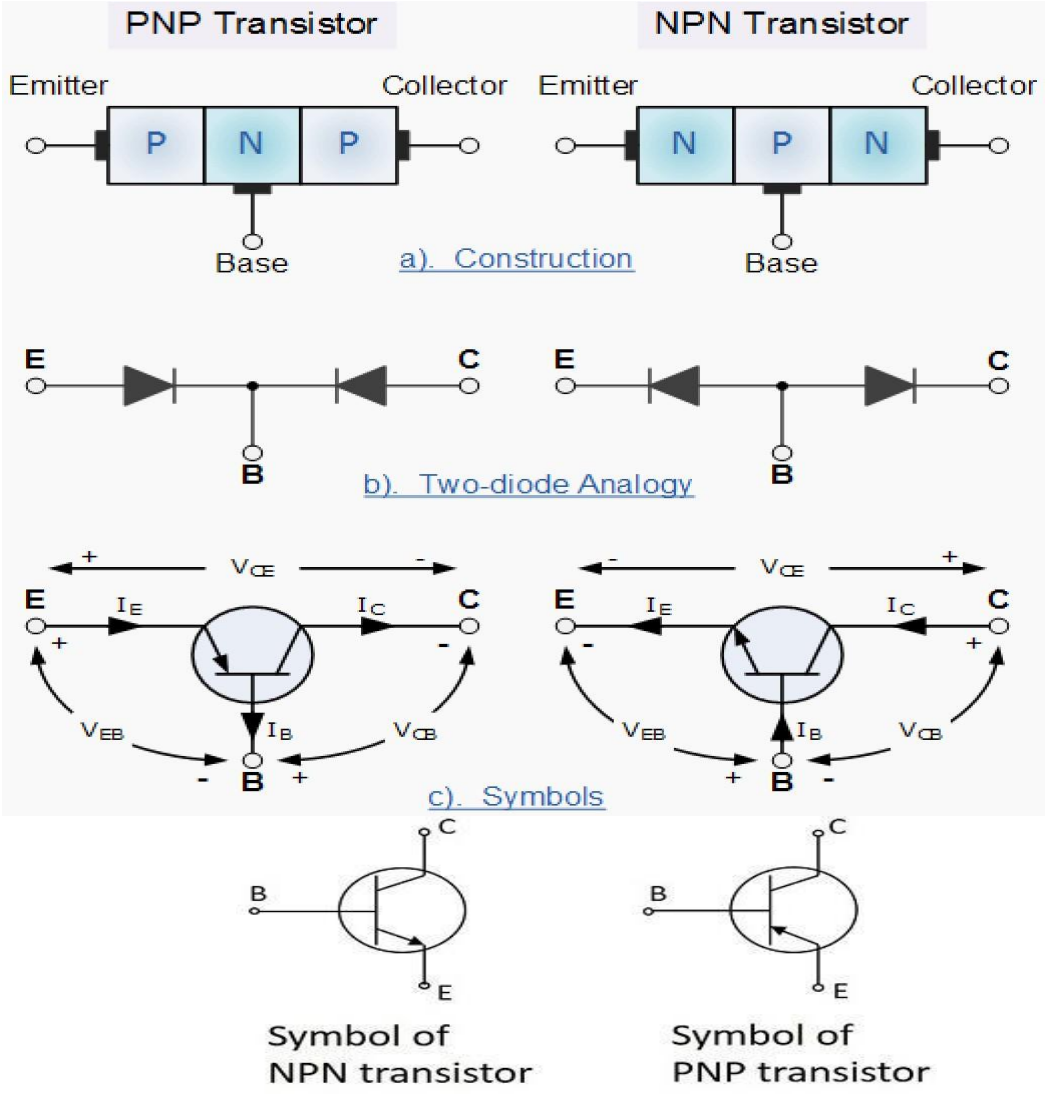
**CONSTRUCTION OF BJT AND ITS SYMBOLS:**

The **Bipolar Transistor** basic construction consists of two PN-junctions producing three connecting terminals with each terminal being given a name to identify it from the other two. These three terminals are known and labelled as the Emitter ( E ), the Base ( B ) and the Collector ( C ) respectively.

There are two basic types of bipolar transistor construction, PNP and NPN, which basically describes the physical arrangement of the P-type and N-type semiconductor materials from which they are made.

Transistors are three terminal active devices made from different semiconductor materials that can act as either an insulator or a conductor by the application of a small signal voltage. The transistor's ability to change between these two states enables it to have two basic functions: "switching" (digital electronics) or "amplification" (analogue electronics). Then bipolar transistors have the ability to operate within three different regions:

1. Active Region - the transistor operates as an amplifier and $Ic = \beta.I_B$
2. Saturation - the transistor is "fully-ON" operating as a switch and $Ic = I_{saturation}$
3. Cut-off - the transistor is "fully-OFF" operating as a switch and $Ic = 0$




The construction and circuit symbols for both the PNP and NPN bipolar transistor are given above with the arrow in the circuit symbol always showing the direction of "conventional current flow" between the base terminal and its emitter terminal. The direction of the arrow always points from the positive P-type region to the negative N-type region for both transistor types, exactly the same as for the standard diode symbol.

The **arrow-head** in the above figures indicated the **emitter and conventional current flow** of a transistor.

**Emitter:**

- The left hand side of the above shown structure can be understood as **Emitter**.
- This has a **moderate size** and is **heavily doped** as its main function is to **supply** a number of **majority carriers**, i.e. either electrons or holes.
- As this emits electrons, it is called as an Emitter.
- This is simply indicated with the letter **E**

**Base**

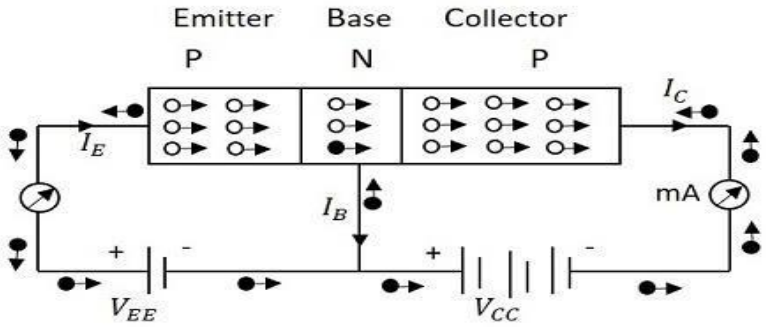
- The middle material in the above figure is the **Base**.
- This is **thin** and **lightly doped**.
- Its main function is to **pass** the majority carriers from the emitter to the collector.
- This is indicated by the letter **B**.

**Collector**

- The right side material in the above figure can be understood as a **Collector**.
- Its name implies its function of **collecting the carriers**.
- This is **a bit larger** in size than emitter and base. It is **moderately doped**.
- This is indicated by the letter **C**.

**Operation PNP Transistor:**

The operation of a PNP transistor can be explained by having a look at the following figure, in which emitter-base junction is forward biased and collector-base junction is reverse biased.




Operation of a PNP transistor

The voltage $\mathbf{V_{EE}}$ provides a positive potential at the emitter which repels the holes in the P-type material and these holes cross the emitter-base junction, to reach the base region. There a very low percent of holes recombine with free electrons of N-region. This provides very low current which constitutes the base current $\mathbf{I_B}$. The remaining holes cross the collector-base junction, to constitute collector current $\mathbf{I_C}$, which is the hole current.

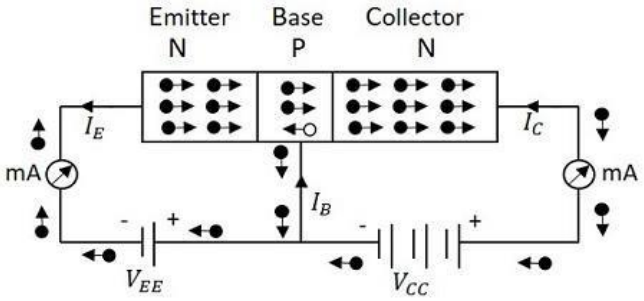
As a hole reaches the collector terminal, an electron from the battery negative terminal fills the space in the collector. This flow slowly increases and the electron minority current flows through the emitter, where each electron entering the positive terminal of $\mathbf{V_{EE}}$, is replaced by a hole by moving towards the emitter junction. This constitutes emitter current $\mathbf{I_E}$.

Hence we can understand that −

- The conduction in a PNP transistor takes place through holes.
- The collector current is slightly less than the emitter current.
- The increase or decrease in the emitter current affects the collector current

**Operation NPN Transistor:**

The operation of an NPN transistor can be explained by having a look at the following figure, in which emitter-base junction is forward biased and collector-base junction is reverse biased.



Operation of a NPN transistor

The voltage $\mathbf{V_{EE}}$ provides a negative potential at the emitter which repels the electrons in the N-type material and these electrons cross the emitter-base junction, to reach the base region. There a very low percent of electrons recombine with free holes of P-region. This provides very low current which constitutes the base current $\mathbf{I_B}$. The remaining holes cross the collector-base junction, to constitute the collector current $\mathbf{I_C}$.

As an electron reaches out of the collector terminal, and enters the positive terminal of the battery, an electron from the negative terminal of the battery $\mathbf{V_{EE}}$ enters the emitter region. This flow slowly increases and the electron current flows through the transistor.

Hence we can understand that

- The conduction in a NPN transistor takes place through electrons.
- The collector current is higher than the emitter current.
- The increase or decrease in the emitter current affects the collector current.

**Advantages**

There are many advantages of a transistor such as −

- High voltage gain.
- Lower supply voltage is sufficient.
- Most suitable for low power applications.
- Smaller and lighter in weight.
- Mechanically stronger than vacuum tubes.
- No external heating required like vacuum tubes.
- Very suitable to integrate with resistors and diodes to produce ICs.

There are few disadvantages such as they cannot be used for high power applications due to lower power dissipation. They have lower input impedance and they are temperature dependent.

**TRANSISTOR CONFIGURATIONS:**

A Transistor has 3 terminals, the emitter, the base and the collector. Using these 3 terminals the transistor can be connected in a circuit with one terminal common to both input and output in a 3 different possible configurations.

**1. Common Base Configuration - has Voltage Gain but no Current Gain.**

**2 Common Emitter Configuration - has both Current and Voltage Gain.**

**3. Common Collector Configuration - has Current Gain but no Voltage Gain.**

**Transistor biasing:**

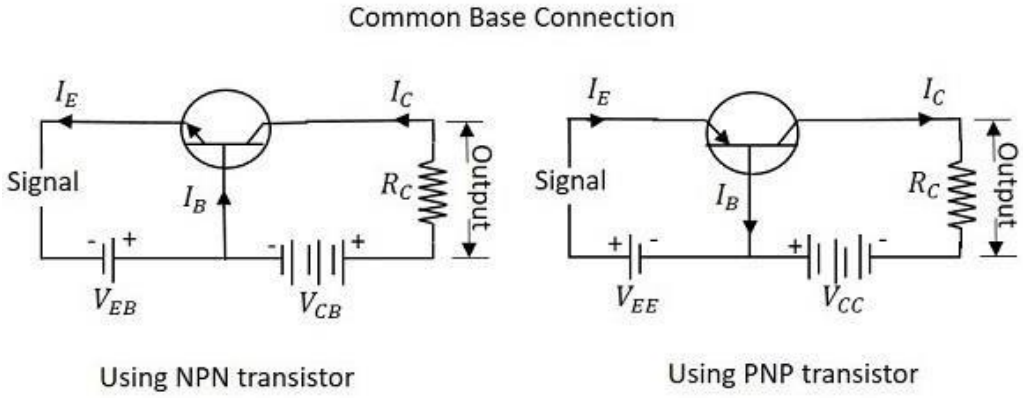
The supply of suitable external dc voltage is called as **biasing**. Either forward or reverse biasing is done to the emitter and collector junctions of the transistor. These biasing methods make the transistor circuit to work in four kinds of regions such as **Active region, Saturation region, Cutoff region** and **Inverse active region**

| EMITTER JUNCTION | COLLECTOR JUNCTION | REGION OF OPERATION |
|---|---|---|
| Forward biased | Forward biased | Saturation region |
| Forward biased | Reverse biased | Active region |
| Reverse biased | Forward biased | Inverse active region |
| Reverse biased | Reverse biased | Cutoff region |

Among these regions, Inverse active region, which is just the inverse of active region, is not suitable for any applications and hence not used

**1. Common Base CB Configuration:**

The name itself implies that the Base terminal is taken as common terminal for both input and output of the transistor. The common base connection for both NPN and PNP transistors is as shown in the following figure.




For the sake of understanding, let us consider NPN transistor in CB configuration. When the emitter voltage is applied, as it is forward biased, the electrons from the negative terminal repel the emitter electrons and current flows through the emitter and base to the collector to contribute collector current. The collector voltage **$V_{CB}$** is kept constant throughout this.

In the CB configuration, the input current is the emitter current **$I_E$** and the output current is the collector current **$I_C$**.

**Current Amplification Factor** α:

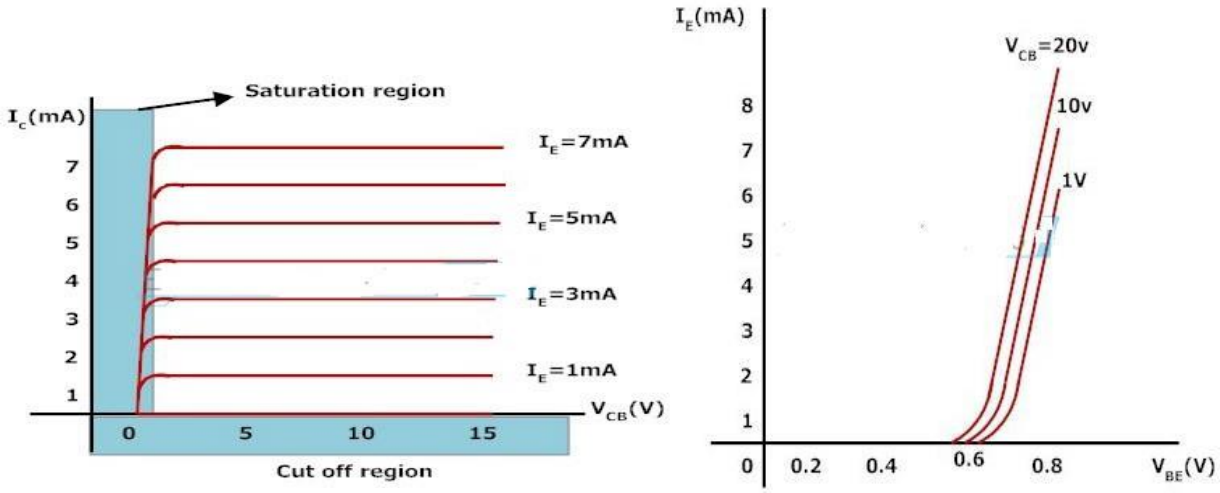
he ratio of change in collector current ΔIC to the change in emitter current ΔIE when collector voltage **$V_{CB}$** is kept constant, is called as **Current amplification factor**. It is denoted by α

$$\alpha = \frac{\Delta I_C}{\Delta I_E} \; at\ constant\ V_{CB}$$

**Characteristics of CB configuration:**

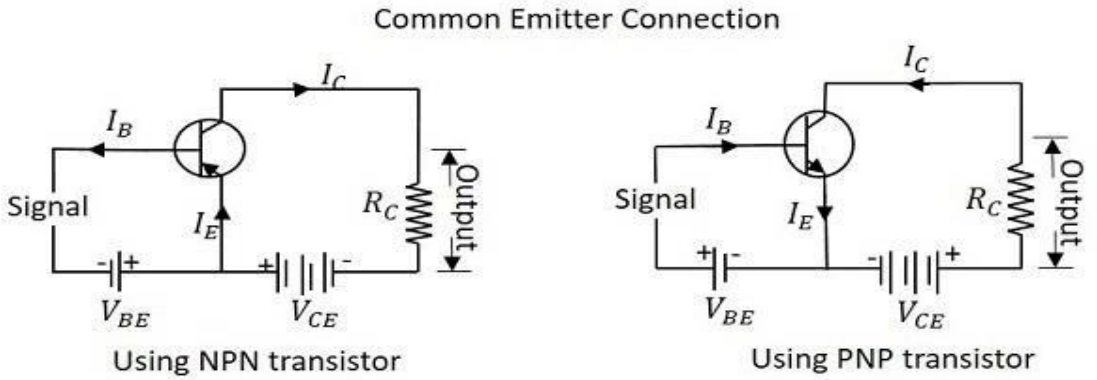
Being **$V_{CB}$** constant, with a small increase in the Emitter-base voltage $V_{EB}$, Emitter current **$I_E$** gets increased.

Emitter Current **$I_E$** is independent of Collector voltage **$V_{CB}$**.




**Common Emitter CE Configuration:**

The name itself implies that the Emitter terminal is taken as common terminal for both input and output of the transistor. The common emitter connection for both NPN and PNP transistors is as shown in the following figure.




Just as in CB configuration, the emitter junction is forward biased and the collector junction is reverse biased. The flow of electrons is controlled in the same manner. The input current is the base current $\mathbf{I_B}$ and the output current is the collector current $\mathbf{I_C}$ here

**Base Current Amplification factor** β:

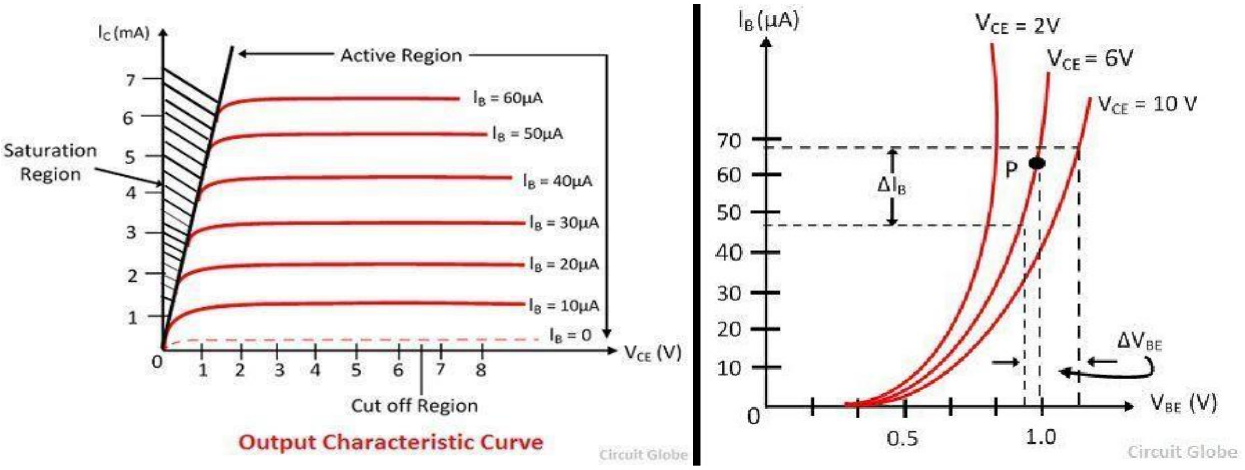
The ratio of change in collector current ΔIC to the change in base current ΔIB is known as **Base Current Amplification Factor**. It is denoted by β

$$\beta = \frac{\Delta I_C}{\Delta I_B}$$

Hence, **the current gain in Common Emitter connection is very high**. This is the reason this circuit connection is mostly used in all transistor applications.

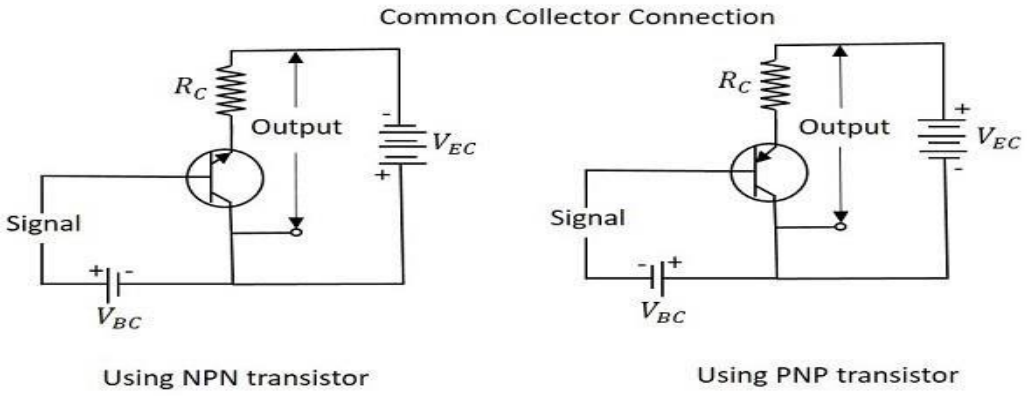
**Characteristics of CE Configuration:**

- Keeping $\mathbf{V_{CE}}$ constant, with a small increase in $\mathbf{V_{BE}}$ the base current $\mathbf{I_B}$ increases rapidly than in CB configurations.
- For any value of $\mathbf{V_{CE}}$ above knee voltage, $\mathbf{I_C}$ is approximately equal to $\beta\mathbf{I_B}$.



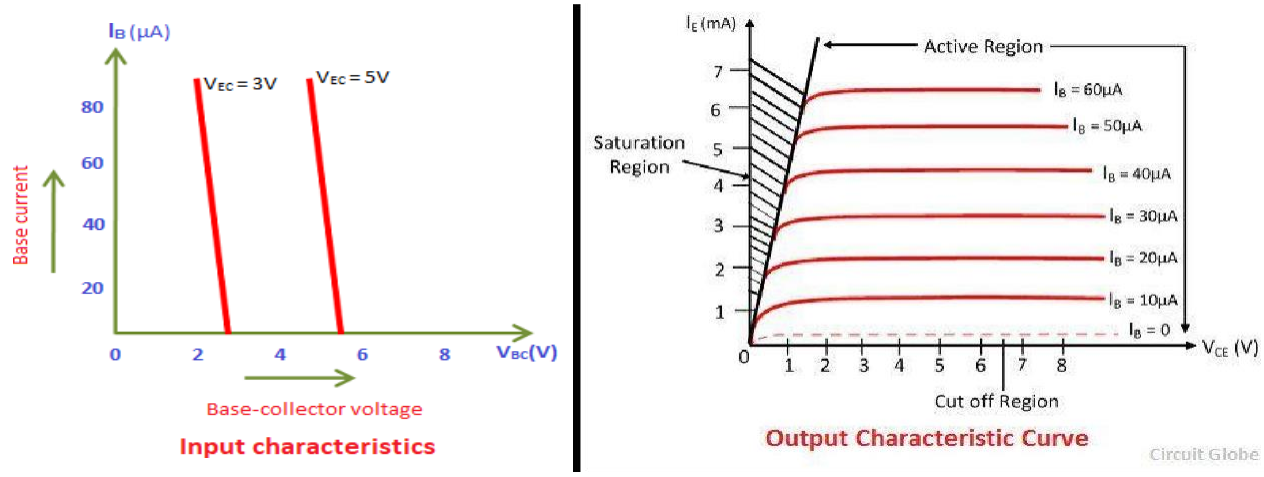

### 3. Common Collector (CC) Configuration:

The name itself implies that the **Collector** terminal is taken as common terminal for both input and output of the transistor. The common collector connection for both NPN and PNP transistors is as shown in the following figure




Just as in CB and CE configurations, the emitter junction is forward biased and the collector junction is reverse biased. The flow of electrons is controlled in the same manner. The input current is the base current $I_B$ and the output current is the emitter current $I_E$ here.

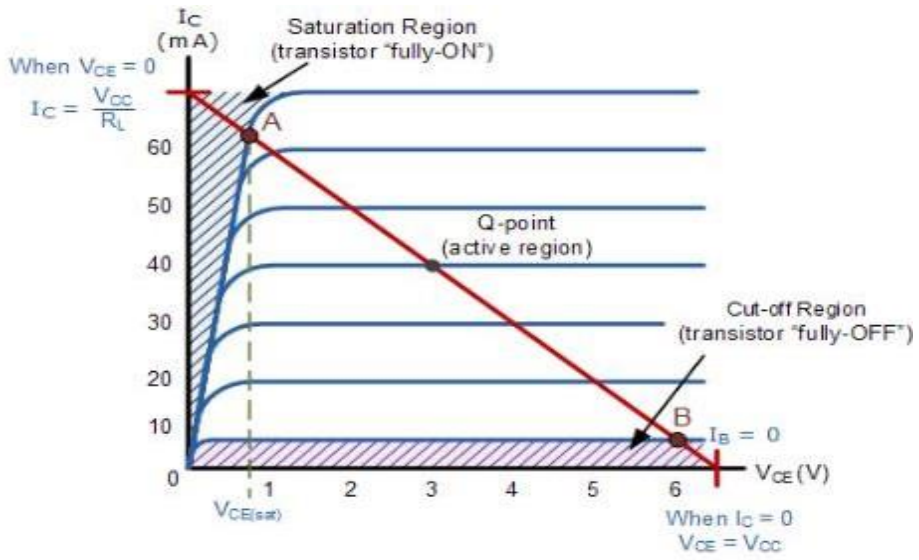
### Characteristics of CC Configuration:



**BJT Operating Point:**

The line drawn in between output voltage and output current is called load line.

The point at which touches the load line is called Q point/operation point/Quescent point.




## Methods of Transistor Biasing

The biasing in transistor circuits is done by using two DC sources $V_{BB}$ and $V_{CC}$. It is economical to minimize the DC source to one supply instead of two which also makes the circuit simple.

The commonly used methods of transistor biasing are

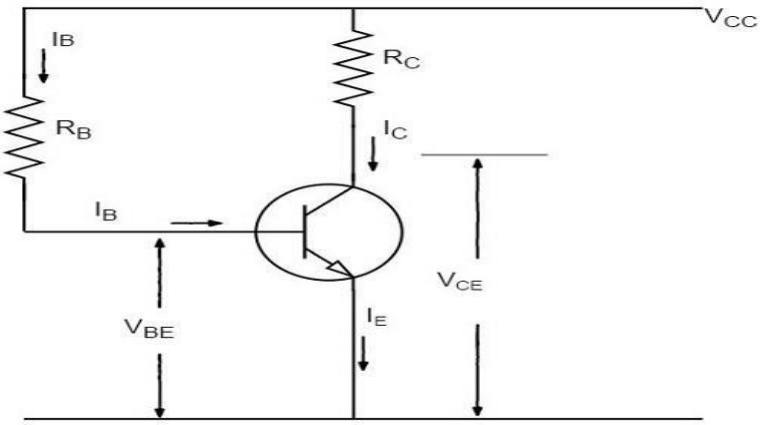
- Base Resistor method (**fixed bias method**)
- Collector to Base bias
- Voltage-divider bias

All of these methods have the same basic principle of obtaining the required value of $I_B$ and $I_C$ from $V_{CC}$ in the zero signal conditions.

### 1. Base Resistor method (fixed bias method):

In this method, a resistor $R_B$ of high resistance is connected in base, as the name implies. The required zero signal base current is provided by $V_{CC}$ which flows through $R_B$. The base emitter junction is forward biased, as base is positive with respect to emitter.

The required value of zero signal base current and hence the collector current (as $I_C = \beta I_B$) can be made to flow by selecting the proper value of base resistor RB. Hence the value of $R_B$ is to be known. The figure below shows how a base resistor method of biasing circuit looks like.



Let $I_C$ be the required zero signal collector current. Therefore,

We know that $V_{CC}$ is a fixed known quantity and $I_B$ is chosen at some suitable value. As $R_B$ can be found directly, this method is called as **fixed bias method**.

**Advantages:**

- The circuit is simple.
- Only one resistor $R_E$ is required.
- Biasing conditions are set easily.
- No loading effect as no resistor is present at base-emitter junction.

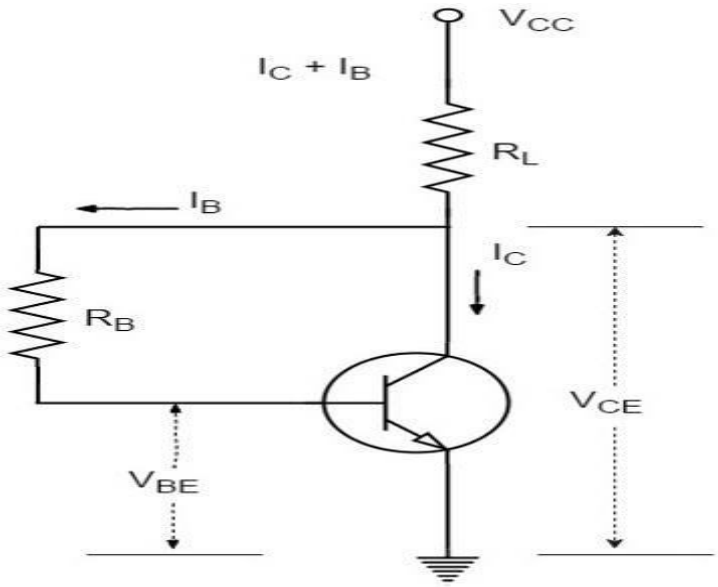
**Disadvantages:**

- The stabilization is poor as heat development can't be stopped.
- The stability factor is very high. So, there are strong chances of thermal run away.

Hence, this method is rarely employed.

**2. Collector to Base Bias:**

The collector to base bias circuit is same as base bias circuit except that the base resistor $R_B$ is returned to collector, rather than to $V_{CC}$ supply as shown in the figure below

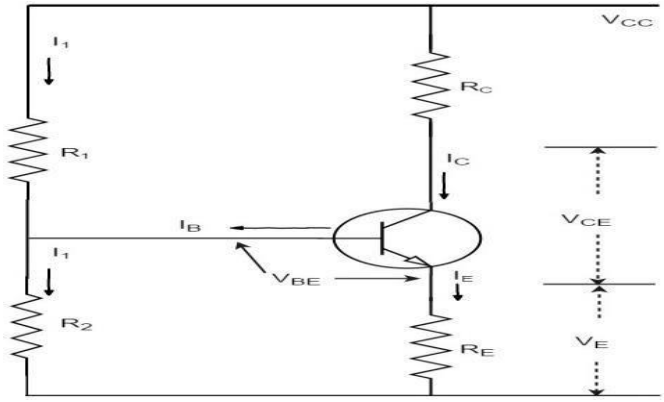



This circuit helps in improving the stability considerably. If the value of $I_C$ increases, the voltage across $R_L$ increases and hence the $V_{CE}$ also increases. This in turn reduces the base current $I_B$. This action somewhat compensates the original increase.

**Voltage Divider Bias Method:**

Among all the methods of providing biasing and stabilization, the **voltage divider bias method** is the most prominent one. Here, two resistors $R_1$ and $R_2$ are employed, which are connected to $V_{CC}$ and provide biasing. The resistor $R_E$ employed in the emitter provides stabilization.

The name voltage divider comes from the voltage divider formed by $R_1$ and $R_2$. The voltage drop across $R_2$ forward biases the base-emitter junction. This causes the base current and hence collector current flow in the zero signal conditions. The figure below shows the circuit of voltage divider bias method.




Suppose that the current flowing through resistance $R_1$ is $I_1$. As base current $I_B$ is very small, therefore, it can be assumed with reasonable accuracy that current flowing through $R_2$ is also $I_1$.
Now let us try to derive the expressions for collector current and collector voltage.

Suppose there is a rise in temperature, then the collector current $I_C$ decreases, which causes the voltage drop across $R_E$ to increase. As the voltage drop across R2 is V2, which is independent of IC, the value of $V_{BE}$ decreases. The reduced value of $I_B$ tends to restore $I_C$ to the original value.

## Hybrid parameters (h-parameters)

To form a transistor amplifier it is only necessary to connect an external load and signal source as indicated in **fig. 1** and to bias the transistor properly. Consider the two-port network of CE amplifier. $R_S$ is the source resistance and $Z_L$ is the load impedance h-parameters are assumed to be constant over the operating range

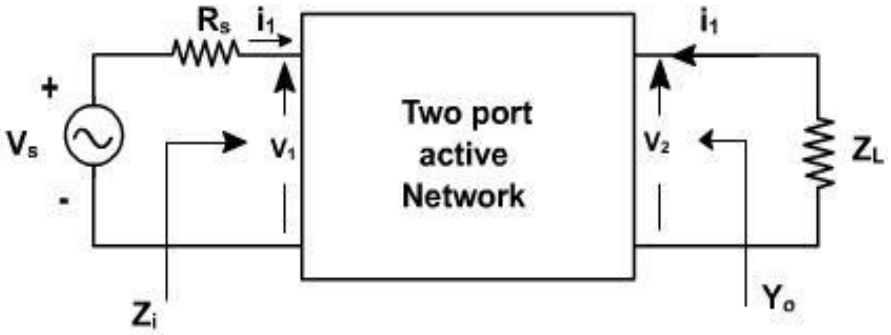



**Fig. 1**

Based on the definition of hybrid parameters the mathematical model for two port networks known as h-parameter model can be developed.
If the input current $I_1$ and output voltage $V_2$ are taken as independent variables, the dependent variables $V_1$ and $I_2$ can be written as

$$\begin{bmatrix} V_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ V_2 \end{bmatrix}$$

The hybrid equations can be written as:

$$\mathbf{V_1 = h_i I_1 + h_r V_2 \ OR \ V_1 = h_{11} I_1 + h_{12} V_2} \quad \text{..... (1)}$$

$$\mathbf{I_2 = h_f I_1 + h_o V_2 \ OR \ I_2 = h_{21} I_1 + h_{22} V_2} \quad \text{---------- (2)}$$

***i*=11= input : *o* = 22 = output**
***f* =21 = forward transfer: *r* = 12 = reverse transfer**
If these parameters are specified for a particular configuration, then suffixes e, b or c are also included, e.g. $h_{fe}$, $h_{ib}$ are h parameters of common emitter and common collector amplifiers

Where h11, h12, h21, h22 are called as hybrid parameters.

$$h_{11} = \left.\frac{V_1}{I_1}\right|_{V_2=0}$$

Input impedance with o/p port short circuited

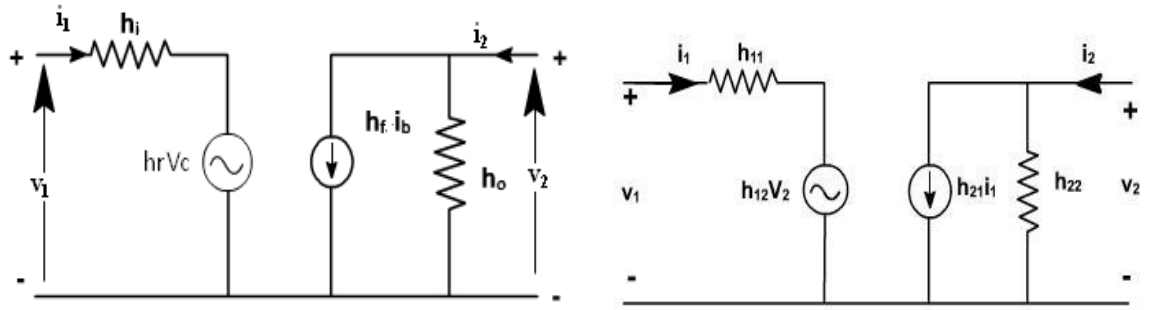
$$h_{12} = \left.\frac{V_1}{V_2}\right|_{I_1=0}$$

Reverse voltage transfer ratio with i/p port open circuited

$$h_{22} = \left.\frac{I_2}{V_2}\right|_{I_1=0}$$

Forward voltage transfer ratio with o/p port short circuited

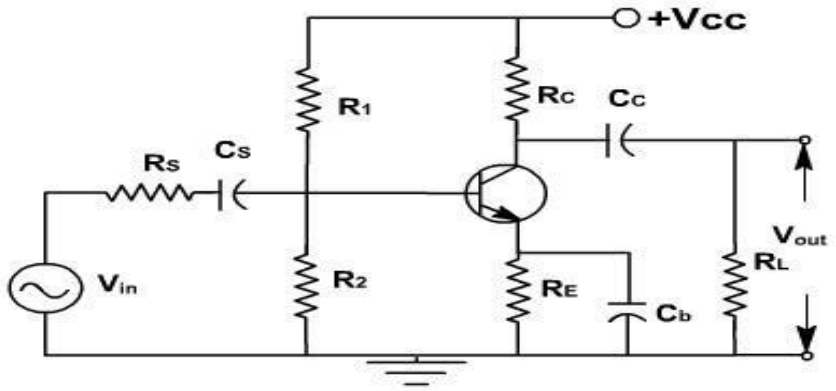
$$h_{21} = \left.\frac{I_2}{I_1}\right|_{V_2=0}$$




**Small Signal CE Amplifier:**

The amplifier circuit that is formed using a CE configured transistor combination is called as CE amplifier. CE amplifiers are very popular to amplify the small signal ac. As long as the input signal is small, the transistor will use only a small part of the load line and the operation will be linear. On the other hand, if the input signal is too large. The fluctuations along the load line will drive the transistor into either saturation or cut off.

The CE amplifier configuration is shown in fig. 1.




The coupling capacitor (CC ) passes an ac signal from one point to another. At the same time it does not allow the dc to pass through it. Hence it is also called blocking capacitor.

**Construction:**

The common emitter amplifier circuit using NPN transistor is as shown below, the input signal being applied at emitter base junction and the output signal being taken from collector base junction.

The emitter base junction is forward biased by $V_{EE}$ and collector base junction is reverse biased by $V_{CC}$. The operating point is adjusted with the help of resistors $R_e$ and $R_c$. Thus the values of $I_c$, $I_b$ and $I_{cb}$ are decided by $V_{CC}$, $V_{EE}$, $R_e$ and $R_c$.

**Operation:**

When no input is applied, the quiescent conditions are formed and no output is present. When positive half of the signal is being applied, the voltage between base and emitter $V_{be}$ is increased because it is already positive with respect to ground.

As forward bias increases, the base current too increases accordingly. Since $I_C = \beta I_B$, the collector current increases as well.

The following circuit diagram shows a CE amplifier with self-bias circuit.

The collector current when flows through $R_C$, the voltage drop increases.

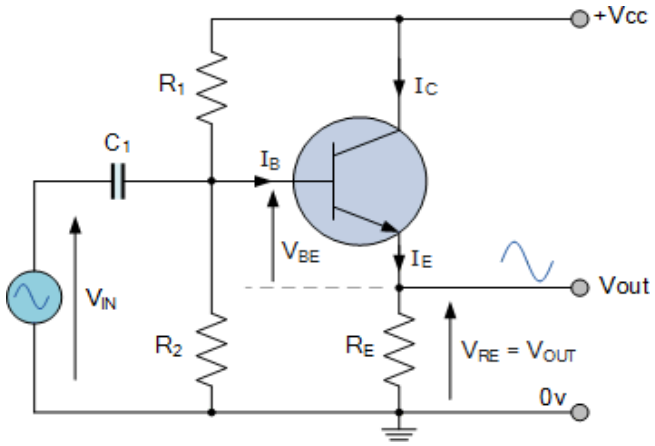
$$V_C = I_C R_C$$

As a consequence of this, the voltage between collector and emitter decreases. Because,

$$V_{CB} = V_{CC} - I_C R_C$$

Thus, the amplified voltage appears across $R_C$. Therefore, in a CE amplifier, as the positive going signal appears as a negative going signal, it is understood that there is a phase shift of 180° between input and output. CE amplifier has a high input impedance and lower output impedance than CB amplifier. The voltage gain and power gain are also high in CE amplifier and hence this is mostly used in Audio amplifiers.

**COMMON COLLECTOR AMPLIFIER:**

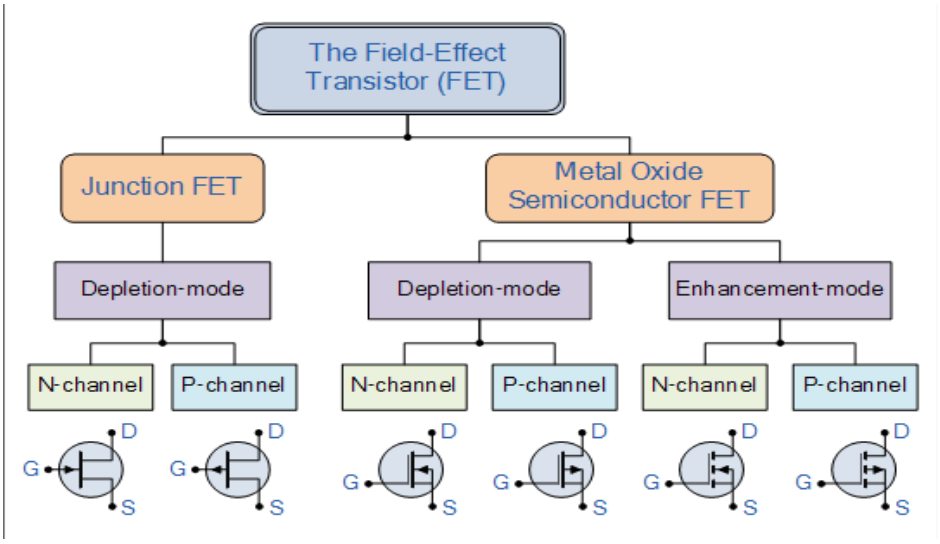



Resistors $R_1$ and $R_2$ form a simple voltage divider network used to bias the NPN transistor into conduction. Since this voltage divider lightly loads the transistor, the base voltage, $V_B$ can be easily calculated by using the simple voltage divider formula as shown.

# Field Effect Transistors

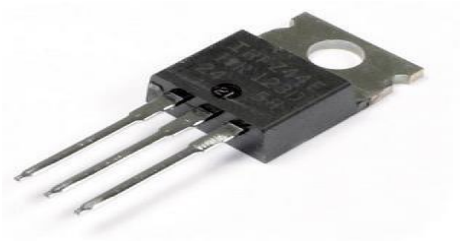
The Field effect transistor is abbreviated as FET, it is an another semiconductor device like a BJT which can be used as an amplifier or switch. The Field effect transistor is a voltage operated (controlled) device. Whereas Bipolar junction transistor is a current controlled device. Unlike BJT a FET requires virtually no input current. Drain Current (Id) depends on the Vgs (gate source) voltage. So that's why it is called as voltage controlled device.

Classification of FETs are shown in below fig.




**Junction Field Effect Transistor:**

An FET is a three-terminal unipolar semiconductor device. It is a **voltage controlled device** unlike a bipolar junction transistor. The main advantage of FET is that it has a very high input impedance, which is in the order of Mega Ohms. It has many advantages like low power consumption, low heat dissipation and FETs are highly efficient devices. The following image shows how a practical FET looks like



The FET is a **unipolar device**, which means that it is made using either p-type or n-type material as main substrate. Hence the current conduction of a FET is done by either electrons or holes.

**Features of FET:**

The following are the varied features of a Field Effect Transistor.

**Unipolar** − It is unipolar as either holes or electrons are responsible for conduction.

**High input impedance** − The input current in a FET flows due to the reverse bias. Hence it has high input impedance.

**Voltage controlled device** − As the output voltage of a FET is controlled by the gate input voltage, FET is called as the voltage controlled device.

**Noise is low** − There are no junctions present in the conduction path. Hence noise is lower than in BJTs.

**Gain is characterized as transconductance:** Transconductance is the ratio of change in output current to the change in input voltage.

**The output impedance of a FET is low.**

**Advantages of FET:**

To prefer a FET over BJT, there should be few advantages of using FETs, rather than BJTs. Let us try to summarize the advantages of FET over BJT.

| JFET | BJT |
|---|---|
| It is an unipolar device | It is a bipolar device |
| Voltage driven device | Current driven device |
| High input impedance | Low input impedance |
| Low noise level | High noise level |
| Better thermal stability | Less thermal stability |
| Gain is characterized by transconductance | Gain is characterized by voltage gain |

**Applications of FET**

- FET is used in circuits to reduce the loading effect.
- FETs are used in many circuits such as Buffer Amplifier, Phase shift Oscillators and Voltmeters

**FET Terminals:**

Though FET is a three terminal device, they are not the same as BJT terminals. The three terminals of FET are Gate, Source and Drain. The Source terminal in FET is analogous to the Emitter in BJT, while Gate is analogous to Base and Drain to Collector.

The symbols of a FET for both NPN and PNP types are as shown below


Symbol of n-channel FET  Symbol of p-channel FET

**Source**

- The Source terminal in a Field Effect Transistor is the one through which the carriers enter the channel.
- This is analogous to the emitter terminal in a Bipolar Junction Transistor.
- The Source terminal can be designated as **S**.
- The current entering the channel at Source terminal is indicated as $I_S$.

**Gate**

- The Gate terminal in a Field Effect Transistor plays a key role in the function of FET by controlling the current through the channel.
- By applying an external voltage at Gate terminal, the current through it can be controlled.
- Gate is a combination of two terminals connected internally that are heavily doped.
- The channel conductivity is said to be modulated by the Gate terminal.
- This is analogous to the base terminal in a Bipolar Junction Transistor.
- The Gate terminal can be designated as **G**.
- The current entering the channel at Gate terminal is indicated as IG.

**Drain**

- The Drain terminal in a Field Effect Transistor is the one through which the carriers leave the channel.
- This is analogous to the collector terminal in a Bipolar Junction Transistor.
- The Drain to Source voltage is designated as VDS.
- The Drain terminal can be designated as **D**.
- The current leaving the channel at Drain terminal is indicated as $I_D$.

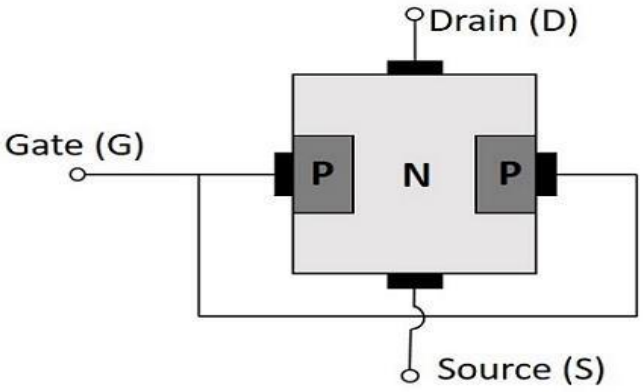
**JFET:**

The JFET is abbreviated as **Junction Field Effect Transistor**. JFET is just like a normal FET. The types of JFET are n-channel FET and P-channel FET. A p-type material is added to the n-type substrate in n-channel FET, whereas an n-type material is added to the p type substrate in p-channel FET. Hence it is enough to discuss one type of FET to understand both

**N-Channel FET:**

The N-channel FET is the mostly used Field Effect Transistor. For the fabrication of N channel FET, a narrow bar of N-type semiconductor is taken on which P-type material is formed by diffusion on the opposite sides. These two sides are joined to draw a single connection for gate terminal.

These two gate depositions p−type materials p−type materials form two PN diodes. The area between gates is called as a **channel**. The majority carriers pass through this channel. Hence the cross sectional form of the FET is understood as the following figure.




Structure of N-channel FET

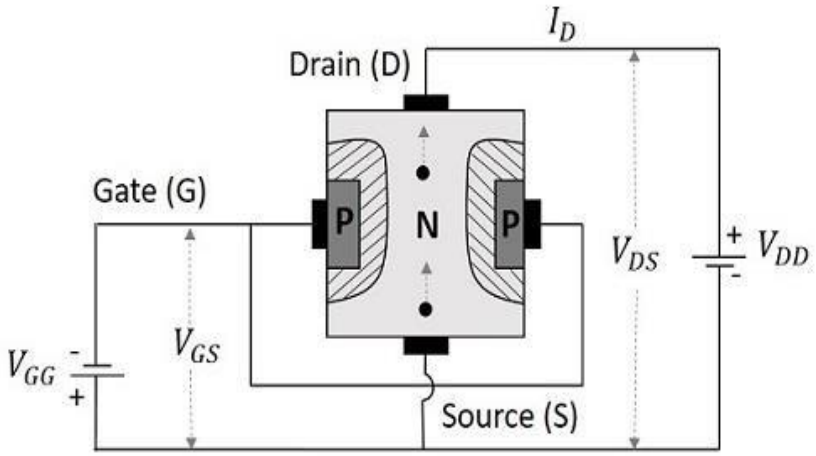
Ohmic contacts are made at the two ends of the n-type semiconductor bar, which form the source and the drain. The source and the drain terminals may be interchanged.

**Operation of N-channel FET:**

Before going into the operation of the FET one should understand how the depletion layers are formed. For this, let us suppose that the voltage at gate terminal say $\mathbf{V_{GG}}$ is reverse biased while the voltage at drain terminal say $\mathbf{V_{DD}}$ is not applied. Let this be the case 1.

- In **case 1**, When $\mathbf{V_{GG}}$ is reverse biased and $\mathbf{V_{DD}}$ is not applied, the depletion regions between P and N layers tend to expand. This happens as the negative voltage applied, attracts the holes from the p-type layer towards the gate terminal.
- In **case2**,When $\mathbf{V_{DD}}$ isapplied positiveterminaltodrainandnegativeterminaltosourcepositiveterminaltodrainandnegativeterminaltosource and $\mathbf{V_{GG}}$ is not applied, the electrons flow from source to drain which constitute the drain current $\mathbf{I_D}$.

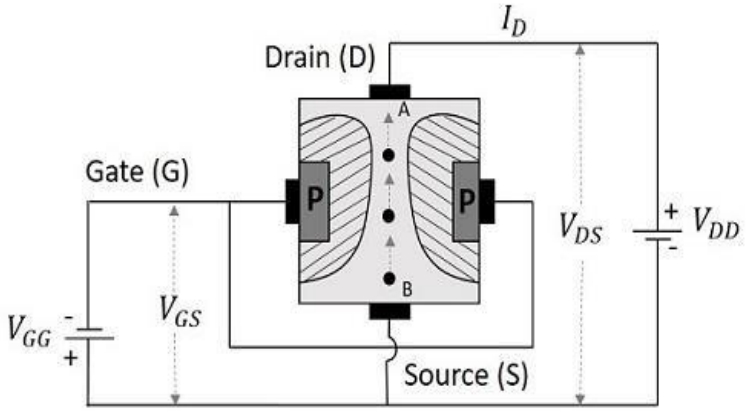
Let us now consider the following figure, to understand what happens when both the supplies are given




The supply at gate terminal makes the depletion layer grow and the voltage at drain terminal allows the drain current from source to drain terminal. Suppose the point at source terminal is B and the point at drain terminal is A, then the resistance of the channel will be such that the voltage drop at the terminal A is greater than the voltage drop at the terminal B.

Which means, $V_A > V_B$

Hence the voltage drop is being progressive through the length of the channel. So, the reverse biasing effect is stronger at drain terminal than at the source terminal. This is why the depletion layer tends to penetrate more into the channel at point A than at point B, when both $\mathbf{V_{GG}}$ and $\mathbf{V_{DD}}$ are applied. The following figure explains this.

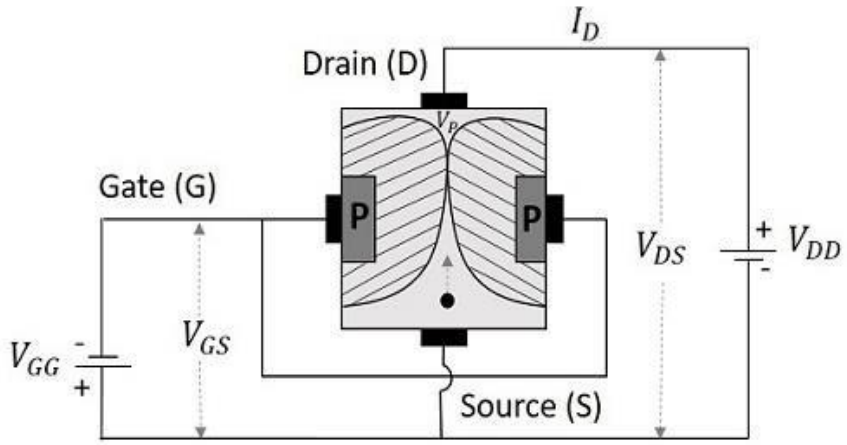



Now that we have understood the behavior of FET, let us go through the real operation of FET.

**Depletion Mode of Operation:**

Let us consider that there is no potential applied between gate and source terminals and a potential $\mathbf{V_{DD}}$ is applied between drain and source. Now, a current $\mathbf{I_D}$ flows from drain to source terminal, at its maximum as the channel width is more. Let the voltage applied between gate and source terminal $\mathbf{V_{GG}}$ is reverse biased. This increases the depletion width, as discussed above. As the layers grow, the cross-section of the channel decreases and hence the drain current $\mathbf{I_D}$ also decreases.

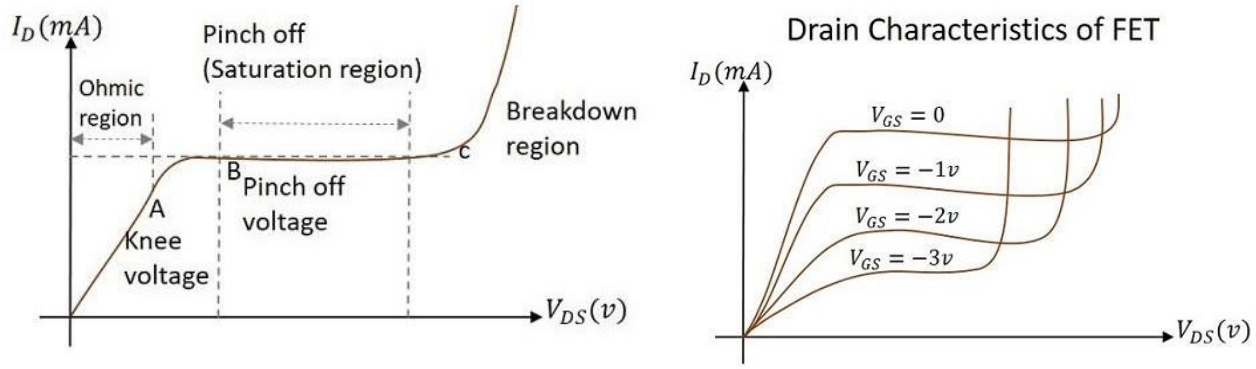
When this drain current is further increased, a stage occurs where both the depletion layers touch each other, and prevent the current $\mathbf{I_D}$ flow. This is clearly shown in the following figure.



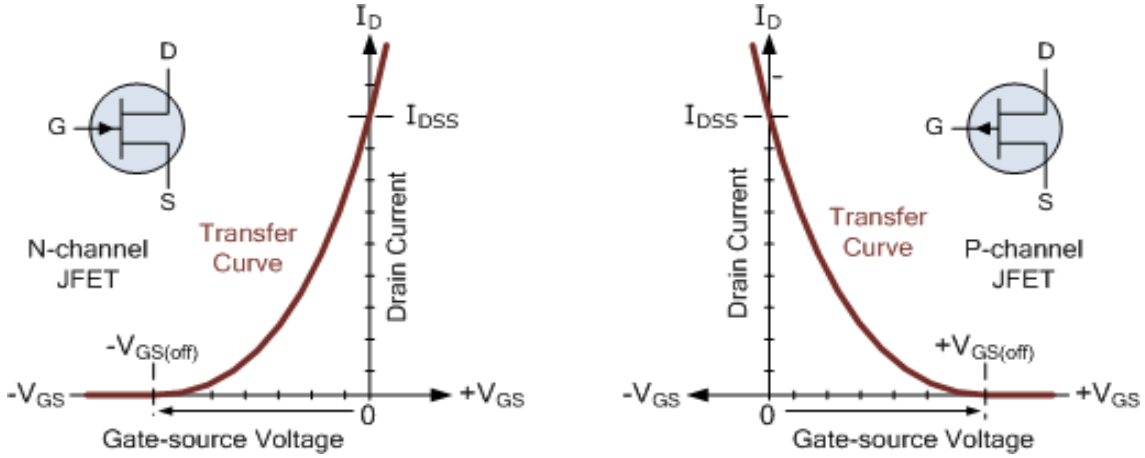

The voltage at which both these depletion layers literally "touch" is called as "**Pinch off voltage**". It is indicated as VP. The drain current is literally nil at this point. Hence the drain current is a function of reverse bias voltage at gate.

Since gate voltage controls the drain current, FET is called as the **voltage controlled device**. This is more clearly understood from the drain characteristics curve.

**Drain (output) Characteristics of JFET:**




The drain characteristics are plotted for drain current **$I_D$** against drain source voltage **$V_{DS}$** for different values of gate source voltage VGS. The overall drain characteristics for such various input voltages is as given under.




As the negative gate voltage controls the drain current, FET is called as a Voltage controlled device. The drain characteristics indicate the performance of a FET. The drain characteristics plotted above are used to obtain the values of Drain resistance, Transconductance and Amplification Factor.

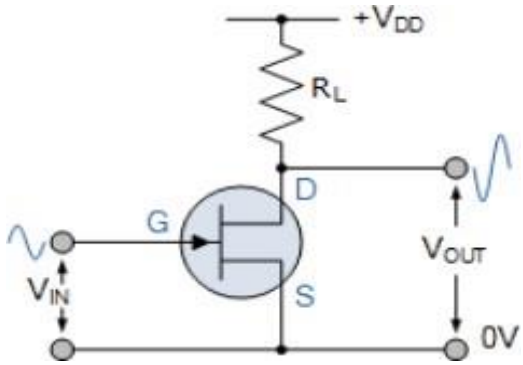
**Drain current in the active region.**

$$I_D = I_{DSS}\left[1-\frac{V_{GS}}{V_P}\right]^2$$

**Configurations of JFET:**

Like the bipolar junction transistor, the field effect transistor being a three terminal device is capable of three distinct modes of operation and can therefore be connected within a circuit in one of the following configurations.

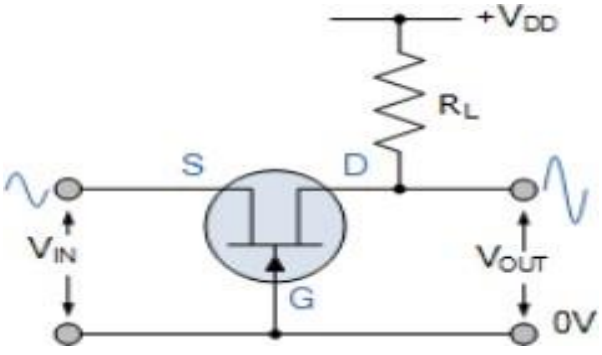
1.Common Source (CS) Configuration:




In the **Common Source** configuration (similar to common emitter), the input is applied to the Gate and its output is taken from the Drain as shown. This is the most common mode of operation of the FET due to its high input impedance and good voltage amplification and as such Common Source amplifiers are widely used.

The common source mode of FET connection is generally used audio frequency amplifiers and in high input impedance pre-amps and stages. Being an amplifying circuit, the output signal is $180^o$ "out-of-phase" with the input.

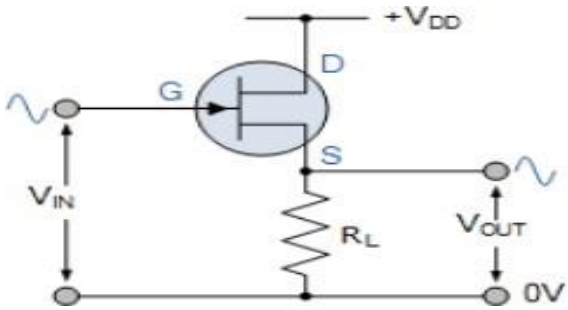
**Common Gate (CG) Configuration**




In the **Common Gate** configuration (similar to common base), the input is applied to the Source and its output is taken from the Drain with the Gate connected directly to ground (0v) as shown. The high input impedance feature of the previous connection is lost in this configuration as the common gate has a low input impedance, but a high output impedance.

This type of FET configuration can be used in high frequency circuits or in impedance matching circuits were a low input impedance needs to be matched to a high output impedance. The output is "in-phase" with the input.

**Common Drain (CD) Configuration:**




In the **Common Drain** configuration (similar to common collector), the input is applied to the Gate and its output is taken from the Source. The common drain or "source follower" configuration has a high input impedance and a low output impedance and near-unity voltage gain so is therefore used in buffer amplifiers. The voltage gain of the source follower configuration is less than unity, and the output signal is "in-phase", $0^o$ with the input signal.

This type of configuration is referred to as "Common Drain" because there is no signal available at the drain connection, the voltage present, $+V_{DD}$ just provides a bias. The output is in-phase with the input.

----------THE END----------