of Open in a plin of the mi

- Introduction to op Amp, Differential Amplifier

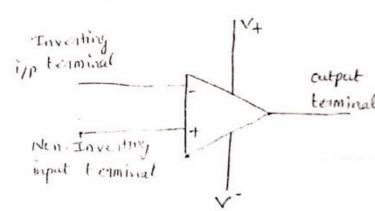
Configurations, CMRR, PSRR, Slew rate. Block diagram, PIN Configuration of 741 op- Amp. Characteristics of Ideal OP-Amp - Concept of virtual ground. Op-Amp Applications:

Inventing: Non-inventing Amplifier, Summing and differential amplifier. Voltage followers, Comparator,

Differentiator, Integrator.

The circuit setumatic of an Op Hopis a triangle shape representation. It can be represented with five terminal representation.

Two terminals for Supply, two terminels for input and one for culput.



There are three popular packages are available

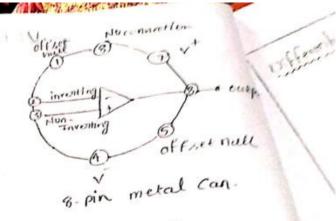
- ii) Deal in line package
- iii) Flat type package.

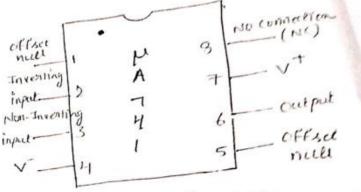
Op. Amp packages may contain single, two (01) four op Amps. Typical packages may have a terminals to terminals and some times 14 terminals. The widely used op Homps are MATHI and the MATHY is a head 7111





In these two sections,
there are 8 pins numbered in causen
clockwise. PIN I and PIN 5 represents
fixet null, PIN 2 is called
inverting input terminal and
PIN 3 is the Non-inverting input
terminal, PIN-6 is called output
terminal and PIN 7 & PIN 4
are the power supply terminal





8 pin Dual Inline package

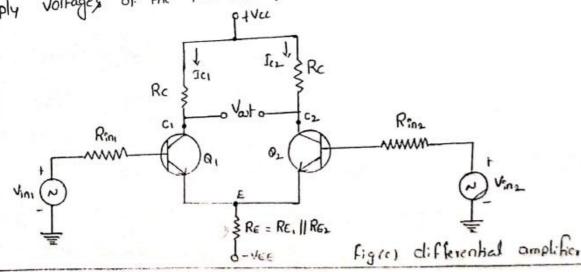
as NC indicates " No Connection". The terminal plas are started at where the det representation is presented.

Each Manufactures uses a specific code and assigns a specific type numbers to the Ic. The codes used by some of the we known manufacturers of Linear Icls are.

- i) Fairchild MA, MAF
- ii) National semi conductor. LM
- iii) Motorola Mc, MFC
- iv) RCA CA, CD
- V) Texas instrument SN
- 11) Signetics N/s, NE/n-

(a) Two identical emitter biased circuits

Let us consider two identical emitter biased Circuits using transistors Q, and Q2 as shown in fig(a). The transistors Q, and Q2 are have identical characteristics with RE1 and RC2, RC1 = RC2 and |Vcc| = |-Vee| have identical characteristics with RE1 and RC2, RC1 = RC2 and |Vcc| = |-Vee| have identical characteristics with RE1 and RC2, RC1 = RC2 and |Vcc| = |-Vee| have circuits can be obtained by combining the two circuits can emitter biased circuit of fig(a) together. These two circuits can be combined together as shown in fig(b). we also connect the tvec be combined together as shown in fig(b). we also connect the tvec be poly voltages of the two circuits and connect the -VEE supply voltages of the two circuits and connect the -VEE supply voltages



C

Let us connect the emiller E, of transister 0, to the Conster E2 of transister 02. Thus, RE, gets connected in parallel with RE2. we also apply an input signal Vin, to the base B1 of transister 0, and Vine to the base B2 of transister 02. The output voltage is obtained between the collectors C1 and C2

fig (c) shows the emitter coupled differential amplifier, This amplifier is dual input babanced output type amplifier, As the input signals are applied to both the input terminals, it is called as dual input and as the output is obtained between the collector of the two transistors, it is called as balanced output, since the output is obtained between two collectors it is known differential output. This amplifier is known as emitter coupled amplifier because the emitters of both the transistors are connected together

Hamat blood An Of amp is a direct Coupled multistage amplifier. The different stages of op- Amp are 1) Input stage --i) First stage ib) Second stage (Intermediate stage) a) Level shifter. 3) Output stage. Diff exential Different Level Amplifier Amplifier first stage Int connection stage Qual input & Deal input & Untralanced off Balanced c/p INDIA BOOK *) In input stage, the First and second stages are coscoded differential - YEE Block diagram of op. Amb. amplifiers used to provid high

* The differential amplifier amplifies the difference of the input signal.

gain .

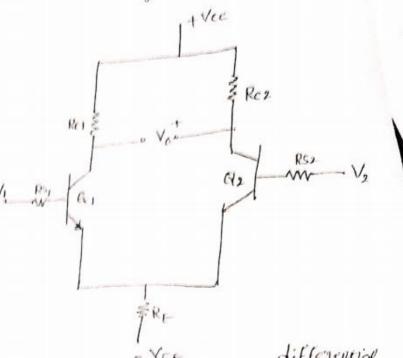
(i) First stage:

The first stage is a dual input balanced output differential amplifier. In this configuration two input signals are used and output is balanced because

Leminals which one of Jame De potential.

- high input impedance.
- +) The CMRR is the ability of canceling the Common signal with
- B. Hall settles
- Dilligh vellage gain
- ii) High iff impedance
- iv) Small t/p offset vellage
- v) Small i/p offset current
- vi) High CHRR
- VII) Lew bias current

1 11



amplifier

The overall gain requirement of Of-Amp is very high.

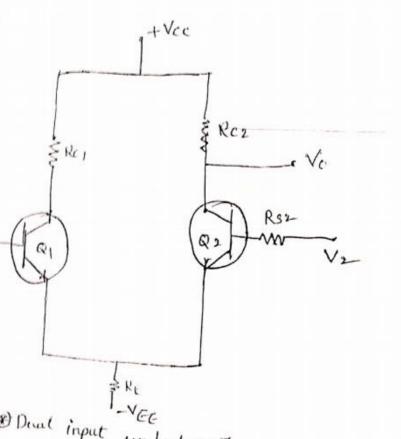
Input first stage alone cannot provide such high gairs.

So, we go for second stage of differential Amplified. Vi

e) Requirements:

Nery High & Voltage, gain.

Direct Coupling with out



Deal input unbalanced output

second stage of op Amp is a dual input unhalanced output, executive amplificil. In this configuration two input signals size used and output is measured at one of the collectors terminals with respect to ground. It is related to unbalanced output because the collector at which output is measured is at some finite DC potential i.e, there is a DC voltage at the output terminal without any input signal.

*) The second stage provides some additional voltage gain.

practically thes stage consists of chain of cascaded amplified called "Multistage amplified".

As we are going for direct coupling without capacitons, the dc component is not filtered. Due to that, it is to be also filtered.

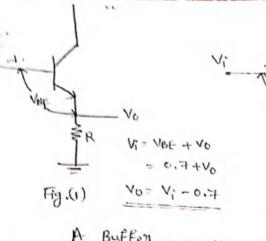
There are two reasons for using a level shift in operational amplifier.

(i) Because of direct coupling the amplifier also amplifies the dc

Because of curent troping to level raises from stage to signals. as a result the Dc level raises from stage to stage. Due to this high voltage levels, the transistoris are drives into saturation so total which may caus clipping of the o/p voltage. So that the level shifter is cused to shift the Dc level to zero with respect to ground, when no o/p signal is applied.

- ii) The output should have Quisent voltage level (

 zero volts for 2010 input signal for belter amplifi
 - emitten follower shown in figures



Vi = VBE + VO (RITE) Vo = R2 (Vi-0.7) Fig (2)

A Buffer cusually used here is an emitter follower with high i/p impedance.

From Fig (i) the amount of shift obtained is Vo = Vi-0.7. This shift is in sufficient. So, of can be taken at the junction of two resistors R, E, R2 as shown in hig(2). Now, shift obtained is Vo = R2 (Vi - 0.7)

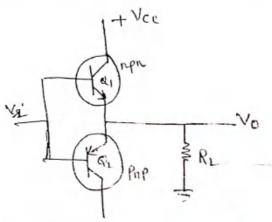
But this arrangement has the disadvantage that the signal voltage also gets allemented by K2/2,+R2' This disadvantage can be ever come by replacing R2 with convent mimor circuit. Cateco

The function of the output stage in op-Amp to supply the load current and provide a low Ofp impedance.

A simple output stage is an emitter follower with complementary transistors is as shown in the figure When Vi is positive, Q is ON and supplies current to the load When Vi is negative, Q = is off and Q2 acts as a sink to remove

* The output stage provides "

- i) Large ofp voltage swing compacity.
- ii) Low of resistance.
- iii) Short circuit protection.



Been that the source current flows throught signal source and Therefore, the signal source could be capable of providing his load arment. of 741 of Amp:

The 741 Op. Amp is originally manuformered by Fairchild and it is sold us MA 741. Where MA represents the neuro factions code.

The 741 Op Amp is also manufactured by some other mary factoreys.

LM741 Ex: National Semi conductor 1901741 Motorola SN 52741 Texus instruments NS 741 Signetics CA 3741 RCA

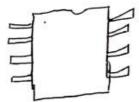
All these op-Amps have some specifications.

-> There whe three types of packages.

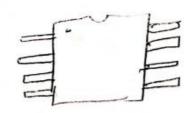
i) The PA Metal Can

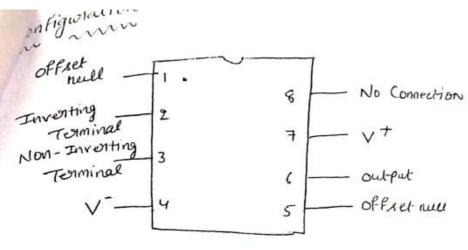


(ii) The Metal Contype Dual in line package



Dust in the package Flat type package (iii)





Features :-

- i) No Frequency Compensation required.
- (ii) Short circuit Protection
 - iii) Offset met voltage neel capacity
 - iv) Lower power Consumption.
 - N) Large Common mode & differential input voltage range.

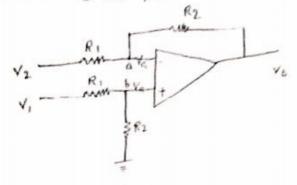
Charlette inter of The Stranger Electrical accelerate acces ~~~~~

For Vs = ±154 at 25%

- i) Input bias current IB = 5007 A (max)
- ii) Input offset-current Fio= 2007A (max)
- iii) Input offset voltage (Vi) = Goin V (max)
 - iv) Input Resistance (Ri) = 9MIL
 - 11) Output Resistance (Ro) = 75-11
 - vi) CMRR = 90 dB
 - vii) PSRR = 150 NV/V
 - viii) offset voltage drift = 154 V/°c offset current drift = 200 p A/°c
 - ix) Slaw rate = 0.5 V/HS
 - x) Large signal voltage gain AOL = 2X105
 - vi) Power Consumption = 85 MW.

Villemential Amplifier

The differential Amplifier is an Amplifier which amplifies the difference between the input signals. The difference amplifier circuit is as shown in the figure



Applying KLL at node a

$$\frac{V_a-V_2}{R_1}+\frac{V_a-V_c}{R_2}=0$$

 $\frac{V_0 = 0}{-\frac{V_0}{R_1} - \frac{V_0}{R_2}} = 0$ $\frac{V_0}{R_1} = \frac{V_0}{R_2} = 0$

$$\frac{-\frac{V_0}{R_1} - \frac{V_0}{R_2}}{V_0 - \frac{K_2}{R_1}V_1} = 0$$

$$\frac{\sqrt{2}}{R_1} + \frac{1}{R_2} = \frac{V_0}{R_2} + \frac{V_2}{R_1} \longrightarrow 0$$
Applying KCL at node's

$$\frac{\sqrt{a-v_1}}{2} + \frac{\sqrt{a}}{6} = 0$$

$$V_0\left(\frac{1}{R_1} + \frac{1}{R_2}\right) - \frac{V_1}{R_1} = 0$$

$$\Rightarrow V_{a}\left[\frac{1}{R_{1}} + \frac{1}{R_{2}}\right] = \frac{V_{1}}{R_{1}} - \frac{V_{2}}{2}$$

. From (1) &(2)

$$\frac{V_0}{R_1} + \frac{V_2}{R_1} = \frac{V_1}{R_2}$$

$$\Rightarrow \frac{Y_0}{R_2} = \frac{1}{R_1} (Y_1 - Y_2)$$

$$V_0 = \frac{R_2}{R_1} \left(V_1 - V_2 \right)$$

Therefore, the difference between two input voltage is amplified by Rz times in the differential Amplifier

(10)

The scenematic symbol of an ideal Op-Amp lass shown below.

Characteristics :

- 1) open loop voltage gain Aon = 0
- 2) Input Impedance R: = x
- 3) Output Impedance Ro-0
- 4) Band width BW = 8
 - 5) Zero offset i.e, Vo=0 When V1=V2=0

in practice. There are practical of Amps that can be made approximate to some of those characteristics.

Fred back to the show

The citility of an OP Amp can be greatly increased by providing negative feedback. There are two feedback Connections are used.

- i) Inverting Operational Amplifier.
- ii) Non investing operational Amplifier.

The electronics, A virtual ground is a node of a circuit that is at a seno potential, with out being directly connected to a ground potential It is a concept that made for easy explanation and calculation prospose as voltage is approximated to seno in ideal operational Amplifiers.

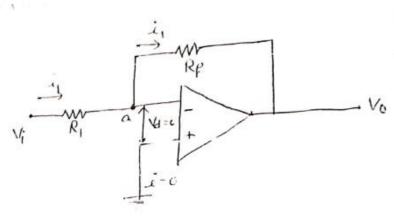
June Hry openational Implifie

In this, the output

Joltage Vo is fed back to the investing input terminal through Vi

the Re and R. Where Re is

the feed back resistor.



Input signal Vi (Ac or DC) is applied to the inverting input terminal through RI and Non-inverting input terminal of CP Amp is grounded.

Applying KCL at node a'.

$$\frac{V_i - V_a}{R_i} = \frac{V_a - V_o}{R_e}$$

Va=0 (: Vistual ground)

$$\frac{V_i^*}{R_1} = \frac{-V_0}{R_p}$$

$$\therefore A_{CL} = \frac{V_0}{V_i^*} = \frac{-R_p}{R_1}$$

Vi and Vo.

(11)

The circuit representation

Non- Investing Amplifier is

Shown.

Applying KCL at node a'

$$\frac{V_i - V_c}{R_f} + \frac{V_i}{R_i} = 0$$

$$\frac{V_{\epsilon}}{V_{i}} = 1 + \frac{R_{f}}{R_{i}}$$

· Closed Loop gain for Non-investing of Amp is AcL= 1+ RE

Ri

Voltage reliance

For a Non-inventing openational Rec

nplified if Re=0 & Ri=0

hen input voltage Follows the

etput voltage. This Circuit is

alled " Voltage follower."

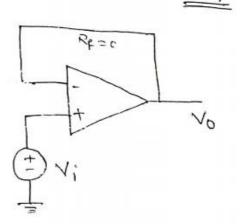
For a Non-inventing op-Amp ACL = 1+ RE

$$\frac{\sqrt{0}}{\sqrt{i}} = 1 + \frac{0}{2} = 1$$

$$\frac{\sqrt{0}}{\sqrt{i}} = 1$$

$$\frac{\sqrt{0}}{\sqrt{i}} = 1$$

$$\frac{\sqrt{0}}{\sqrt{i}} = 1$$



The Common mode rejection ratio is the ratio of evential mode gain to the Common mode gain.

CMRR (P) = / ADM/

Usually it is expressed in decibels.

Ideally ADM must be very large and Acm should be 2010. So, higher the value of CMRR, better is the Op-amp.

power supply rejection ratio is defined as the ratio of the change in the supply the change in input offset voltage due to the change in the supply voltage constant voltage producing it, keeping other power supply voltage constant. It is also called as Power supply constituty (PSV).

PSRR = ____________/constant VEZ

PSRR = DVics / Constant Vcc

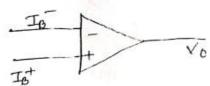
It is also called as Supply Voltage Rejection Ratio.

Operational Amplifier has two types of Characteristics

Those one 1) DC Characteristics

2) AC Character istics.

The DC Characteristics are Input bias Current, Input Offset Current, Input Offset Voltage and thornmal In an ideal op amp, we assumed that no current is drawn the input terminals. However, practically, input terminals do conduct small value of dc current to bias the input transistors. The base ments entering into the inventing and non-inventing terminals are as shown in IB and IB respectively. Even though both the transistors are identical, IB and IB are not exactly equal due to internal imbalences between the two inputs



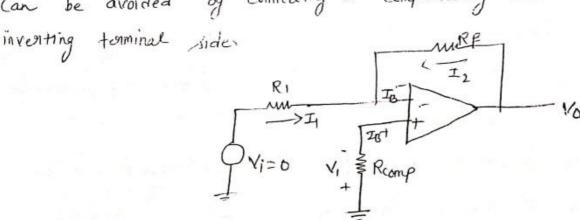
The no bias current given by the manufactures can be given as $I_B = I_B^+ + I_B^-$

For a 741 op-amp the bias current is 500 MA(er) less.

Because of this bios current, the voltage at the output

terminal is Vo= (IE) Rp.

To Compessate this output voltage because of bias current Can be avoided by Connecting a Compensating resistance at non-



Vi = Ist Rcomp Ist = Vi

Rcomp

The node of is at voltage (-V), because the voltage at the non-inventing input terminal is (-VI). So, with Vi-n we get

ctepel No

Ne

$$T_1 = \frac{v_1}{R_1}$$

$$T_2 = \frac{V_2}{R_P}$$

For Compensation, No should 2010 for Vi=0.

$$V_1 = V_2$$

$$\overline{I_{B}} = \overline{I_{1}} + \overline{I_{2}} = \frac{V_{1}}{R_{p}} + \frac{V_{1}}{R_{1}} = V_{1} \left(\frac{1}{R_{p}} + \frac{1}{R_{1}} \right) = V_{1} \left(\frac{R_{1} + R_{p}}{R_{1}R_{p}} \right)$$

$$\mathcal{N}\left(\frac{R_1+R_P}{R_1R_P}\right)=\frac{\mathcal{N}}{R_{comp}}$$

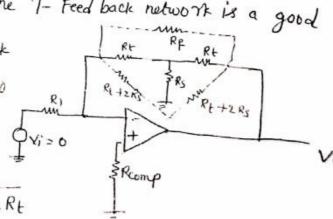
Current Compensation will work if both bias currents Ist and Is one equal. Since the input transistors cannot be made identical, there will always be some small difference between Is and Is. This difference is called the offset current Is. and can be written as

Because of this offset current, the output voltage can be given as Vo = R& Ios.

To compensate this, the T-feed back network is a good solution. This will allow longe feed back resistance while keeping the resistance to ground Low.

by T to a conversion

$$R_{f} = \frac{R_{t}^{2} + 2R_{t}R_{s}}{R_{s}} \Longrightarrow R_{s} = \frac{R_{t}}{R_{t}}$$



The op voltage due to ip offset voltage is Vo = (1+ Re) Vios where Vios = input offset voltage.

Slew Rate in Nove The slew rate is defined as the maximum rate of the slew rate is defined as the maximum rate of change of output voltage per unit time and is expressed in Volts/sec. For a 741 Op. Amp, slew rate is 0.5 V/sec. The slew rate change with i) frequency & Amplitude of ipsignal ii) Temperature.

Determination of Slew Rate:

Let us consider a voltage follower

Circuit. Vs = Vm sinut Vo = Vs = Vm sinut

Slew rate = dVo/ = d (Vmsinut)/max

= w Vm cosut/max

cos is marimum at cut=0 then cosut= coso=1

- : Slew rate = w Vm = 2 of Vm V/usec
 - : Slew rate for voltage follower is 2xf /m //usec

Op-Amp may be used to design a circuit whose output is summing Amplified or summer to The summer is classifical as inverting summer (or) Non-inverting Summer.

Inventing Summer :

applying KCL

$$\frac{Va-V_1}{R_1} \rightarrow \frac{Va-V_2}{R_2} \rightarrow \frac{Va-V_3}{R_3} \rightarrow \frac{Va-V_4}{R_5} = 0$$

but for an ideal Of-Amp the potential difference is 3010

$$\frac{O - V_1}{R_1} + \frac{O - V_2}{R_2} + \frac{O - V_0}{R_2} = 0$$

$$- \left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} \right) - \frac{V_0}{R_f} = 0$$

$$\frac{V_0}{R_F} = -\left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}\right)$$

Basic applications of OP Amp -

The Operational Amplifier has a count less applications

are classified as i) linear applications

(11) Non-Linear Applications.

the input signal in a Linews manners. Some linear Applications are added, Subtractor Nollage to Convented and Current to Voltage Convented incommendations.

In Non- Linear Applications the output signed basies with the input signal in a Non-Linear marrier Some NON- Linear Applicac

an e Sample and Held Great .. etc

in S Linear Applications;

i) Scale Change / En encor:

The basic inverting Operational Amytitien 18

Vi - ARI JAMES VE

The gains of the involting OP- Any is

ACL = -RE

if we make $R_1 = R_F$ then $A_{Ci} = -1$ then that circuit is called as inverted i.e. the output is 1800 out of phase with

In this case, the all the input voltages are and up but invented lon- investing Summer: The circuit diagram representation of Since voltage at the inventing terminal is Va, and to satisfy the ideal condition i.e. 1/2 = 0, to we have to mintain jours Va at + Ve' input terminal is By applying Kil $\frac{V_1-V_q}{R_1} \rightarrow \frac{V_2-V_q}{R_2} \rightarrow \frac{V_3-V_q}{R_3} \rightarrow 0$ $\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_1} - V_A \left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} \right) = 0$

 $V_{a} = \frac{\frac{V_{1}}{R_{1}} + \frac{V_{2}}{R_{2}}}{\left(\frac{1}{R_{1}} + \frac{1}{R_{2}} + \frac{1}{R_{5}}\right)}$

FOR Non Let RI = R2 = R3 = R then

We know that for Non-investing to coupur Voltage $V_0 = \left(1 - \frac{R_F}{R}\right) * V_a$

OF LU RF = 2R

then
$$\frac{y_0}{x} = (1 + \frac{y_1}{x}) \times V_a$$

$$= \frac{y_1}{x} (v_1 + v_2 + v_3)$$

PF = 2R then that mon-investing note Op- ping Can be wed as Adden.

Subtractor :-

The basic differential Amplifier Can be used as a Subtractory

with all rusistors one equal.

Applying KCL at node a

$$\frac{V_3}{P} - \frac{V_2}{P} + \frac{V_1}{P} - \frac{V_0}{P} = 0 \implies \frac{1V_1}{R} - \frac{V_2}{R} - \frac{V_0}{R} = 0 \implies 0$$

Applying KCL node bi

$$\frac{V_3-V_1}{R} + \frac{V_3}{R} = 0 \implies \frac{V_4}{R} - \frac{V_1}{R} + \frac{V_3}{R} = 0 \implies \frac{2V_3}{R} = \frac{V_1}{R} \rightarrow 2$$

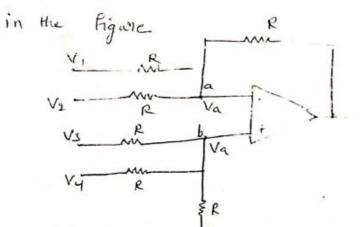
Con

$$\frac{V_1-V_2}{R}=\frac{V_0}{R}$$

working at a Subtractor, it we make all resistors as equal.

Addel - Subtractor :-

The circuit diagram for Addel - Subtractor is as shown



Apply KCL Node a'

$$\frac{V_1-V_a}{R}+\frac{V_2-V_a}{R}+\frac{V_0-V_a}{R}=0$$

$$\frac{1}{R}\left(V_1+V_2\right)+\frac{V_0}{R}-\frac{3V_9}{R}=0$$

$$\frac{1}{R}\left(V_1+V_2+V_0\right)=\frac{3V_q}{R}$$

Apply KCL at node b

$$\frac{V_{3}-V_{a}}{R}+\frac{V_{4}-V_{a}}{R}-t\frac{O-V_{q}}{R}=0$$

$$\frac{1}{R}(V_3 + V_4) - \frac{3V_a}{R} - 0$$

$$\frac{1}{\cancel{K}}(V_s+V_q)=\frac{3V_q}{\cancel{K}}$$

From (1) & (2)

.. The above circuit Can be used on for as beet for

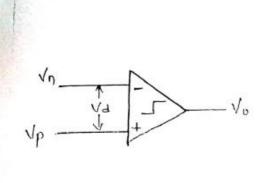
both Adder- Austracta circuit.

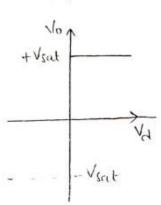
Iterrumentation Amplifier :

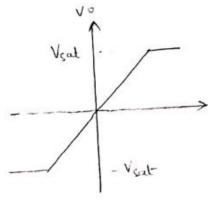
In a number of industrial and Consumer applications, one is regulare measure can a Control physical quantities. Some typical examples are measurement and control of temperature, humiding light intensity water Plow etc. These physical quantities wile usually measured with the help of transducers. The output of transducer has to be amplified. that it can drive the indicator (or) display system. This function The feature of instrument amplifier is as shown below i) High gain According

Comparator

A comparator is a circuit, which compares an input Signal with a known reference voltage. It is busically an open loop op-Amp with output I Vsal







Comparator signal

Ideal + practical

Comparator transistor

The comparator operation can be expressed as

Vo = +Vsat for Vp > Vn

Vo = -Vsat for Vp < Vn

- ⇒ For all possible Vp 7 Vn values, Vo is restricted to only two values + Veat 7 Veat . Thus the comparator accepts analog signals at the input and produces a binary signal at the cutput.
- → In ideal transfer characteristics of comparator, the Vertical line indicates the infinite gain practical op-Amp gains are typically in the Gange 103 to 105

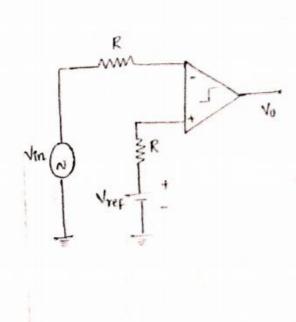
Non- Investing + Veat

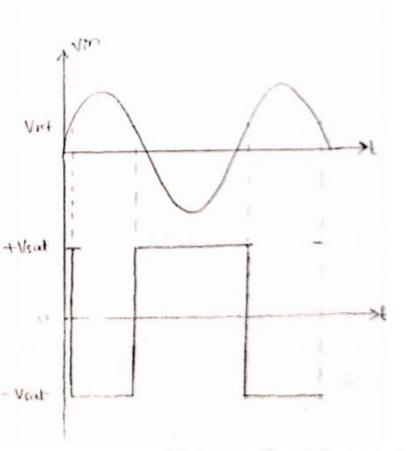
Here Enput signal is applied to the non-investing terminal and a setting dinage where a applied to the Enverting terminal It input voting is intoine their of their output at high

State (+ Vsai)

The output dollage do + dear for do > dref No Vent for Vin (Viet

Inverting Compression:





there—the input signed is applied to investing teams, and a deference voltage when is applied to non-shreeting teams.

It—the input voltage is above—the Voet then output is at low state (-Voet).

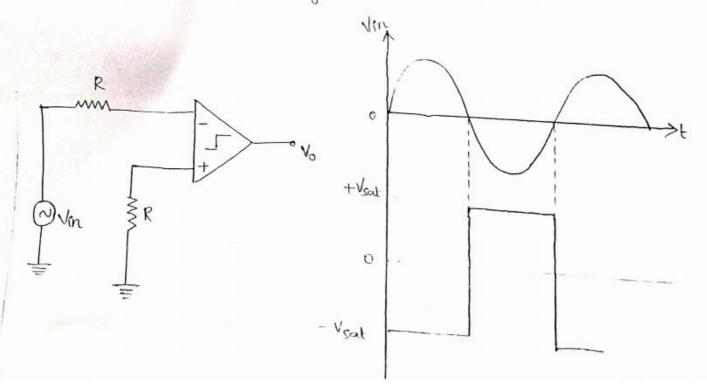
The output voltage No = - Vent for Vin > Veref No = + Vent for Vin < Vref

Application of compression:

- (1) Zero crossing latertal
- (2) Window detector
- (3) Time maker generator
- (4) phase detector
- (5) Noltage limiters

1) Zero crossing detector.

In the busic comparator circuit, its Vier to then,
the output will change from one state to another state every
time when input passes through sore.



Integrales circuit

From figure.

Apply ker at node in '

$$\frac{\sqrt{2n-\sqrt{n}}}{R_1} = \frac{d}{dt} \left(\sqrt{n-\sqrt{n}} \right)$$
 (The current through the capacilin $i=c\frac{dv}{dt}$)

$$\frac{\sqrt{n}}{R} = -C_F \frac{d}{dt} v_0 \qquad (: v_n - v_p = 0)$$

Making integration on both side,

$$\sqrt{90 = \frac{1}{R_1 C_F}} \int \sqrt{n} dt + \sqrt{c} (0)$$

where V.(0) is the integration constant of the Value of to at teo.

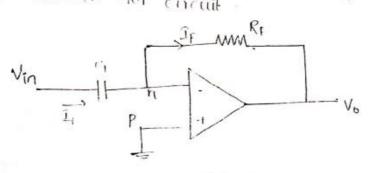
From eq (1), Vo(t) is directly proportional to the regardive integral of Vin (1)

Volt) is Enversely propositional to the time constant RICF.

Examples

Viri	Vo
Sine wave	Cosine wave
Square wave	Pricingulas nave
step input	Ramp Signal

operation of differentiation ic., the output wave is the desiration of input waveform. It R1 and CF of the integrator are interchanged as shown in lique we obtain a differentiation for circuit



Apply kul at node'n'

$$C_1 \frac{d}{dt} (V_{in} - V_{in}) - \frac{V_{in} - V_{in}}{R_F}$$

$$C_1 = \frac{dV_{in}}{dt} = \frac{V_0}{R_F}$$

$$V_0 = -R_F C_1 = \frac{dV_{in}}{dt}$$

Hence the cutput is the differentiation of input.

Apply taplace transform to equi) on both sides

Vo(s) = - RF CIS Vin(s)

(ransfer function Vo(s) = - S RF CI

Vin(s)

T(jw) = -jw RF CI

Gain | T(jw)| = WRF CI

The frequency at which gain =1 is No = RFCI