

1. Description

1.1. Project

Project Name	SWD
Board Name	custom
Generated with:	STM32CubeMX 6.14.1
Date	07/20/2025

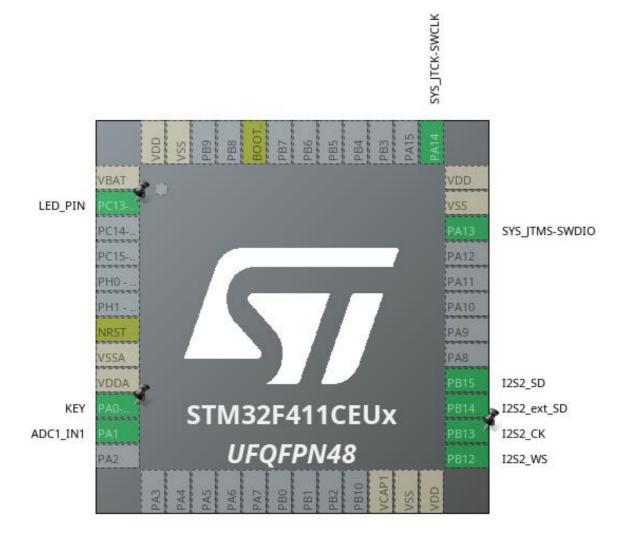
1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F411
MCU name	STM32F411CEUx
MCU Package	UFQFPN48
MCU Pin number	48

1.3. Core(s) information

Core(s)	Arm Cortex-M4

2. Pinout Configuration

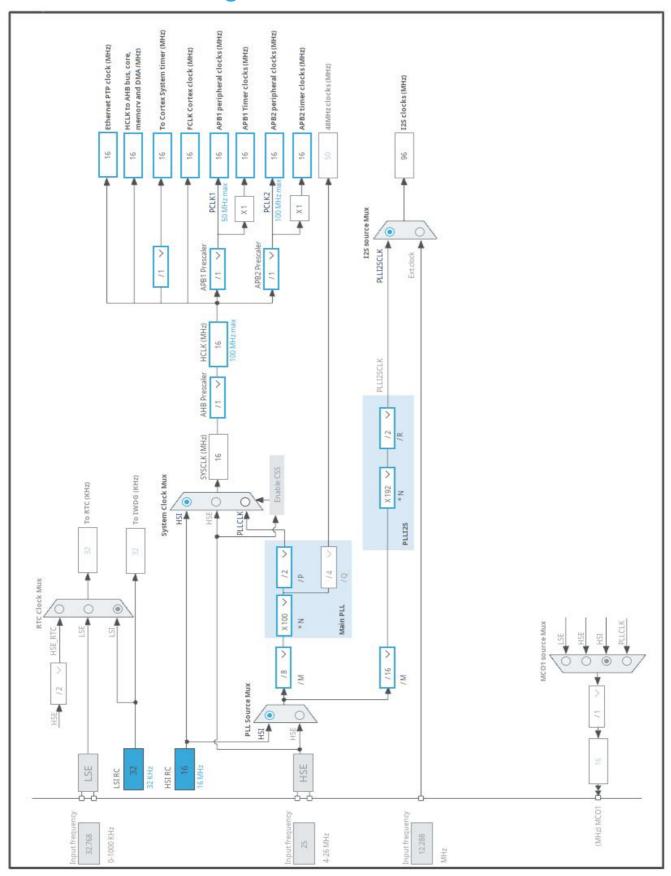


3. Pins Configuration

Pin Number UFQFPN48	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
2	PC13-ANTI_TAMP *	I/O	GPIO_Output	LED_PIN
7	NRST	Reset		
8	VSSA	Power		
9	VDDA	Power		
10	PA0-WKUP	I/O	GPIO_EXTI0	KEY
11	PA1	I/O	ADC1_IN1	
22	VCAP1	Power		
23	VSS	Power		
24	VDD	Power		
25	PB12	I/O	12S2_WS	
26	PB13	I/O	12S2_CK	
27	PB14	I/O	I2S2_ext_SD	
28	PB15	I/O	12S2_SD	
34	PA13	I/O	SYS_JTMS-SWDIO	
35	VSS	Power		
36	VDD	Power		
37	PA14	I/O	SYS_JTCK-SWCLK	
44	воото	Boot		
47	VSS	Power		
48	VDD	Power		

^{*} The pin is affected with an I/O function

4. Clock Tree Configuration



Page 4

1. Power Consumption Calculator report

1.1. Microcontroller Selection

Series	STM32F4
Line	STM32F411
мси	STM32F411CEUx
Datasheet	DS10314_Rev6

1.2. Parameter Selection

Temperature	25
Vdd	1.7

1.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

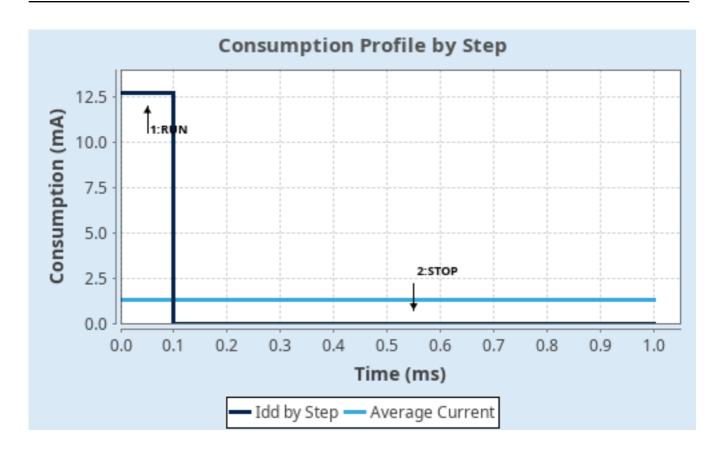
1.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	1.7	1.7
Voltage Source	Battery	Battery
Range	Scale1-High	No Scale
Fetch Type	SRAM	n/a
CPU Frequency	100 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator_LPLV Flash- PwrDwn
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	12.7 mA	9 μΑ
Duration	0.1 ms	0.9 ms
DMIPS	125.0	0.0
Ta Max	104.31	105
Category	In DS Table	In DS Table

1.5. Results

Sequence Time	1 ms	Average Current	1.28 mA
Battery Life	3 months, 19	Average DMIPS	125.0 DMIPS
	days, 6 hours	-	

1.6. Chart



2. Software Project

2.1. Project Settings

Name	Value
Project Name	SWD
Project Folder	/home/diogo/Desktop/estudos/PIC2/SWD
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_F4 V1.28.2
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

2.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power	Yes
consumption)	
Enable Full Assert	No

2.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_DMA_Init	DMA
4	MX_ADC1_Init	ADC1
5	MX_TIM2_Init	TIM2
6	MX_I2S2_Init	12\$2

3. Peripherals and Middlewares Configuration

3.1. ADC1 mode: IN1

3.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode Independent mode

ADC_Settings:

Clock Prescaler PCLK2 divided by 2

Resolution 12 bits (15 ADC Clock cycles)

Data Alignment

Scan Conversion Mode

Continuous Conversion Mode

Disabled

Enabled *

Discontinuous Conversion Mode

Disabled

DMA Continuous Requests Enabled *

End Of Conversion Selection EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion 1

External Trigger Conversion Source Timer 2 Trigger Out event *

External Trigger Conversion Edge Trigger detection on the rising edge

Rank 1

Channel 1
Sampling Time

84 Cycles *

ADC Injected ConversionMode:

Number Of Conversions 0

WatchDog:

Enable Analog WatchDog Mode false

3.2. I2S2

Mode: Full-Duplex Master 3.2.1. Parameter Settings:

Generic Parameters:

Transmission Mode Mode Master Transmit

Communication Standard I2S Philips

Data and Frame Format 24 Bits Data on 32 Bits Frame *

Selected Audio Frequency 48 KHz *

Real Audio Frequency 48.387 KHz *

Error between Selected and Real 0.8 % *

Clock Parameters:

Clock Source I2S PLL Clock

Clock Polarity Low

3.3. RCC

3.3.1. Parameter Settings:

System Parameters:

VDD voltage (V) 3.3
Instruction Cache Enabled
Prefetch Buffer Enabled
Data Cache Enabled

Flash Latency(WS) 0 WS (1 CPU cycle)

RCC Parameters:

HSI Calibration Value 16

TIM Prescaler Selection Disabled

HSE Startup Timout Value (ms) 100

LSE Startup Timout Value (ms) 5000

Power Parameters:

Power Regulator Voltage Scale Power Regulator Voltage Scale 1

3.4. SYS

Debug: Serial Wire

Timebase Source: SysTick

3.5. TIM2

Clock Source : Internal Clock

3.5.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value) 0

Counter Mode Up

Counter Period (AutoReload Register - 32 bits value) 332 *

Internal Clock Division (CKD) No Division

auto-reload preload Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit) Disable (Trigger input effect not delayed)

Trigger Event Selection Update Event *

* User modified value

4. System Configuration

4.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA1	ADC1_IN1	Analog mode	No pull-up and no pull-down	n/a	
1282	PB12	12S2_WS	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB13	I2S2_CK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB14	I2S2_ext_SD	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB15	12S2_SD	Alternate Function Push Pull	No pull-up and no pull-down	Low	
SYS	PA13	SYS_JTMS- SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK- SWCLK	n/a	n/a	n/a	
GPIO	PC13- ANTI_TAMP	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_PIN
	PA0-WKUP	GPIO_EXTI0	External Interrupt Mode with Rising edge trigger detection	Pull-up *	n/a	KEY

4.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC1	DMA2_Stream0	Peripheral To Memory	Low
SPI2_TX	DMA1_Stream4	Memory To Peripheral	Low

ADC1: DMA2_Stream0 DMA request Settings:

Mode: Circular *
Use fifo: Disable
Peripheral Increment: Disable
Memory Increment: Enable *
Peripheral Data Width: Half Word
Memory Data Width: Half Word

SPI2_TX: DMA1_Stream4 DMA request Settings:

Mode: Normal
Use fifo: Disable
Peripheral Increment: Disable
Memory Increment: Enable *
Peripheral Data Width: Word *
Memory Data Width: Word *

4.3. NVIC configuration

4.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority	
Non maskable interrupt	true	0	0	
Hard fault interrupt	true	0	0	
Memory management fault	true	0	0	
Pre-fetch fault, memory access fault	true	0	0	
Undefined instruction or illegal state	true	0	0	
System service call via SWI instruction	true	0	0	
Debug monitor	true	0	0	
Pendable request for system service	true	0	0	
System tick timer	true	15	0	
EXTI line0 interrupt	true	0	0	
DMA1 stream4 global interrupt	true	0	0	
DMA2 stream0 global interrupt	true	0	0	
PVD interrupt through EXTI line 16	unused			
Flash global interrupt	unused			
RCC global interrupt	unused			
ADC1 global interrupt	unused			
TIM2 global interrupt	unused			
SPI2 global interrupt	unused			
FPU global interrupt	unused			

4.3.2. NVIC Code generation

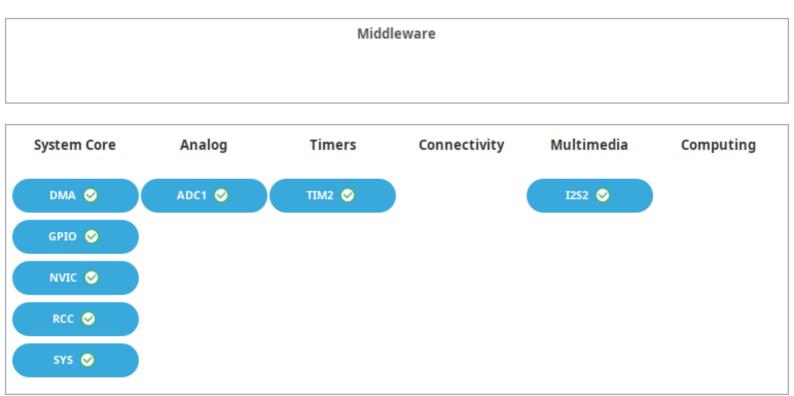
Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	false	false
Hard fault interrupt	false	false	false
Memory management fault	false	false	false
Pre-fetch fault, memory access fault	false	false	false
Undefined instruction or illegal state	false	false	false
System service call via SWI instruction	false	false	false
Debug monitor	false	false	false
Pendable request for system service	false	false	false
System tick timer	false	false	true
EXTI line0 interrupt	false	true	true
DMA1 stream4 global interrupt	false	true	true
DMA2 stream0 global interrupt	false	true	true

* User modified value				

5. System Views

5.1. Category view

5.1.1. Current



6. Docs & Resources

Type Link

BSDL files https://www.st.com/resource/en/bsdl_model/stm32f411_bsdl.zip

IBIS models https://www.st.com/resource/en/ibis_model/stm32f411_ibis.zip

System View https://www.st.com/resource/en/svd/stm32f4-svd.zip

Description

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