Automated Chip Tester - System Summary

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System Description

The aim of this project is designing an automated chip tester for the Superchip Platform[1]. These chips contain up to 16 different designs that must be tested individually (only one at a time); each design contains an oscillator, thus a measurement of the frequency must be done as well. Figure 1 shows a diagram of the blocks within the chip to be tested. All the designs share the input/output ports and each design is selected trough the local power supply (*individual vdd* on the diagram).

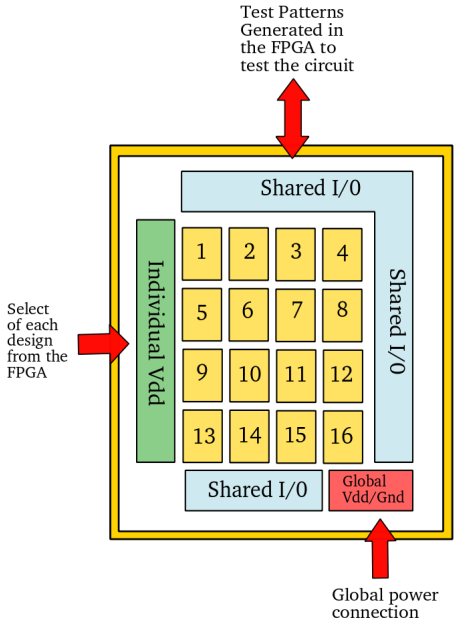


Figure 1: Diagram of the chip to be tested, from [1]

The chip tester will be implemented using an Altera DE2-115 Development Board, featuring an Altera Cyclone IV EP4CE115 and a budget of approximately £200 provided by the University of Southampton.

Figure 2 shows the block diagram of the system to be designed. An integrated SoPC using a NIos II processor running *µCLinux* will be used as a controller. It will interface with the SDCard and with a host computer over USB and via Ethernet. Test vectors and expected result vectors will be loaded via one of the aforementioned methods into fast on-board SRAM.

Control is then passed to the Test Harness or runner, which will load one set of stimuli and expected results at a time and pass them to the stimulus generator and results checker. Input and output of the stimulus generator and results checker will be synchronized with the external clock provided by the design, which is regenerated locally using a PLL.

The stimulus generator enables the Vdd of a particular design as requested by the test harness (runner) by outputting a 4-bit binary number to the external interface board. The interface board has

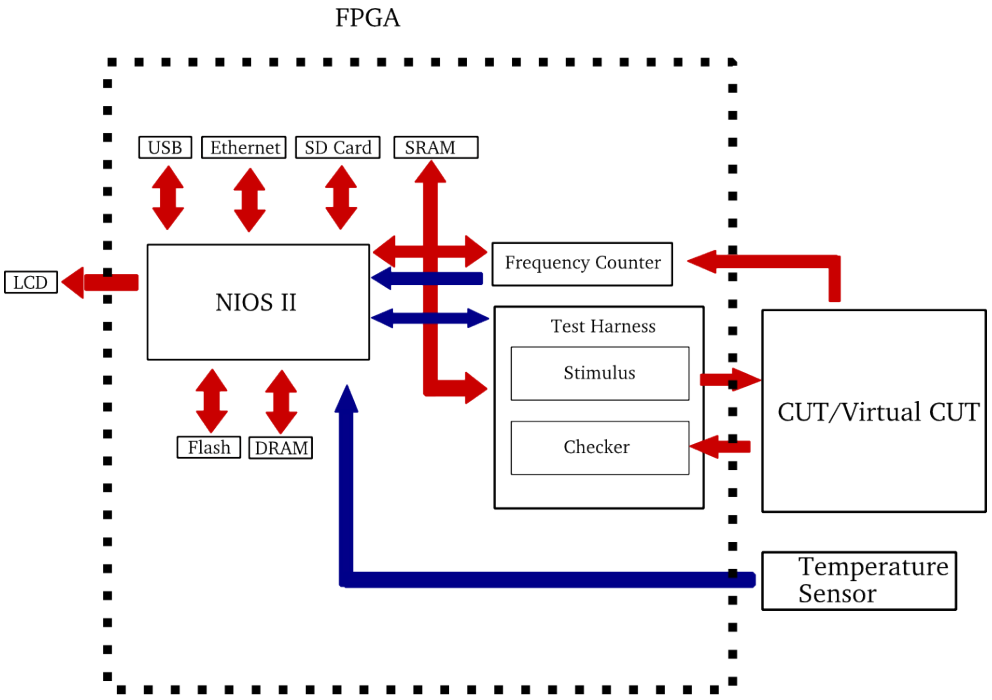


Figure 2: Block diagram of the initial system on the FPGA

a 4-to-16 decoder, with each line connected to a switch or transistor that will connect the external Vdd to one of the designs on the chip under test. The board will also contain a temperature sensor connected to a simple serial bus to record the temperature during testing, since this is a significant factor influencing IC performance and even failure.

The results of the verification of each design is stored back to SRAM including the actual output of the design under test. Once testing is complete, an interrupt is raised to the controller, which then reads the results from SRAM and stores and/or processes them.

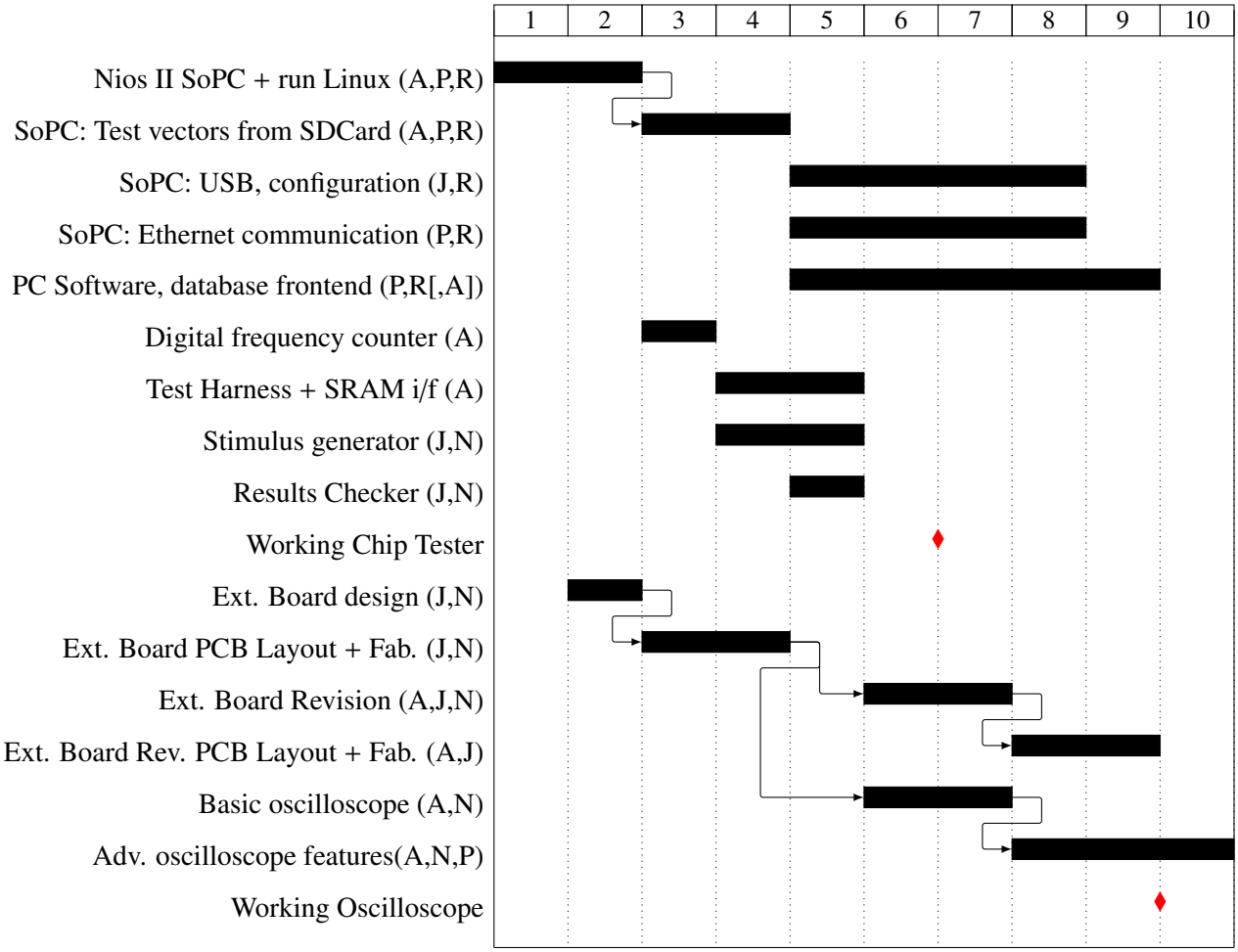
Additionally a digital frequency counter will be designed, which will allow measurement of the external clock frequency of each design.

As extended goal a simple one-channel digital storage oscilloscope will be developed. This allows for quick troubleshooting and analysis of the clock signal generated on the chip under test. An 8-bit 250MSps external ADC, differential amplifier and a passive filter will form the first version of the analog frontend. Triggering will occur on the sampled data on the FPGA.

If time permits this version will be refined by replacing the differential amplifier with a programmable gain amplifier to allow for different voltage ranges, as well as a variable filter to control the passband and proper external triggering implemented with comparators in the analog frontend.

The sampled analog data will be stored into the fast on-board SRAM and then processed and displayed, possibly using a graphics LCD or the VGA output.

Tasks



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Bibliography

[1] Wilson, P.R.; Wilcock, R.; McNally, I.; Swabey, M.;, *Innovative Teaching of IC Design and Manufacture Using the Superchip Platform* IEEE Transactions on Education, Vol. 53, Issue 2, pp. 297 - 305